

NODAL ANALYSIS OF CIRCUITS CONTAINING CURRENT CONVEYORS

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Abstract

A special method of the nodal analysis of the circuits containing several types of the multi-port current conveyors is presented in this paper. The method is based on the given regular and homogeneous models of the irregular current conveyors by the gyrators. Then a diakoptic solving and modification of the inversion of the admittance matrix is applied.

Keywords

Analogue circuits, analysis, current conveyors

1. Introduction

The recent progress of the analogue technology has bred modern active devices [1], i. e. the monolithic IC active components and functional blocks. Such devices are the multi-port current conveyors (CC), namely CC I, CC II CC II+/-, ICCII, DVCC, FDCC, UCC, etc. They are versatile and powerful building blocks for many signal-processing applications, with higher frequency operation and wider dynamic range, comparing with the classical operational amplifiers.

2. Current conveyor as an irregular element to nodal analysis method

Note that the current conveyors are irregular to nodal analysis method [2], having no defined the admittance matrix (\mathbf{Y}). Ideal current conveyor can be directly described by heterogeneous set of eq's only, e.g. by hybrid matrix.

The well known is three-port CC (Fig. 1), given by Sedra and Smith in 1968. Specially, the type CC3011, originally called the second generation (CC II) has been taken great interest and most of applications. It can be ge-

nerally described by the following hybrid matrix equation

$$\begin{bmatrix} 0 & a_1 & a_2 \\ b_1 & 0 & 0 \\ b_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix} = \begin{bmatrix} E_x \\ J_y \\ J_z \end{bmatrix}. \quad (1)$$

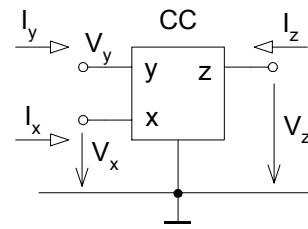


Fig. 1 General 3-port current conveyor

One of the modern CC's is a 5-port differential voltage current conveyor (DVCC), with balanced output CC501±2±2, which has been published in [3] and realized in CMOS FET technology. This block (Fig. 2) is described by the hybrid matrix equation

$$\begin{bmatrix} 0 & a_1 & a_2 & a_3 & a_4 \\ b_1 & 0 & 0 & 0 & 0 \\ b_2 & 0 & 0 & 0 & 0 \\ b_3 & 0 & 0 & 0 & 0 \\ b_4 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_{y1} \\ V_{y2} \\ V_{z1} \\ V_{z2} \end{bmatrix} = \begin{bmatrix} E_x \\ J_{y1} \\ J_{y2} \\ J_{z1} \\ J_{z2} \end{bmatrix}. \quad (2)$$

In eq's (1), (2), V_i and I_i are port variables of the CC, the E_i and J_i are variables of driving sources. The coefficients a_i and b_i are evaluated on some value from (0, +1, -1), what depends on the type of the CC. Similarly can be described the 4-port and 8-port CC as well.

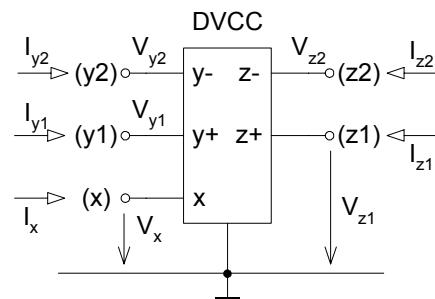


Fig. 2 General 5-port current conveyor

The heterogeneous mathematical description (1) or (2) given above has a corresponding electrical model, containing controlled sources, namely VCVS and CCCS. For the three-port CC (Fig. 1) and eq. (1), the model is given in the following Fig. 3.

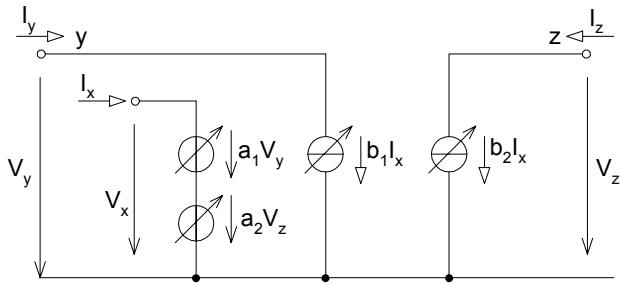


Fig. 3 Heterogeneous model of the three-port current conveyor

3. Homogeneous model of the CC regular to the nodal method

As was mentioned above, the circuit of the Fig. 3 is irregular to nodal analysis method (NAM). There, for the NAM is better to use homogenous model given in Fig. 4 containing three gyrators, having the admittance matrix \mathbf{Y} . This circuit (Fig. 4) was obtained from Fig. 3, modelling the VCVS and the CCCS by the gyrators, using the

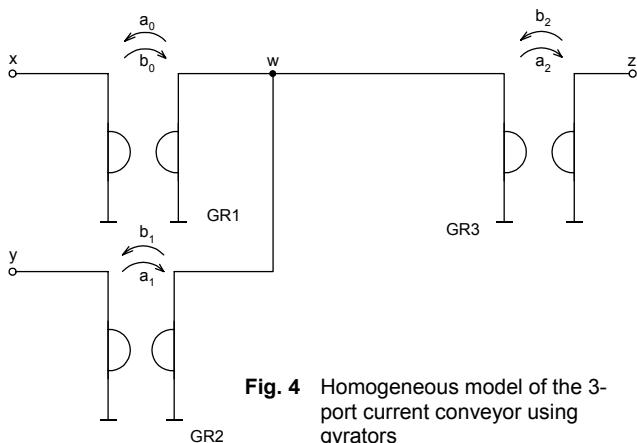


Fig. 4 Homogeneous model of the 3-port current conveyor using gyrators

transformation method given in [4]. The parameters of these gyrators, namely the transfer conductance (g_T), are corresponding with the parameters of the CC (a_i, b_i).

The gyrator in Fig. 4 can be replaced by two VCCS anti-parallel connected and the other equivalent circuit of the three-port CC is obtained (Fig. 5). There all elements have the admittance matrix and the NAM can be straightforward used. The equivalent circuit (Fig. 5) and the three-port current conveyor (Fig. 1) can be now described by the following matrix equation (3) in same basis of variables

$$\begin{bmatrix} 0 & a_0 & a_1 & a_2 \\ b_0 & 0 & 0 & 0 \\ b_1 & 0 & 0 & 0 \\ b_2 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_w \\ V_x \\ V_y \\ V_z \end{bmatrix} = \begin{bmatrix} 0 \\ J_x \\ J_y \\ J_z \end{bmatrix}. \quad (3)$$

There for the standard conveyors is $a_0 = -1$ and $b_0 = 1$.

On the other hand in the models (Fig. 4 or Fig. 5) and in the equation (3) is an additional internal node (w) and order of the admittance matrix, describing whole given net-

work, increases with the number of the CC's. Therefore better is to use a method of diakoptic modification given in [4]. The method is based on tearing of some branches and then subsequently solving modified subnetworks, step by step adding the particular torn branches.

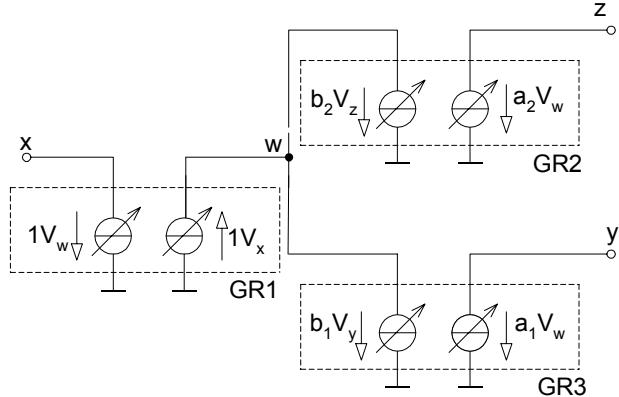


Fig. 5 Homogeneous model of the three-port current conveyor

4. Diakoptic solution of admittance matrix inversion

The certain network (N) is in initial modification divided in two subnetworks (A and B) and one coupling subcircuits (C). The subcircuits (C) can contain a standard passive admittances (\mathbf{Y}) or specially here the VCCS's as well, tearing the transfer conductance (g_T). The torn network (A+B) is described by blocked diagonal node admittance matrix, that can be easy inverted (separately \mathbf{Y}_A and \mathbf{Y}_B), with minimum numerical errors. In the first modification, the subcircuit C (torn branch) is now added to the original description and new inverse matrix is given by

$$\mathbf{Y}_{(1)}^{-1} = \mathbf{Y}_{(0)}^{-1} + k_{(0)} \mathbf{B}_{(0)}. \quad (4)$$

Here, $\mathbf{B}_{(0)}$ is the matrix of some additional increments given by formula (6), and $k_{(0)}$ is a correction coefficient (8). Furthermore the other coupling subcircuits are consecutive added. The formula (4) can be generalised to (5) for any $(m+1)$ -th step of the other modification

$$\mathbf{Y}_{(m+1)}^{-1} = \mathbf{Y}_{(m)}^{-1} + k_{(m)} \mathbf{B}_{(m)}. \quad (5)$$

The matrix $\mathbf{B}_{(m)}$ of the increments between two steps of modification is given by the product (6) of two vectors, namely \mathbf{Z}_{ZO} (7) and \mathbf{Z}_{OZ} (8), resulting from the previous step of the matrix modification

$$\mathbf{B}_{(m)} = \mathbf{Z}_{ZO} \cdot \mathbf{Z}_{OZ}. \quad (6)$$

The row vector, with dimension $(1 \times n)$, is defined as

$$\mathbf{Z}_{OZ} = [(z_{a1} - z_{b1}); (z_{a2} - z_{b2}); (z_{a3} - z_{b3}); \dots (z_{an} - z_{bn})] \quad (7)$$

and the column vector (with dimension $n \times 1$) by

$$\mathbf{Z}_{ZO} = [(z_{1c} - z_{1d}); (z_{2c} - z_{2d}); (z_{3c} - z_{3d}); \dots (z_{nc} - z_{nd})]^T, \quad (8)$$

where z_{ij} are the entries of the matrix $\mathbf{Z}_{(m)} = \mathbf{Y}_{(m)}^{-1}$ from the previous step and (n) is the order of this matrix. Here (a, b) are the nodes with the controlling voltages $V_{ab} = V_a - V_b$ (input port of the VCCS) and (c, d) are the nodes, where the controlled source (VCCS) is connected (output port of the VCCS). In other words, where is the torn branch with transconductance (g_T) . Note that the current flows from the node (c) to the node (d) .

The correction coefficient $k_{(m)}$ is given by

$$k_{(m)} = \frac{-g_{Tm}}{1 + g_{Tm} Z_m}, \quad (9)$$

where g_{Tm} is the increment of the added transfer admittance of the VCCS and the scalar Z_m is calculated as

$$Z_m = Z_{(a+b)(c+d)}. \quad (10)$$

5. Improvement of diakoptic matrix inversion

The procedure given above is rather complicated, adding six VCCS's (Fig. 5) for each conveyor one by one. Therefore a new modification of this algorithm is given now, taking the whole CC directly in one step, to improve the efficiency of this diakoptic method.

It can be mathematically described as follows. In the first step the passive subnetwork (usually RC) is regularly described by the diagonal admittance matrix \mathbf{Y}^* . Then, the inversion of the admittance matrix \mathbf{Y} , describing the whole circuit (including the CC), can be obtained by general formula of the diakoptic modification [4]

$$\mathbf{Y}^{-1} = \tilde{\mathbf{Y}}^{-1} + \tilde{k} \cdot \tilde{\mathbf{B}}. \quad (11)$$

There, the matrix \mathbf{B} of the increments is given as a product of the two vectors

$$\mathbf{B} = \tilde{\mathbf{Z}}_{Z_0} \cdot \tilde{\mathbf{Z}}_{0Z}. \quad (12)$$

Namely for the 3-port conveyor the column vector is (with dimension $n \times 1$)

$$\tilde{\mathbf{Z}}_{Z_0} = \begin{bmatrix} b_0 Z_{xx} + b_1 Z_{xy} + b_2 Z_{xz} \\ b_0 Z_{yx} + b_1 Z_{yy} + b_2 Z_{yz} \\ \dots \\ b_0 Z_{nx} + b_1 Z_{ny} + b_2 Z_{nz} \end{bmatrix}, \quad (13)$$

and the row vector (with dimension $1 \times n$)

$$\tilde{\mathbf{Z}}_{0Z} = \begin{bmatrix} (a_0 Z_{xx} + a_1 Z_{yx} + a_2 Z_{zx}), \dots \\ (a_0 Z_{xn} + a_1 Z_{yn} + a_2 Z_{zn}) \end{bmatrix}, \quad (14)$$

The both vectors above (13), (14) are resulting from the previous step of the matrix modification. The z_{ij} are the entries of the matrix $\tilde{\mathbf{Z}} = \tilde{\mathbf{Y}}^{-1}$, the (n) is the order of this

matrix and number of all nodes, the (x, y, z) are the corresponding nodes of the CC.

The correction coefficient in (11) is for 3-port current conveyor given by

$$\tilde{k} = -1/k, \quad (15)$$

$$k = k_3 = a_0 b_0 Z_{xx} + a_0 b_1 Z_{xy} + a_0 b_2 Z_{xz} + \\ + a_1 b_0 Z_{yx} + a_1 b_1 Z_{yy} + a_1 b_2 Z_{yz} + \\ + a_2 b_0 Z_{zx} + a_2 b_1 Z_{zy} + a_2 b_2 Z_{zz} \quad (16)$$

where a_i, b_i are corresponding with parameters in (3) and they are evaluated on some value from $(0, +1, -1)$.

The procedure above can be easily modified for multiple-port conveyors too. Then e.g. for the general 5-port current conveyor CC 50122 (Fig. 2), the correction coefficient (15), (16) is modified in following form

$$k = k_5 = \\ = a_0 b_0 Z_{xx} + a_0 b_1 Z_{xy1} + a_0 b_2 Z_{xy2} + a_0 b_3 Z_{xz1} + a_0 b_4 Z_{xz2} + \\ + a_1 b_0 Z_{y1x} + a_1 b_1 Z_{y1y1} + a_1 b_2 Z_{y1y2} + a_1 b_3 Z_{y1z1} + a_1 b_4 Z_{y1z2} + \\ + a_2 b_0 Z_{y2x} + a_2 b_1 Z_{y2y1} + a_2 b_2 Z_{y2y2} + a_2 b_3 Z_{y2z1} + a_2 b_4 Z_{y2z2} + \\ + a_3 b_0 Z_{z1x} + a_3 b_1 Z_{z1y1} + a_3 b_2 Z_{z1y2} + a_3 b_3 Z_{z1z1} + a_3 b_4 Z_{z1z2} + \\ + a_4 b_0 Z_{z2x} + a_4 b_1 Z_{z2y1} + a_4 b_2 Z_{z2y2} + a_4 b_3 Z_{z2z1} + a_4 b_4 Z_{z2z2} \quad (17)$$

The column vector (13) is grown up on this form

$$\tilde{\mathbf{Z}}_{Z_0} = \begin{bmatrix} b_0 Z_{xx} + b_1 Z_{xy1} + b_2 Z_{xy2} + b_3 Z_{xz1} + b_4 Z_{xz2} \\ b_0 Z_{y1x} + b_1 Z_{y1y1} + b_2 Z_{y1y2} + b_3 Z_{y1z1} + b_4 Z_{y1z2} \\ \dots \\ b_0 Z_{nx} + b_1 Z_{ny1} + b_2 Z_{ny2} + b_3 Z_{nz1} + b_4 Z_{nz2} \end{bmatrix} \quad (18)$$

and similarly is grown the row vector (14).

6. Illustrative example

As an illustrative example of the given procedure, the simple circuit of the Fig. 6 will be solved, assuming following values of resistors: $G_1 = 1$, $G_2 = 2$, $G_3 = 3$ and parameters (3) of 3-port CC: $a_0 = -1$, $a_1 = a_2 = 1$, $b_0 = b_2 = 1$, $b_1 = -1$.

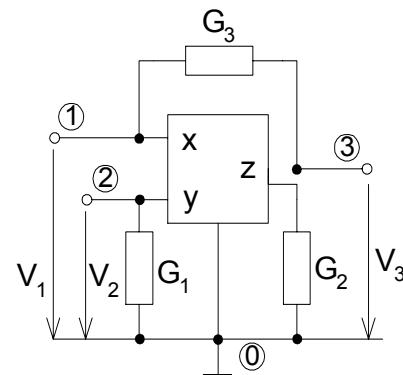


Fig. 6 Illustrative example

The nodal admittance matrix of the passive subnet-work (without the CC) has this form

$$\tilde{\mathbf{Y}} = \begin{vmatrix} G_3 & & -G_3 \\ & G_1 & \\ -G_3 & & G_3 + G_2 \end{vmatrix} = \begin{vmatrix} 3 & 0 & -3 \\ 0 & 1 & 0 \\ -3 & 0 & 5 \end{vmatrix} \quad (19)$$

Then the inversion of this matrix is

$$\tilde{\mathbf{Z}} = \tilde{\mathbf{Y}}^{-1} = \begin{vmatrix} 5/6 & 0 & 1/2 \\ 0 & 1 & 0 \\ 1/2 & 0 & 1/2 \end{vmatrix}. \quad (20)$$

The correction coefficient (15), using (16), results in

$$\tilde{k} = -1/(-5/6 - 1/2 - 1 + 1/2 + 1/2) = 6/8. \quad (21)$$

The row vector (14) is

$$\tilde{\mathbf{Z}}_{0Z} = [-1/3, 1, 0] \quad (22)$$

and column one (13)

$$\tilde{\mathbf{Z}}_{Z0} = [1, -3/4, 3/4]^T. \quad (23)$$

Then, the inverse matrix \mathbf{Z} is given by (11) and results in

$$\begin{aligned} \mathbf{Z} = \mathbf{Y}^{-1} &= \tilde{\mathbf{Y}}^{-1} + \tilde{k} \cdot \tilde{\mathbf{Z}}_{Z0} \cdot \tilde{\mathbf{Z}}_{0Z} = \\ &= \begin{vmatrix} 5/6 & 0 & 1/2 \\ 0 & 1 & 0 \\ 1/2 & 0 & 1/2 \end{vmatrix} - \begin{vmatrix} 1/3 & -1 & 0 \\ -1/4 & 3/4 & 0 \\ 1/4 & -3/4 & 0 \end{vmatrix} = \\ &= \begin{vmatrix} 1/2 & 1 & 1/2 \\ 1/4 & 1/4 & 0 \\ 1/4 & 3/4 & 1/2 \end{vmatrix}. \end{aligned} \quad (24)$$

7. Conclusion

The method given above, of the nodal analysis of the circuit containing several types of the multi-port current conveyors, can be applied on other types of the impedance converters as well.

Furthermore this procedure is suggested for computer aided analysis of large networks. An algorithm was proposed and this method was used in special software [5] for computer analysis of the circuits based on the current conveyors.

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References

- [1] TOUMAZOU, C., LIDGEY, F.J., HAIGH, D.G. Analogue IC design: The current-mode approach. London: Peter Peregrinus Ltd., 1990.
- [2] VLACH, J. Basic network theory with computer applications. New York: Van Nostrand Reinhold, 1992.
- [3] ELVAN, H.O., SOLIMAN, A.M. Novel CMOS differential voltage current conveyor and its applications. IEE Proc. Circuits Devices Systems. 1997, no. 3, p. 195-200.
- [4] RYBIN, A.I., DOSTÁL, T. Diakoptic modeling of VLS nonstandard networks. In Proc. of international conference Analysis, control & design SYS'95. Brno: AMSE, 1995, pp. 73-78.
- [5] MANJUK, I. J. Software for analysis of linear networks based on diakoptic modification. Kiev (Ukraine):Technical University of Kiev - KPI, 2001.

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