Frequency Stability Improvement in Direct Digital Frequency Synthesis

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Abstract. *The paper describes a digital frequency synthesizer that incorporates a novel method of the clock signal frequency versus temperature dependency compensation. The clock signal is derived directly from a dual-mode crystal oscillator (DMXO). With introducing the method, synthesized signal frequency versus temperature instability below ±0.15ppm can be obtained over a wide temperature range (between -45°C and +85°C). Since a temperature information is obtained directly from a crystal itself rather than from an external sensor, temperature offset and lag effects are eliminated.*

Keywords

Direct digital frequency synthesis, crystal oscillator stability.

1. Introduction

Frequency stability of a clock signal is usually assumed to determine frequency stability of a synthesized signal. However, if an evaluation of direct digital frequency synthesizer (DDS) frequency-tuning words is done according to actual frequency of the clock signal, then the frequency versus temperature (*f-T*) dependency of the synthesized signals may be reduced (i.e. the frequency versus temperature stability of the synthesizer may be improved).

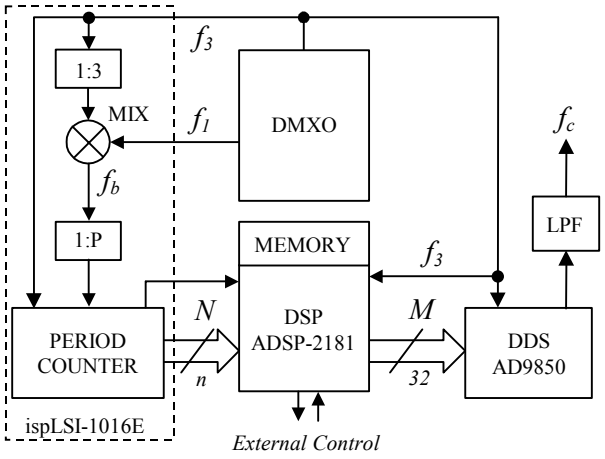

Fig. 1. Block diagram of the synthesizer.

The crystal self-thermometry using DMXO, which excites fundamental and 3rd overtone c-modes (i.e. slow-shear acoustic modes) of the crystal, has been published in [1]. Processing of actual frequencies of both the modes enables prediction of their frequency shifts due to ambient temperature changes. DMXO employing fundamental and 3rd overtone c-modes of a stress compensated (SC) crystal has been also incorporated in a microcomputer compensated crystal oscillator (MCXO) [2]–[4]. The self-thermometry eliminates temperature offset and lag effects since no external temperature sensor is used.

2. Operation of the Synthesizer

The synthesizer we have designed reduces the negative effect of the clock signal f-T dependency on synthesized signal frequency stability. The simplified block diagram of the synthesizer is shown in Fig. 1. The single-chip DDS frequency-tuning words are repetitively recalculated according to the actual temperature of the system.

The clock signal of the synthesizer is derived from the DMXO. A design of a DMXO circuit depends on parameters of the crystal that is considered. Due to the relatively low equivalent series resistances at the used SC crystal c-modes, a double gain loop emitter degenerative type DMXO circuit we have selected. The schematic diagram and detail description of such a DMXO configuration has been published in [1], [5].

We have selected a high quality 10-MHz fundamental c-mode frequency SC quartz crystal as frequency-determining element in DMXO. We have observed that the crystal fundamental c-mode and 3rd-overtone c-mode are free of significant anomalies in wide temperature range [5], [6].

An actual clock signal frequency $f_3(T)$ depends on the crystal actual 3rd overtone c-mode series resonant frequency (Fig. 2). T represents an actual temperature of the crystal in DMXO.

The DMXO simultaneously produces also the auxiliary signal with actual frequency $f_1(T)$ that depends on the

crystal actual fundamental c-mode series resonant frequency.

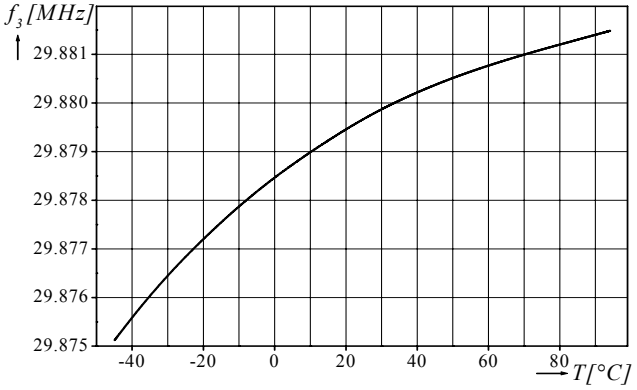

Fig. 2. SC crystal 3rd overtone c-mode series resonant frequency versus temperature.

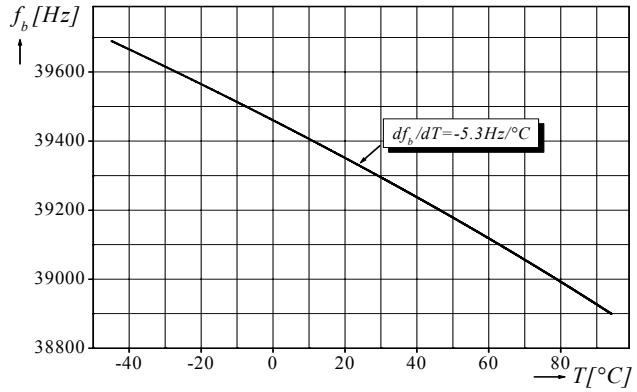

Fig. 3. Difference frequency f_b versus temperature.

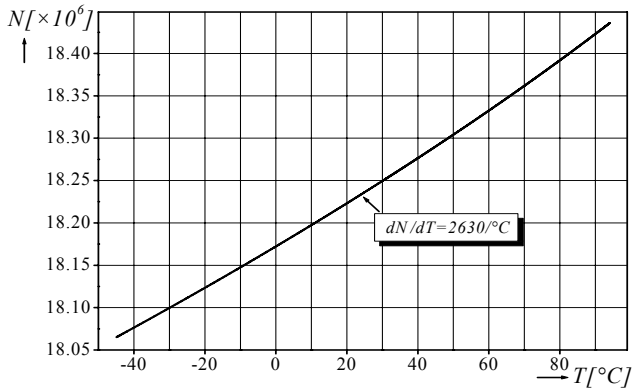

Fig. 4. Temperature number N versus temperature; P = 24000, N(25°C) = 18236200.

At the subtracting digital mixer output is available the difference signal with actual frequency $f_b(T)$ that is expressed by following equation

$$f_b(T) = f_1(T) - f_3(T)/3\,. \tag{1}$$

The difference frequency f_b versus temperature is illustrated in Fig. 3.

The period counter is cleared at each compensation cycle begin. The clock pulses are accumulated during P periods of the difference signal. After the P periods of the difference signal, the amount of the accumulated clock pulses represents an actual temperature number $N(T)$; it can be expressed by following formula

$$N(T) = \frac{f_3(T)}{f_b(T)}P = \frac{f_3(T)}{f_1(T) - f_3(T)/3}P\,. \tag{2}$$

Temperature number N versus temperature is shown in Fig. 4. Actual shift $\Delta N(T)$ of the temperature number is given by following equation:

$$\Delta N(T) = N(T) - N(25°C)\,. \tag{4}$$

Actual frequency of clock signal is calculated by solving a K-th order polynomial that approximates f_3 versus $\Delta N(T)$ dependency; it can be expressed by following formula

$$f_3\left(\Delta N(T)\right) = \sum_{i=0}^{K} a_i \cdot \left(\Delta N(T)\right)^i\,, \tag{3}$$

The coefficients of the polynomial are derived from a least squares curve-fitting routine using the data collected during a temperature calibration run. The calibration process requires an external precise frequency counter, a controllable chamber and a personal computer (PC). The PC controls the temperature in the chamber and records the calibration data (f_{3m}-data are read from the counter and N-data are read from the synthesizer). After the temperature-run is complete, the PC performs the curve fitting and finally sends the determined coefficients of the polynomial to the synthesizer. The synthesizer stores the received coefficients to the internal memory. The synthesizer communicates with the PC via a standard asynchronous serial interface (*External Control* in Fig. 1).

Compensated frequency-tuning word is calculated repetitively according to the actually required synthesized signal carrier frequency f_c using following equation:

$$M(f_c, T) = \frac{f_c}{f_3\left(\Delta N(T)\right)} \cdot 2^{32}\,. \tag{4}$$

The approximation polynomial solving and the frequency-tuning word calculation we have implemented within the 16-bit fixed-point digital signal processor (ADSP-2181).

A simple programmable logic device (ispLSI-1016E) was used to form additional digital parts of the synthesizer (the digital mixer, dividers and the period counter).

3. Experimental Results

When coefficients of the 9th order approximation polynomial are derived from least square curve-fit according to a complete set of f_3 versus ΔN data, which was collected over temperature range between -45°C and +95°C, the approximation gives the maximal error approx. ±0.15 ppm; it is shown in Fig. 5. The same type of the approximation gives the maximal error approximately ±0.1 ppm when the

coefficients are derived from least square curve-fit according to the another set of f_3 versus ΔN data, which was collected over reduced temperature range (above -20°C); it is shown in Fig. 6. Better results can be obtained utilizing segmented approximation with more polynomials [6].

Unfortunately, from the f_3 versus ΔN data sets, which we have recorded up to date, we can analyze a hysteresis only above a room temperature, where it usually not exceeds ±0.080 ppm.

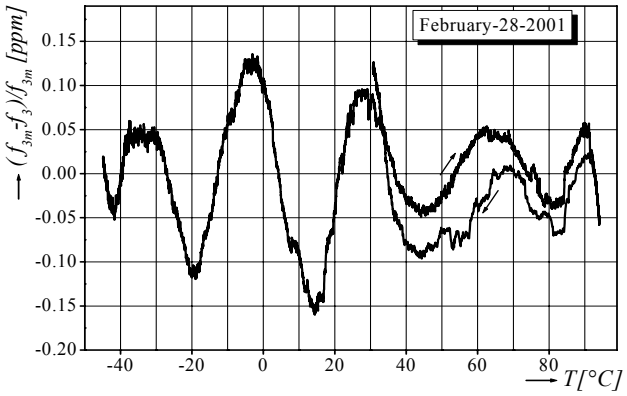

Fig. 5. Calculated frequency f_3 error versus temperature; f_{3m} is measured frequency of the clock signal.

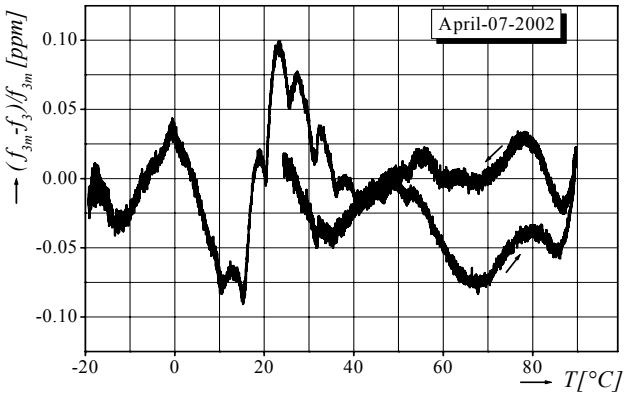

Fig. 6. Calculated frequency f_3 error versus temperature; f_{3m} is measured frequency of the clock signal.

Long-term stability of the synthesizer mostly depends on aging of the used SC crystal in DMXO. The aging approximately -6×10^{-8} per a year has been identified. The aging was compensated by recalculation of the constant term coefficient a_0 of the used approximation polynomial.

Two examples of power spectrum measured at the synthesizer output were published in [6]. Spectral purity of synthesized signals depends on the properties of DDS as well as on the clock signal spectral purity. The noise close to the carrier of the synthesized signals depends on the noise of the clock signal; therefore the noise particularly depends on the used DMXO and SC crystal properties.

On the other hand, locations and levels of discrete spurious components measured in the output power spectrum mostly depend on the fundamentals of the direct digital frequency synthesis (e.g. phase truncation or digital to analog conversion within DDS) [7]. In some instances the spurious components induced by DDS may also appear close to the carrier [8]. The noise very close to the carrier (below 1Hz) we could not measure due to limitation of the available measuring equipment (ANRITSU MS2802A spectrum analyzer) we have used.

4. Conclusions

Over a wide temperature range the frequency versus temperature instability of the DDS system can be essentially reduced implementing the described method of clock signal f-T dependency compensation without a temperature stabilization of a reference crystal oscillator (system clock).

The synthesizer we have described uses entirely digital compensation of its own clock signal *f-T* dependency; i.e. the compensation method does not require a tuning of crystal oscillator frequency.

Acknowledgements

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