Assembly Influence on the Small-Signal Parameters of a Packaged Transistor

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Abstract. *A detailed analysis of the assembly influence on the small-signal parameters of a packaged transistor is presented. A new method, based on 3D field simulation and mixed-mode scattering parameters approach is proposed. Differences in scattering parameters caused by assembly change are computed using the new proposed method and compared to the standard method based on admittance matrix. The differences, accuracy, error sources and suitability of both methods are discussed. Results are verified experimentally in microstrip line for two fundamental assembly changes of a transistor in SOT 343 package in frequency range 45 MHz - 18 GHz.*

Keywords

Assembly influence, Component modeling, EM simulation, Mixed-Mode scattering parameters.

1. Introduction

Radio-frequency and microwave-millimeter wave engineering stimulated by worldwide growth in digital communications have rapidly grown in importance in recent years. Successful realization of high-frequency circuits and systems is strongly dependent on computer-aided design (CAD). Due to the growing requirements of the commercial sector, a design has to be increasingly accurate and first-pass design success is required. Thus the availability of high accurate models is becoming acute.

Packaged SMD components, such as resistors, capacitors, diodes and transistors, can be successfully used in microwave planar and/or multilayer circuits up to tens of gigahertz on the assumption that the model of the component or scattering parameters (S-parameters) is known. Effective linear and nonlinear modeling of packaged components is strongly dependent on accurate characterization of the linear portion of the circuit [1]. The assembly may have a large impact on noise parameters of the packaged transistor. In principle, all of the noise figure parameters are influenced when the assembly is changed including the optimal input reflection coefficient Γ_{opt} for the best noise matching, R_N and minimum noise figure F_{min}. Because the package of the transistor can be considered as a lossless N–port the problem of noise figure parameters change can be solved using information about change in S–parameters.

S-parameters of the components are usually obtainable on data sheets of a producer. Only seldom information on reference planes positions, type of substrate and an assembly arrangement is given. To obtain reliable data the designer is forced to measure a component in a corresponding assembly arrangement on a vector network analyzer (VNA) on a test fixture. Once measured in a certain assembly arrangement the S-parameters are valid only for this arrangement. They are of little use if the arrangement is changed. In this case the designer is forced to re-measure the S–parameters. This makes the design process expensive and heavily time consuming.

The alternative and more efficient solution for S-parameters correction with respect to the assembly change is CAD modeling. A standard method based on Y-matrix and de-embedding in a circuit simulator is generally used for this purpose [2]. However, this method suffers from systematic errors and therefore it is not able to cover all cases of assembly change with required accuracy.

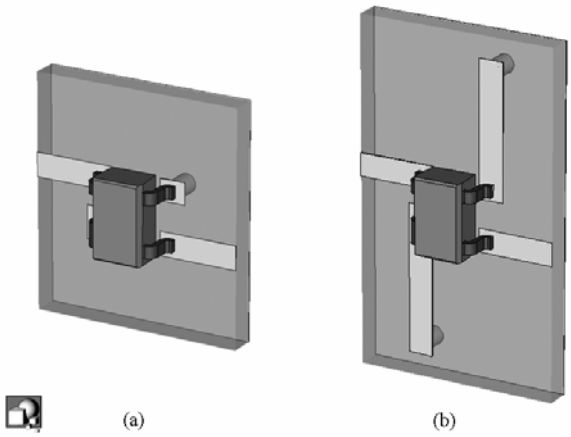

Fig. 1. Packaged SMD transistor. (a) Common emitter assembly. (b) Assembly with emitter feedback microstrip lines.

The aim of this paper is to analyze the problem of assembly influence on S–parameters of packaged components and to suggest a new method for their correction. The packaged transistor is used as a device under test for this purpose. The theoretical background as well as numerical and experimental results for the new method and a com-

parison to the standard method is discussed in the following sections.

2. Assembly Changes Studied

Usually a circuit with common emitter or source is used to determine the S-parameters of a transistor (Fig. 1a).

The assembly influence on the S-parameters of the packaged transistor was investigated for two fundamental cases. The first case assumes changes in the substrate parameters e.g. substrate thickness and/or permittivity. In this case the layout of the printed circuit board (PCB) is kept constant except the width of feeding microstrip lines being adjusted to 50 Ω impedance. The second studied case consists in change of the length of feedback microstrip lines, which are connected between emitter and ground. This assembly is often used in the design of oscillators in order to make the transistor potentially unstable, see Fig. 1b.

3. Modeling Methods

3.1 Standard Method

The standard method obtains the S-parameters of the new assembly by de-embedding of the original layout (soldering pads, via holes etc.) and re-embedding of the new layout, see Fig. 2. It is necessary to consider the transistor as a three-port network when the assembly is changed at the emitter or source lead. As just two-port parameters of the transistor are available the extension of 2-port Y matrix to 3-port Y matrix is used for this purpose using following formulae

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \rightarrow \begin{bmatrix} y_{11} & y_{12} & -(y_{11}+y_{12}) \\ y_{21} & y_{22} & -(y_{21}+y_{22}) \\ -(y_{11}+y_{21}) & -(y_{12}+y_{22}) & y_{11}+y_{12}+y_{21}+y_{22} \end{bmatrix}. \quad (1)$$

The extension of the Y matrix has an origin in circuit theory. Unfortunately the obtained small–signal parameters are valid only at low frequencies, where Kirchhoff's laws are valid and the cross–coupling between transistor leads can be neglected.

Generally, the extension of the Y matrix leads to systematic error at higher frequencies because the transistor package becomes distributed element circuit. The situation at higher frequencies can be explained using simplified equivalent circuit of the transistor assembly, which is illustrated in Fig. 3. The capacitor C1 (C2) represents parasitic capacitance between the base (collector) and ground while the capacitor C3 (C4) represents coupling capacitance between the base (collector) and the emitter. Only coupling capacitors C3 and C4 should be connected to the emitter pin according to Fig. 3a when the emitter of the transistor is supported by section of the microstrip line. In contrast the extension of the Y matrix results in the equivalent circuit in Fig. 3b. The original ground node (before assembly change) is considered as the emitter pin (after assembly change). Consequently the differences in equivalent circuit topology can lead to substantial error at higher frequencies. Despite this fact the extension of the Y matrix is implemented in many circuit simulators and the standard method procedure is widely used by producers of packaged transistors because of its simplicity [2]. Moreover, the standard method can be used without any knowledge of the transistor internal structure.

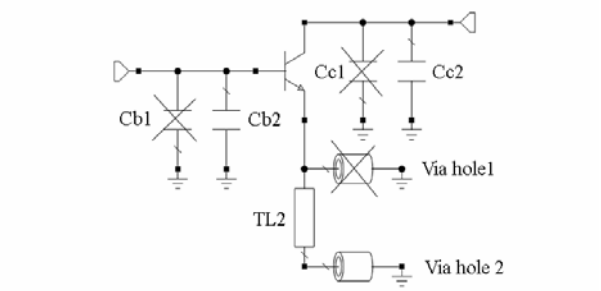

Fig. 2. Procedure of the standard correction method. (1) Original assembly. (2) New assembly.

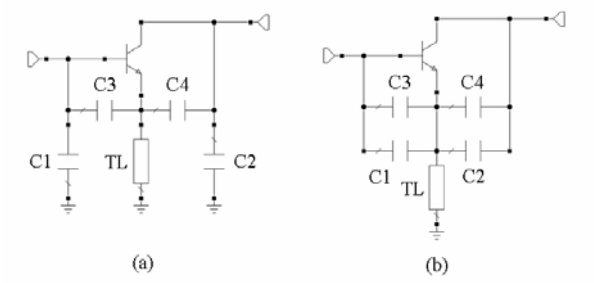

Fig. 3. Simplified model of the packaged transistor assembly with the emitter feedback microstrip line. (a) True equivalent circuit. (b) Wrong equivalent circuit after extension of Y matrix to 3-port.

3.2 Mixed-Mode Method

The new Mixed-Mode method is based on the electromagnetic simulation of the transistor package and the use of Mixed–Mode scattering parameters.

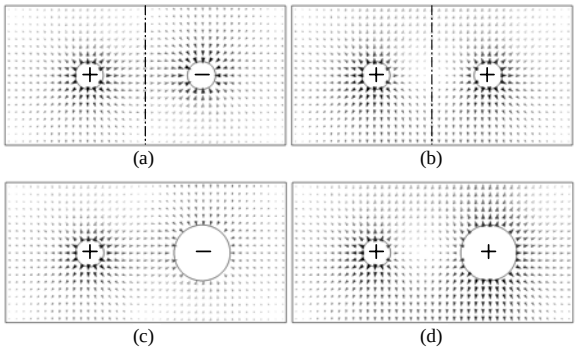

Fig. 4. Distribution of electric field at cross-section of a differential circuit. (a) Differential symetrical mode - 2 × odd mode. (a) Common symetrical mode - 1/2 even mode. (c) Differential asymetrical mode. (d) Common asymetrical mode.

The Mixed-Mode approach is generally used for a description of differential circuits where the excitation is considered between two signal conductors in contrast to single-ended circuits where only one signal conductor is used. Thus, one differential (Mixed-Mode) port can be considered as two single-ended ports and vice-versa. Such structure enables a propagation of two basic modes - differential and common mode - whereas two signal conductors are excited out of phase and in phase, respectively, see Fig. 4. Usually, odd and even mode is used for the description of the half structure when the cross-section is symmetrical, which is illustrated in Fig. 4a and Fig. 4b.

However, differential and common modes have to be used for the description of asymmetrical differential circuit, see Fig. 4c and Fig. 4d. More detail information about the definition of Mixed-Mode scattering parameters can be found in [3]-[5].

In this the most general approach the transistor package is considered as a Mixed-Mode 4-port, while the chip is assumed as a Mixed-Mode 2-port, see Fig. 5. Obviously, all sixty-four Mixed–Mode S–parameters of the transistor package cannot be assessed unambiguously from only 2-port measurements at external ports 1,2.

Fortunately, the model can be simplified to a mode converter only when two following approximations are applied. The first approximation consists of an assumption of the common global ground. In case that the packaged transistor is assembled into microstrip transmission line, Coplanar Waveguide (CPW) or grounded CPW the ground metallization can be considered as a global ground. In this case the Common mode is shorted at Mixed-Mode ports 1 and 2 in Fig. 5. Thus, the Mixed-Mode ports 1 and 2 are reduced to the simple single-ended ports and the model of the transistor package is simplified to a single-ended six-port network. The second approximation assumes that the chip is almost floating with respect to the global ground and therefore the interaction between the chip and the remaining circuit is provided mainly via Differential Mode. In this case the Common-Mode is terminated with an open end at the Mixed-Mode ports 3 and 4 of the package.

Now it is possible to obtain unambiguous differential 2-port parameters of the chip using 2-port single-ended measurement at external single-ended ports because the package model reduces to a 4-port having Mixed-Mode S-matrix

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3^d \\ b_4^d \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{13}^d & s_{14}^d \\ s_{21} & s_{22} & s_{23}^d & s_{24}^d \\ s_{31}^d & s_{32}^d & s_{33}^{dd} & s_{34}^{dd} \\ s_{41}^d & s_{42}^d & s_{43}^{dd} & s_{44}^{dd} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3^d \\ a_4^d \end{bmatrix}. \quad (2)$$

The S-parameters for a new assembly are obtained using de–embedding and re–embedding of the package 4-port network for the original and the new assembly, respectively. The procedure of the Mixed-Mode correction method is depicted in Fig. 6. A technique described in [6], [7] is used for the de-embedding of the package 4-port network.

The 4-port S-parameters for given assembly of the transistor package are obtained directly from the electromagnetic field simulation of the 3-D model, which is illustrated in Fig. 7. The termination of the Common-Mode with an open end is ensured explicitly using discrete differential internal ports in the electromagnetic field simulator. An implementation of the differential internal ports is shown in detail in Fig. 8. All objects in the vicinity of the transistor have to be included in the simulation in order to get a proper model of the assembly. Also the reference planes and port locations have to be set properly to avoid a violation of the near field of the packaged transistor.

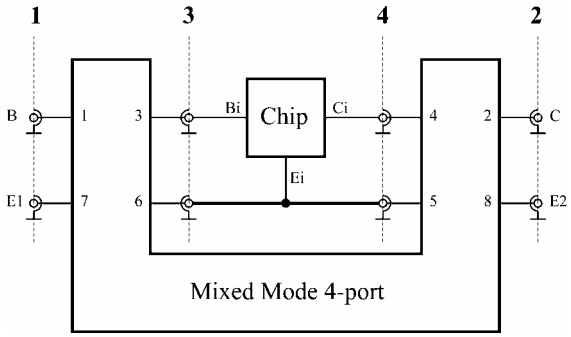

Fig. 5. Mixed-Mode model of packaged transistor.

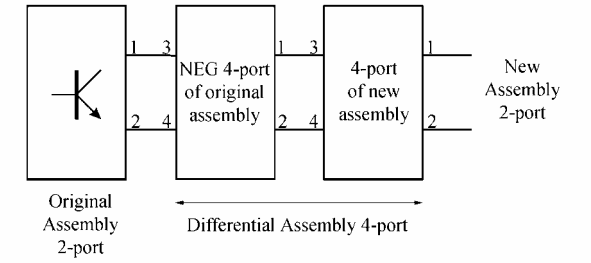

Fig. 6. Procedure of the Mixed–Mode correction method.

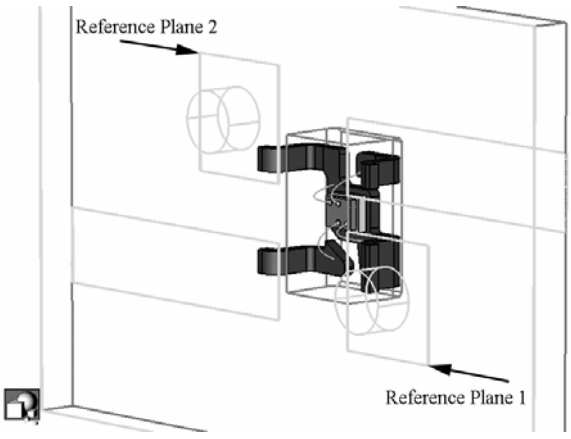

Fig. 7. Model of the transistor package SOT 343 including assembly in microstrip line footprint (common emitter circuit).

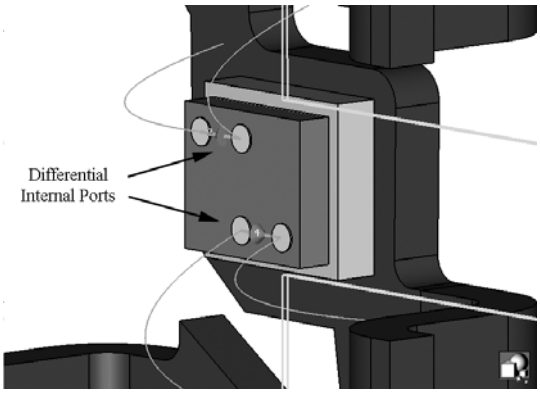

Fig. 8. Implementation of the differential internal ports for Mixed-Mode method.

4. Experimental Verification

The methods described above were verified experimentally for both fundamental assembly changes using an SMD bipolar transistor BFG 410W with the package SOT 343. Three different bias points V_{ce}/I_c={2V/10 mA, 1V/10 mA, 1V/1 mA} were set in the verification process.

The package SOT343 of the transistor including the assembly was modeled using the time domain electromagnetic field simulator CST Microwave Studio®. The dimensions of the package inner structure were obtained from sliced transistor using measuring microscope with resolution 1 μm.

Agilent E 8364A PNA was used for the measurement of external 2-port S-parameters. An Open, Short, Thru and Fixed load calibration set was used for the VNA calibration in frequency range from 45 MHz to 18 GHz. The reference planes were considered at the edge of the emitter soldering pads according to Fig. 7, which is 2.15 mm out from the center of the transistor.

The compliance between simulated data and measured data was evaluated in Microwave Office® using Average Least Square Error (ALSE) criterion,

$$ALSE = 20\log\frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{N}\left|S_{i,j}^{\mathrm{mod}} - S_{i,j}^{meas}\right|^2 \qquad (3)$$

where S^{mod} and S^{meas} are modeled and measured matrix of transistor S-parameters respectively.

4.1 Assembly Change in Substrate Permittivity

The differences in S-parameters were investigated for the substrate change from Rogers TMM4 substrate (h=0.508 mm, ε_r=4.5) to Arlon CuClad 233 (h=0.508 mm, ε_r=2.33). The layout of the PCB was kept excepting the width of feeding microstrip lines being adjusted to 50 Ω impedance. Measured S-parameters on TMM4 were transformed by the standard and the Mixed-Mode method and compared with S-parameters measured on CuClad 233. The resulting ALSE for this assembly change is shown in Fig. 9. Significant differences in measured data on both substrates can be seen. In Fig. 10 there are depicted measured S-parameters on CuClad 233 substrate and transformed S-parameters measured on TMM4.

It can be seen that both methods provide good agreement between measured and transformed data. Hence, the usage of simple standard method is preferable for this assembly change in comparison to more complicated Mixed-Mode method.

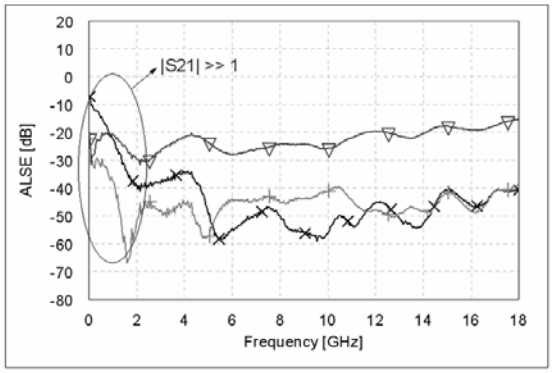

Fig. 9. ALSE for assembly change in substrate parameters at bias point 1V/10mA (∇ comparison of measurements on both substrates, + standard method transformation, × Mixed-mode method transformation).

4.2 Change in Length of the Feedback Microstrip Line

Three different lengths for the feedback microstrip line connected between emitter and grounding via holes were used for the assembly change. The PCB samples fabricated on Rogers TMM4 substrate (h=0.508 mm, ε_r=4.5) are depicted in Fig. 11. The ALSE and the corrected S–parameters are shown in Fig. 12-15 as representative results for this kind of assembly change. The measurement has not been processed for all combination of microstrip line length and bias points due to instability of the transistor for certain conditions. For instance, a 3 mm feedback microstrip line led to oscillation for all bias points mentioned above. As it could be expected the standard method offers good agreement with the measurement for a short emitter feedback microstrip line and frequencies below 7-9 GHz giving a poor accuracy for frequencies above 7-9 GHz. The Mixed-Mode method suffers from problems at frequencies where magnitude of S–parameters is greater than one. This results from high sensitivity of the corrected data obtained by the 3D modeling. This phenomenon is further discussed in the section on error analysis.

However the Mixed-Mode method provides significantly more reliable estimation of S-parameters for a new assembly. In spite of a large ALSE at "resonant frequencies" the Mixed-Mode method achieves significantly better

agreement with the measured data compared to the standard method.

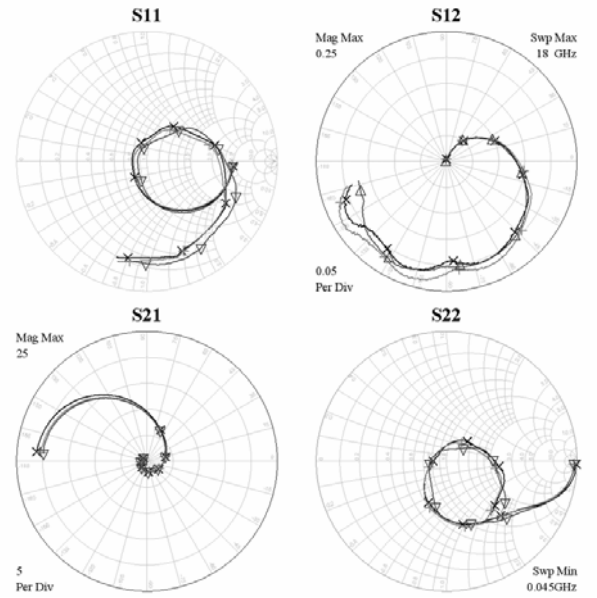

Fig. 10. S-parameters for assembly change in substrate parameters at bias point 1V/10mA (∇ measurement on CuClad 233, + standard method transformation, × Mixed-mode method transformation).

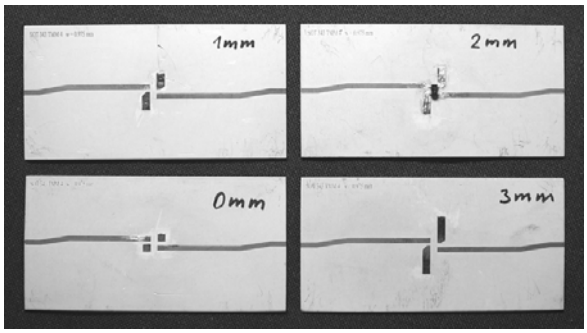

Fig. 11. Set of DUT samples with different lengths of the feedback microstrip line between emitter and via hole (substrate Rogers TMM4).

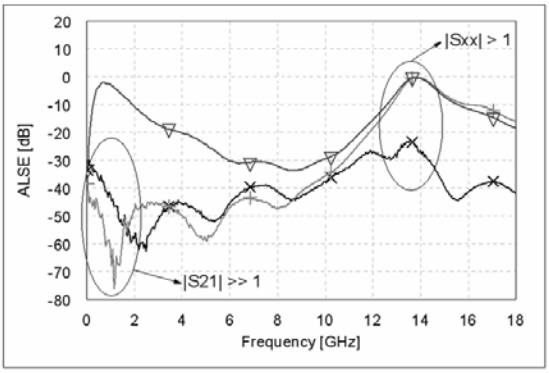

Fig. 12. Average least square error for assembly change in length of emitter feedback microstrip line from 0 mm to 1 mm at bias point 2V/10mA (∇ comparison of measurements, + standard method transformation, × Mixed-mode method transformation).

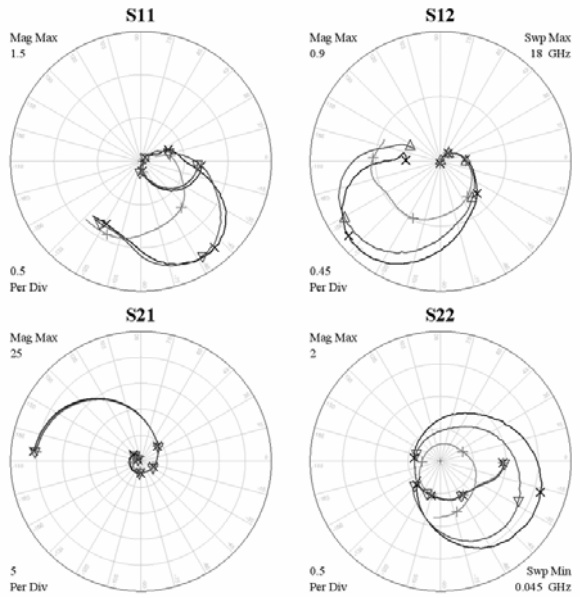

Fig. 13. S-parameters for assembly change in length of emitter feedback microstrip line from 0 mm to 1 mm at bias point 2V/10mA (∇ measurement, + standard method, × Mixed-mode method).

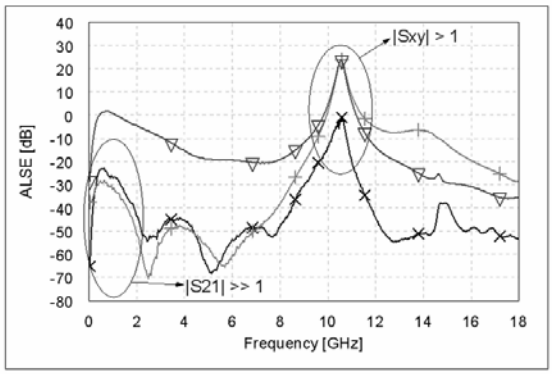

Fig. 14. Average least square error for assembly change in length of emitter feedback microstrip line from 0 mm to 2 mm at bias point 1V/10mA (∇ comparison of measurements, + standard method transform, × Mixed-mode method transform).

5. Error Analysis

The results obtained from the Mixed-Mode correction method suffer from poor accuracy at frequencies where the magnitude of an arbitrary S-parameter is greater than one. It was observed that the Mixed-Mode correction method at these frequencies is extremely sensitive to the simulation error of the differential assembly 4-port depicted in Fig. 6.

More detailed analysis of the simulation accuracy showed that the error in the order of 0.1 in 3D modeled S-parameters of the differential assembly 4-port causes 70 times greater error in the transformed S- parameters.

Nevertheless it is very important to know that high accuracy of the simulation of inner blocks of differential assembly 4-port is not necessary. If systematic errors in both simulations have a high repeatability and are close to

each other they are canceled in the de-embedding and re-embedding process.

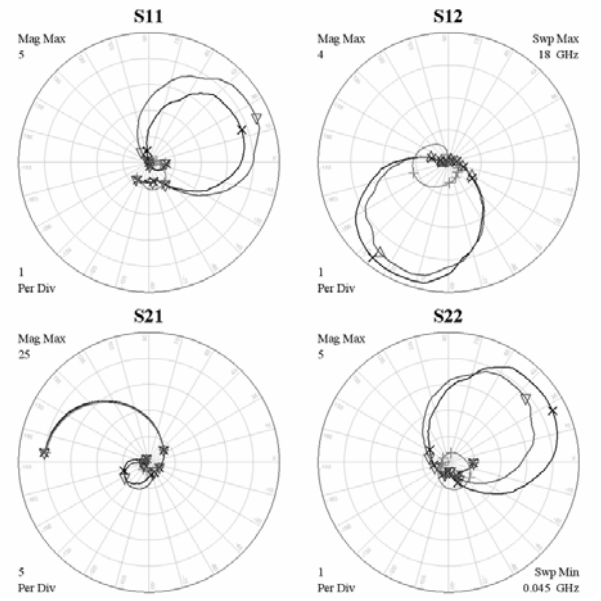

Fig. 15. S-parameters for assembly change in length of emitter feedback microstrip line from 0 mm to 2 mm at bias point 1V/10mA (∇ measurement for 2 mm microstrip, + standard method transform, × Mixed-mode method transform).

The mesh adjustment in the electromagnetic field simulator was found as the most important parameter with respect to simulation accuracy. Therefore the mesh was adjusted manually in the process of the experimental verification in order to get the best repeatability of the simulation errors. Moreover the reference planes and port locations were set properly avoiding a violation of the near field of the packaged transistor using a rigorous method, as described in [8].

The sensitivity analysis showed that the modeling is quite insensitive to other changes including permittivity change of the package material or the displacement of the transistor package. Measurement errors due to uncertainties of calibration elements on microstrip lines on soft substrates had also second order influence.

6. Conclusion

The influence on S–parameters of an assembly change for packaged transistors was analyzed using 3D time domain electromagnetic field simulator, a Mixed-Mode approach and precise vector network measurement. The new proposed Mixed-Mode method provides very good prediction of S-parameter differences giving significantly better agreement with measured data than the standard method used up to now. It also allows transformation of the S-parameters for a packaged component corresponding to a certain assembly into a new assembly without requiring experimental measurement. Further investigations of the EM-simulation improvements and the impact of the changed assembly on noise parameters are currently being researched.

Acknowledgements

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Karel HOFFMANN – for biography, see p. 90 of this issue.

Zbyněk ŠKVOR – for biography, see p. 90 of this issue.