The Utilization of Novel Bandpass Sigma-delta Modulator for Capacitance Pressure Sensor Signal Processing

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Abstract. *The paper deals with a novel approach to processing of pressure sensor signals. A bandpass sigma-delta modulator is used for this purpose. This technique is relatively new and it is not used widely, because this kind of modulator is usually utilized for wireless and video applications. Since the bandpass sigma-delta modulator works within its defined band it is resistant to offsets of its subcircuits. The main stages of this modulator are implemented by means of switched-capacitor (SC) technique. The article presents the basic ideas of this approach and simulation results of the first order of ideal and real modulator. The paper also shows the design of the phase locked loop (PLL) block for synchronization of sensor signal and modulator driving signal. The simple evaluation board was fabricated for confirmation of the proposed principle. Also shown are the results of the chip testing, the modulator layout and the design and test results of the second order of bandpass sigma-delta modulator briefly.*

Keywords

Bandpass sigma-delta modulation, pressure measurement, capacitance sensor.

1. Introduction

Bandpass sigma-delta modulators [1], [2], [3] are well suited for direct conversion of the complex analog signal into two digital values representing its amplitude and phase. They are well suited for demodulation of quadrature amplitude modulation (QAM) signals. Once the QAM signal is digitized, most of the signal processing tasks, such as channel filtering, demodulation etc., can be easily done in the digital domain with a high degree of programmability. Induced noise and high sampling frequencies require corresponding electronic technology as it is used in the implementation for GPS/GSM communication systems.

The binary flux delivered by the bandpass sigma-delta modulator output is downconverted by digital multiplier and transformed into the digital number in the lowpass digital filter. The whole structure represents bandpass sigma-delta analog to digital converter. Coherency between input signal f_{in} and clock frequency ($f_s = 4.\ f_{in}$) makes the converter phase sensitive. Because of this fact two lowpass digital filters controlled by the f_s and shifted by $\pi/2$ represent a converter of the input vector into its digital representation.

There are several similar applications of bandpass sigma-delta modulator [6], [7], [8], [9], [10] for sensoric measurement, but the authors introduce a new application of bandpass sigma-delta modulator as the processing circuit of capacitive pressure sensor as complex SoC with output signal with the direct digital outputs representing real and imaginary components of the input vector. The simple first order bandpass sigma-delta modulator was designed for integrated sensor system using the CMOS 0.7 μm technology. The defined narrow band represents an advantage in the offset suppression such as operational amplifier, delay stage and summator. The first order modulator is tuned at 100 kHz sampling frequency. The paper shows a comparison of simulation results of a proposed ideal and real bandpass sigma-delta modulator. The contribution also presents first real-time functionality test results. The article also presents measurement results of redesigned second order bandpass sigma-delta modulator. The required PLL circuit is discussed, too.

2. Structure of Bandpass Sigma-delta Modulator

Fig. 1 shows the block diagram of the bandpass sigma-delta modulator [5]. It contains a band-pass filter, an N-bit quantizer and a digital to analog converter connected in a feedback loop. The bandpass filter can be synthesized by cascading two or more second-order biquadrate filters or resonators, which must have a sharp transfer function and well-defined resonance at f_n. These resonators may be implemented as discrete-time filters using either SC or SI (switched current) techniques.

Let consider a $2L^{th}$-order bandpass filter composed of a cascade of L resonators with transfer function given by

$$H_R(z) = \frac{1}{(1 - z^{-1} z_n)(1 - z^{-1} z_n^*)}\ , \qquad (1)$$

where z_n and z_n * are the conjugate-complex poles of $H_R(z)$.

The output of the modulator in Z-domain, assuming a quantization error, is

$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E_q(z) \quad . \tag{2}$$

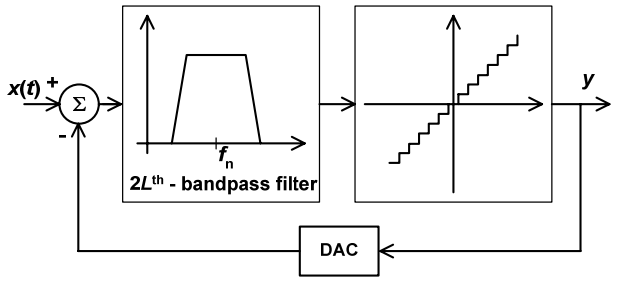


Fig. 1. Basic block diagram of a bandpass sigma-delta modulator.

The signal transfer function (STF) and noise transfer function (NTF) are as follows

$$S_{TF}(z) = \frac{\left[N_R(z)\right]^L}{\left[N_R(z) + (1 - z^{-1}z_n)(1 - z^{-1}z_n^*)\right]^L} \quad , \tag{3}$$

$$N_{TF}(z) = \frac{\left[(1 - z^{-1}z_n)(1 - z^{-1}z_n^*)\right]^L}{\left[N_R(z) + (1 - z^{-1}z_n)(1 - z^{-1}z_n^*)\right]^L} \quad . \tag{4}$$

The output transfer characteristic for the proposed bandpass sigma-delta modulator is

$$Y(z) = X(z).z^2 + E_q(z)\left(1 + z^2\right) \quad . \tag{5}$$

Power density after noise shaping in the spectral domain is

$$\varepsilon_{NS}^2(f) = \varepsilon_q \frac{4}{f_S}\left(1 + \cos\frac{4\pi f}{f_S}\right) \quad . \tag{6}$$

Fig. 2 shows the measurement chain containing a capacitive pressure sensor where one branch is the sensing branch and the other is the reference branch. The PLL circuit provides coherent processing of the input signal in the bandpass sigma-delta modulator. While pressure influences the ΔC_X capacity, humidity impacts the ΔG_X conductivity of the sensing branch. The preprocessing circuit converts $G_X + j\omega C_X$ complex conductance by the bandpass sigma-delta modulator and two digital lowpass filters into digital value of the real and the imaginary part. The digital resolution is proportional to the time window of the digital low pass filter. The bandpass sigma-delta modulator is controlled by the coherent input frequency from the PLL circuit. The digital output values are determined by the quantized vectors in all three switch positions as follows

$$\begin{aligned} u_1 &= -Ru\left[\, j\omega\left(C_N + \Delta C_X\right) + G_N + \Delta G_X \,\right], \\ u_2 &= -Ru\left[\, j\omega C_N + G_N \,\right], \\ u_3 &= -Ru / R. \end{aligned} \tag{7}$$

The phase shift of the processing block is suppressed by the compensation principle. The difference of the digital values from the output of the low-pass filter in position 1 and 2 normalized to the value measured in position 3 is expressed by the formula (8). Here measured changes of capacity and resistance changes are obtained by

$$\frac{u_1 - u_2}{u_3} = R(j\omega\Delta C_X + \Delta G_X) \quad . \tag{8}$$

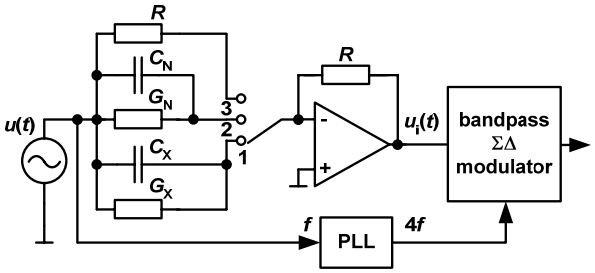


Fig. 2. Measurement chain with bandpass sigma-delta modulator.

The bandpass sigma-delta modulator is tuned to 100 kHz of sampling frequency. The maximal noise suppression is achieved at the central frequency

$$f_C = \frac{f_S}{4} = \frac{10^5}{4} = 25 \text{ kHz}. \tag{9}$$

3. Design of Bandpass Sigma-delta Modulator

The switching of the inputs is synchronized with internal clock of the modulator and it is implemented in the SC technology.

The ideal modulator consists of an input S/H circuit, a summator, four delay circuits, a comparator and a DAC connected in a closed loop. There are several auxiliary stages mainly D flip-flops and an XOR logic gate.

The behavior of the modulator was simulated with an input harmonic signal of frequency 25 kHz. The signal amplitude is 0.5 V with offset voltage 0.5 V. The value computed by CADENCE software tool is average value of logic 1 and logic 0 (represented as 5 V and 0 V, respectively). It means that number on the *y* axis is the ratio between logic levels appropriate to input amplitude.

It can be seen from Fig. 7 that values of XOR output are quite linear and appropriate to current values of input signal. The beginning of the curve is affected by the start-up phase of the modulator and should not be considered.

The real bandpass sigma-delta modulator circuitry is depicted in Fig. 3. The time delay and S/H circuits are designed using the SC technique. The comparator contains a latch at the input. The modulator was designed and simulated in the CADENCE software using the CMOS 07 technology, provided by AMI Semiconductor within the

EUROPRACTICE project. The power supply is 5 V. The offset of the basic loop is 140 μV.

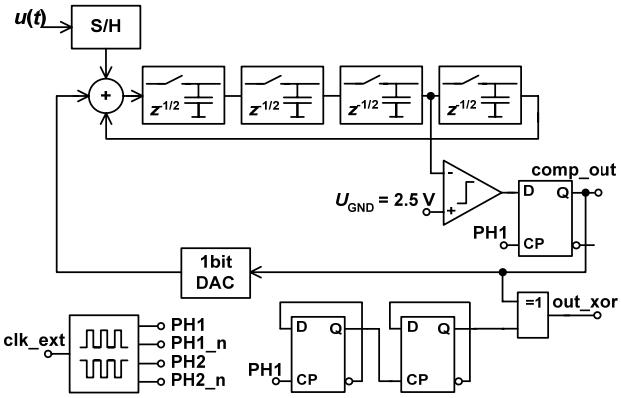


Fig. 3. Block diagram of real bandpass sigma-delta modulator.

4. Phase Locked-Loop

The PLL stage is designed utilizing the structure [6], as shown in Fig. 4. The comparator converts the input sine wave into the pulse form. Then the phase detector, which is a bipolar charge pump, compares the phase between these pulses and the signal generated by the voltage controlled oscillator (VCO).

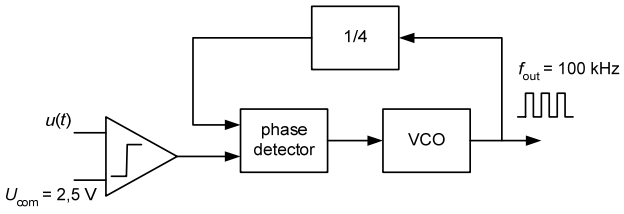


Fig. 4. Block diagram of designed PLL.

The VCO is starving ring oscillator [6] with current controlled invertors as shown in Fig. 5. It is designed for 25 μA driving current at the control voltage of 1.3 V.

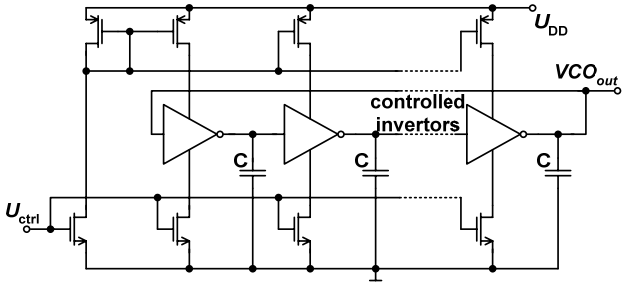


Fig. 5. Controlled VCO.

In order to achieve low frequency in the wide controlling range the ring oscillator consists of 5 controlled invertors.

The phase detector detects the phase difference between the reference signal and the feedback signal from the VCO and frequency divider. A charge-pump with a tri-state phase-frequency detector [6] is always used for frequency synthesizer implementation. Since the VCO generates the desired signal at the predefined value of control voltage (1.3 V), the control signal from the RC filter has to be stabilized with low sensitivity on any changes at input. That is why the sensitivity divider was designed and added into the charge pump as the third stage after the simple RC filter.

Fig. 6 shows the PLL output signal (VCO_OUT) and the suspension process of the input signal and the VCO signal.

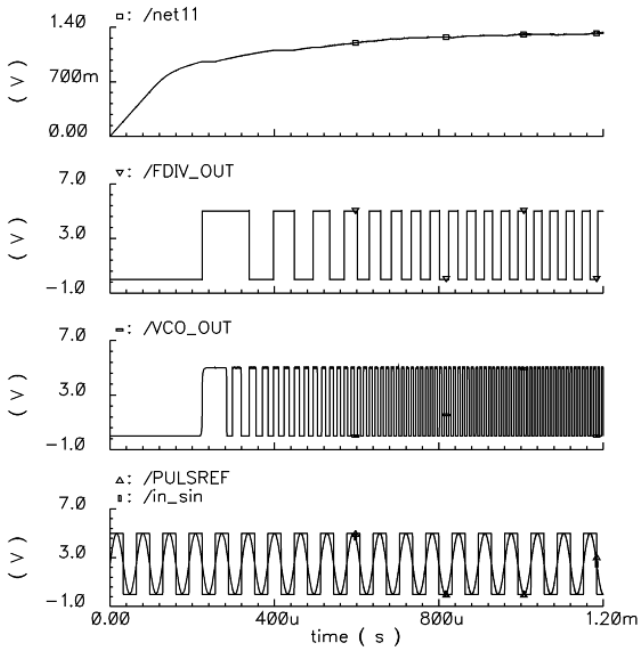


Fig. 6. Confirmation of designed PLL functionality.

The suspension process is accomplished within 1.1 ms, which is sufficient for the proposed application. The signal net11 shows settling of the control voltage during the suspension process and signal FDIV_OUT is the output signal from the divider. The signal in_sin is input signal fed into the modulator and signal PULSREF is its converted representation made by comparator.

5. Simulation Results

Since this is the first implementation of that kind of chip for capacitive pressure sensors, there are many auxiliary pins used for testing purposes. The aim of this arrangement is to obtain maximum information about the behavior of each stage of bandpass sigma-delta modulator. The most critical parts are blocks using the SC approach, because there are many nonidealities and error sources, mainly clock feedthrough and noise.

The output average values of the ideal and the real bandpass sigma-delta modulator depending on the magnitude of analog input signal (range 0 to 1 V) are shown in Fig. 7 and 8, respectively. It can be seen that the output of XOR is mostly linear, which is an expected result. The

beginning of the curve for the ideal bandpass sigma-delta modulator is affected by starting conditions set before simulation.

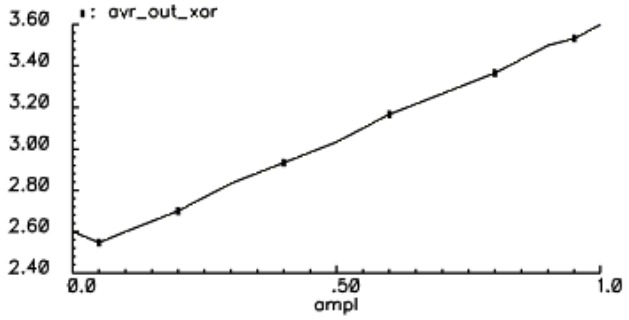


Fig. 7. Transfer characteristic of ideal bandpass sigma-delta modulator.

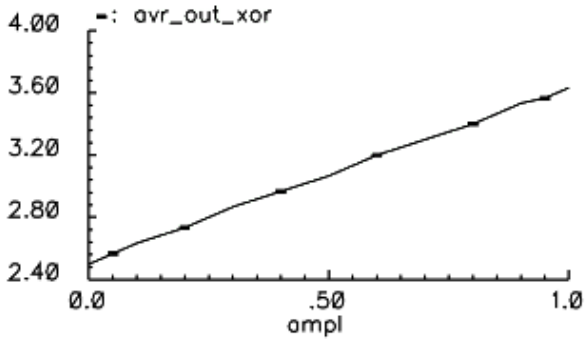


Fig. 8. Transfer characteristic of real bandpass sigma-delta modulator.

Consequently the output plots of the real bandpass sigma-delta modulator correspond with the ideal one, so the proposed first generation bandpass sigma-delta modulator for capacitive pressure sensing works correctly.

6. Chip Fabrication and Test Results

The layout of the modulator is shown in Fig. 9.

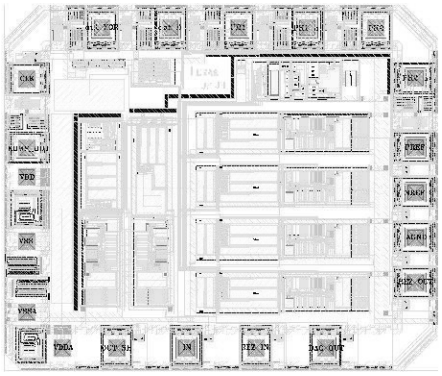


Fig. 9. Chip layout of bandpass sigma-delta modulator.

The central part of the die contains four delay stages, an input S/H circuit and an analog summing stage. The comparator is placed on the left side, the digital parts with flip-flops and non-overlapping driving clock generator are located on the upper part of the chip. The total area of the whole chip is 4.2 mm^2. The chip was fabricated in the frame of a EUROPRACTICE project in IMEC in Belgium.

The evaluation board was also fabricated as depicted in Fig. 10. The basic measurement function of the bandpass sigma-delta modulator (1) is driven via the microcontroller ATMEGA48 (2), which communicates with the PC. Some of the auxiliary signals, such as DAC output, driving clock etc., are measured using an external precise digital oscilloscope.

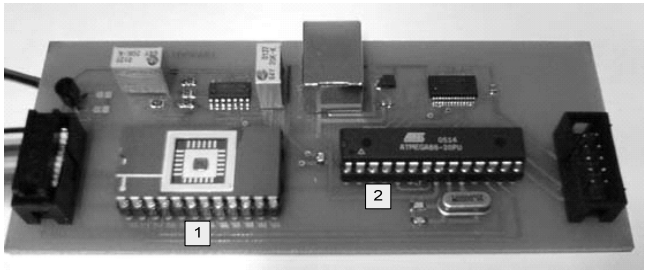


Fig. 10. Chip evaluation board.

Since the primary purpose of this work was verification of the proposed approach, the first basic tests were focused on the functionality of the chip itself. The results were processed and they confirm that the described principle works correctly.

Next figures describe the behavior of the complete bandpass sigma-delta modulator and some selected basic stages. The input signal was a sine wave with magnitude of 1 V and frequency of 25 kHz. Some unwanted effects that were specified above can be observed there. Fig. 11 shows the problem of clock feedthrough in the S/H stage.

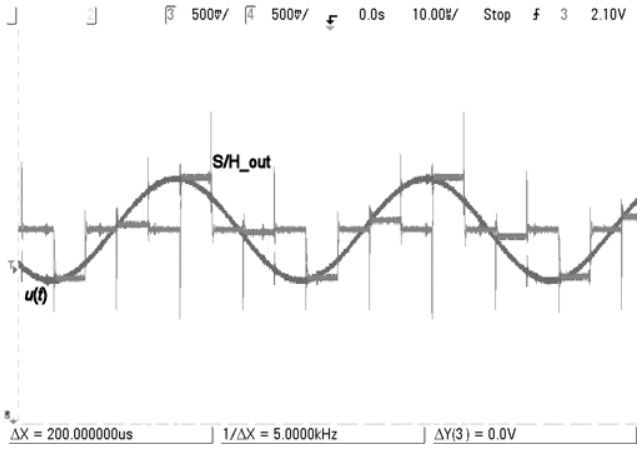


Fig. 11. Illustration of clock feedthrough problem in SC circuits.

The maximum positive peak value is 600 mV and the maximum negative peak value is -850 mV. Since these values are not sufficient, the error was withdrawn during redesign.

The functionality of the summator is depicted in Fig. 12 (bottom curve). This block works correctly in the comparison with calculations and the designed stage simulated in the CADENCE. There is also trouble with the SC tech-

nique – clock feedthrough (the maximum peak value is 20 mV) and it was suppressed in redesign as well.

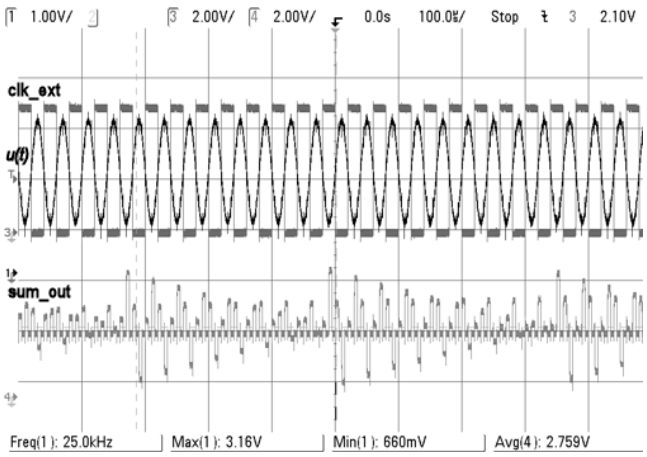
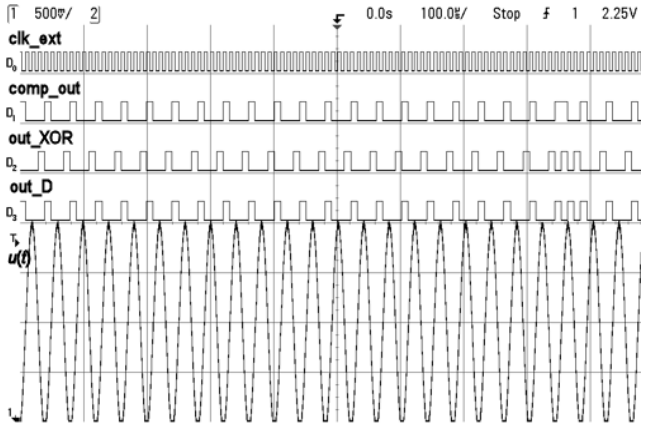
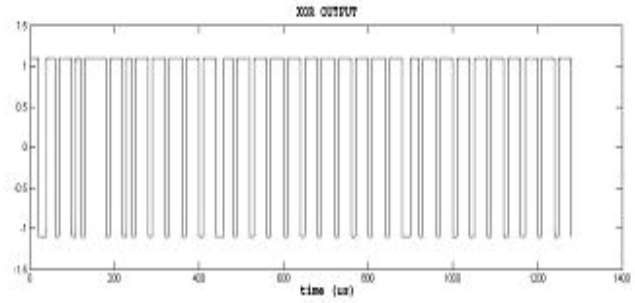


Fig. 12. Output signal of summator.

Fig. 13 and Fig. 14 confirm the utility of the complete chip. Fig. 13 a) and b) show the XOR output bitstream (signal D2) depending on the input sinewave signal with amplitude of 1 V in the real modulator compared to the output bitstream of the simulated modulator in MATLAB Simulink software.



a)



b)

Fig. 13. Output bitstream of XOR stage vs. input signal with 1 V magnitude in real a) and simulated modulator b).

Fig. 14 describes relation between modulator output and the input signal sweeped magnitude. This signal varies from 250 mV to 1 V.

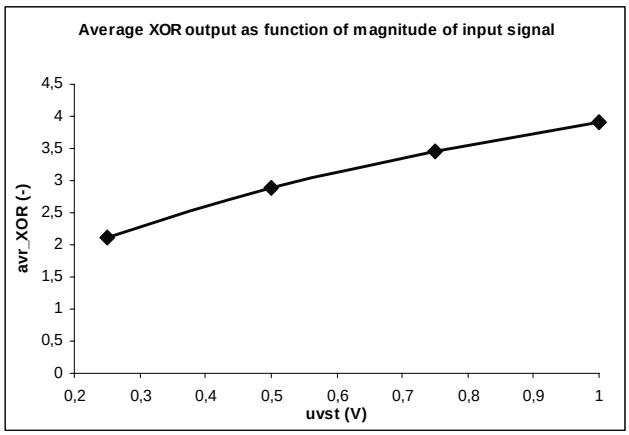


Fig. 14. Average output value of XOR stage vs. sweeped magnitude of input signal.

7. The Second Generation of Bandpass Sigma-delta Modulator

The redesign of the first version of bandpass sigma-delta modulator processed. There were several reasons for this procedure such as effects of the SC approach (mainly clock feedthrough), the high value of the basic loop offset, which led to the nonsufficient accuracy and resolution.

Advanced techniques were utilized to reach the requested parameters. The fully differential resonator correlated double sampling and dummy switches [13] were used to reduce clock feedthrough.

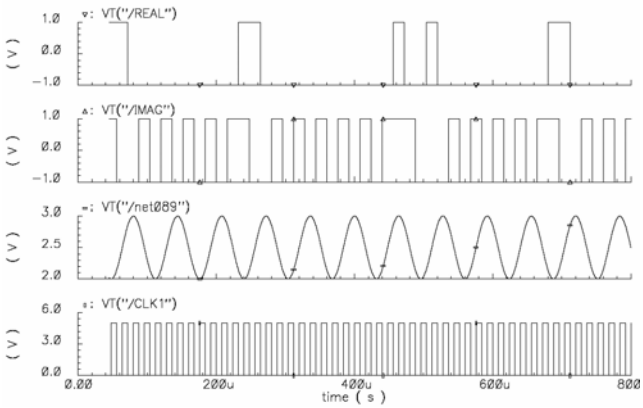


Fig. 15. Simulated output of second generation bandpass sigma-delta modulator.

The resonator output is a digital bitstream which is represented by the real and the imaginary component as shown in Fig. 15 and 16, where the simulated and the real measurement results are presented.

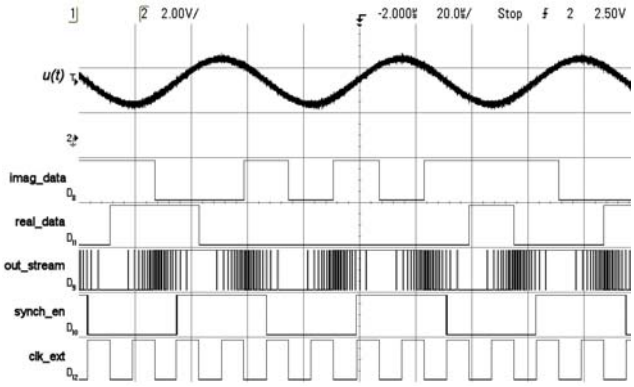


Fig. 15. Measured output of second generation bandpass sigma-delta modulator.

8. Conclusion

The bandpass sigma-delta modulators are well suited for wireless applications. This paper shows another way how to use its advantages. Authors designed the first and second order bandpass sigma-delta modulator as a preprocessing block for capacitive pressure sensing. The behavior of the ideal and the real modulator was verified and compared. The layout of the bandpass sigma-delta modulator was accomplished and the manufactured chip has been tested with the aim to compare the tested results with the simulation ones obtained from the design software environment.

The results confirm that the described principle works correctly. Moreover, the test results served for chip redesign targeted at the improvement of conversion accuracy and reduction of power consumption.

The redesign procedure was completed. First, the problem with SC technique (clock feedthrough, noise) utilizing fully-differential circuitries and advanced design approaches such as CDS have been dealt with. Then, the new version of PLL was designed. The first PLL presents the conventional approach and the second one uses the bandpass sigma-delta modulator as a generator of input harmonic signal.

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