Analysis and Design of Wideband Low Noise Amplifier with Digital Control

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Abstract. *The design issues in designing low noise amplifier (LNA) for Software-Defined-Radio (SDR) are reviewed. An inductor-less wideband low noise amplifier aiming at low frequency band (0.2-2 GHz) for Software-Defined-Radio is presented. Shunt-shunt LNA with active feedback is used as the first stage which is carefully optimized for low noise and wide band applications. A digitally controlled second stage is employed to provide an additional 12 dB gain control. A novel method is proposed to bypass the first stage without degrading the input matching. This LNA is fabricated in a standard 0.18 μm CMOS technology. The measurement result shows the proposed LNA has a gain range of 6 dB-18 dB at high gain mode and -12 dB to 0 dB at low gain mode, as well as a –3dB bandwidth of 2 GHz. The noise figure (NF) is 3.5-4.5 dB in the high gain setting mode. It consumes 20 mW from a 1.8 V supply.*

Keywords

Low noise amplifier, inductor-less, software-defined-radio, digital gain control.

1. Introduction

The wireless standards are growing rapidly in recent decade. Multi-mode multi-band wireless terminals that can reconfigure themselves in order to adapt to different wireless standards without the need of multiple terminals are highly desirable. Recently, a universal programmable software-defined-radio (SDR) approach for such terminals which provides a single hardware platform but can deal with different existing standards such as GSM, WCDMA, Bluetooth, WLAN, UWB, etc., is greatly in developing. The ideal implementation of a SDR receiver is shown in Fig. 1. This receiver can deal with different wireless channels appeared at the antenna simultaneously. The only analog/RF blocks are the reconfigurable antenna and the wideband Low Noise Amplifier (LNA). The 'super' ADC directly converts the RF signal into the digital domain and sent it to the digital baseband, where the down conversion and filtering are implemented. In such a way, the analog and mixed-signal circuit between RF and baseband can be

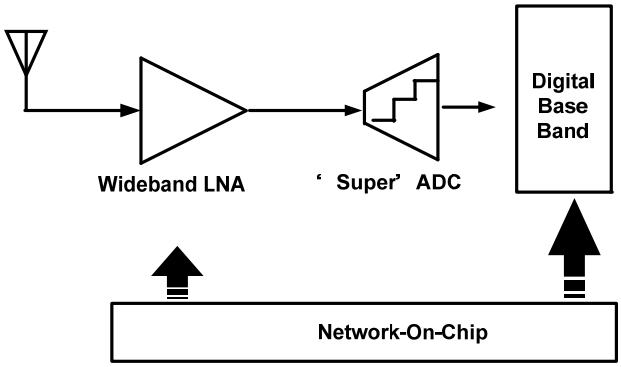

Fig. 1. The conceptual view of an ideal Software-Defined-Radio receiver.

eliminated. However, there exist severe problems in such kind of implementation. Firstly, the requirements of single antenna and single LNA to cover such a wide bandwidth will be difficult to meet. Secondly, the accuracy and sampling rate requirements make no suitable candidate to perform such conversion of RF signal directly into digital domain, considering the performance of existing ADCs. Even if so called 'super' ADC can be implemented, the power consumption will far exceed what a hand-hold terminal can endure. Thirdly, parallel DSPs have to be used in the digital baseband in order to perform real-time functions such as frequency conversion and filtering, which leads to high power consumption and dissipation. Therefore, analog signal processing is still necessary and is the only feasible way to implement Software-Defined-Radio with state-of-art semiconductor technology. With signal conditioning in the analog domain in the front-end of the receiver, the implementation of SDR can be done at a much lower speed, so that the critical requirements of both ADC and digital baseband can be released. Based on such a consideration, pioneer works have been demonstrated in recently literatures [1], [2], [3]. The prototypes are demonstrated as digitally enhanced flexible radios [1] or novel directly digital RF implementations [2], [3].

Among various transceiver architectures, direct conversion is the only suitable candidate which can be reconfigurable over a very broad frequency range, while reducing the power, cost and size at the same time. For other architectures, such as heterodyne and digital IF, the common IF suitable for all the different wireless standards is

almost impossible to be found. One conceptual implementation of such reconfigurable Software-Defined-Radio transceiver is shown in Fig. 2 (a). It composes of a direct conversion receiver, a transmitter and frequency synthesizer. Tunable filtering is provided at the antenna interface so that the blocking requirements for multi-band operation can be met. The sub-building blocks such as Low Noise Amplifier (LNA), Low Pass Filter (LPF), Variable Gain Amplifier (VGA) and Analog to Digital Converter (ADC) are all made tunable. In such a way, the RF carrier frequency, the channel bandwidth, the noise figure and the linearity can be reconfigured over a very wide range. Among all the sub-building blocks, the low noise amplifier (LNA) always plays a critical role in the receiver of such a system.

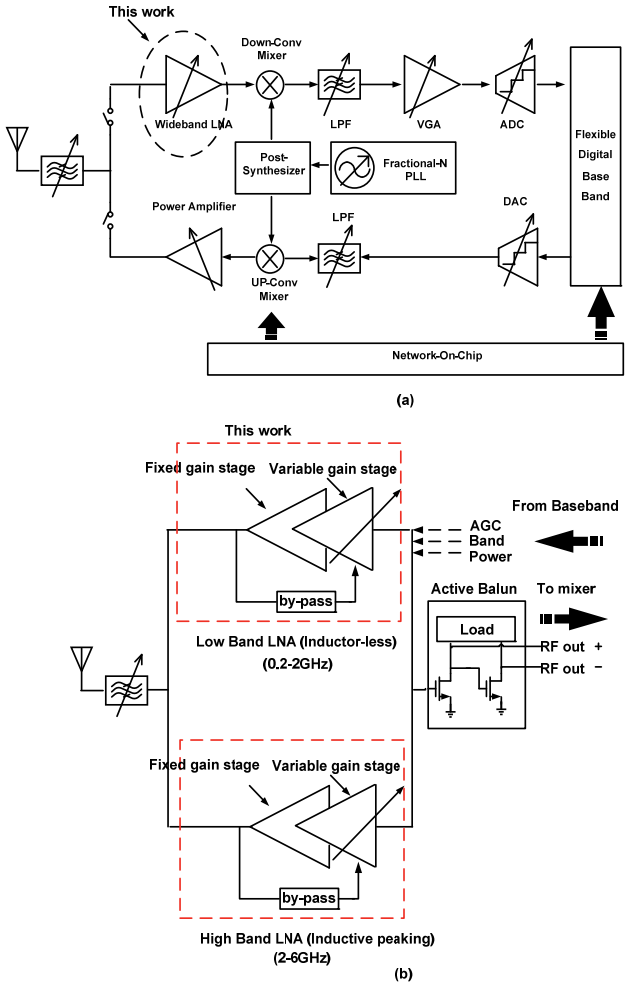

Fig. 2. **(a)**The conceptual view of a zero-IF SDR transceiver. **(b)** The dual LNA flexible receiver front-end architecture for Software-Defined-Radio applications.

The requirements of a wideband, digital controlled, low noise, high linearity and low power consumption make the design of the LNA for SDR receiver very challenging. One traditional and simple implementation is to put several narrow band LNAs in a multi-standard receiver in parallel, which introduces higher power consumption and larger silicon area [4]. A more popular solution is to design a single ultra wideband LNA which covers the whole operating range. Such implementation can save power and chip area greatly. Unfortunately, it suffers from inflexibility of tuning through digital ways. In addition, it is sensible to parasitic components due to the ultra wideband working band. Hence it lacks of robustness in real implementation. Recently, some interesting implementations focusing on low power design [5] and gain control [6] provide new concepts on the design of LNA for SDR.

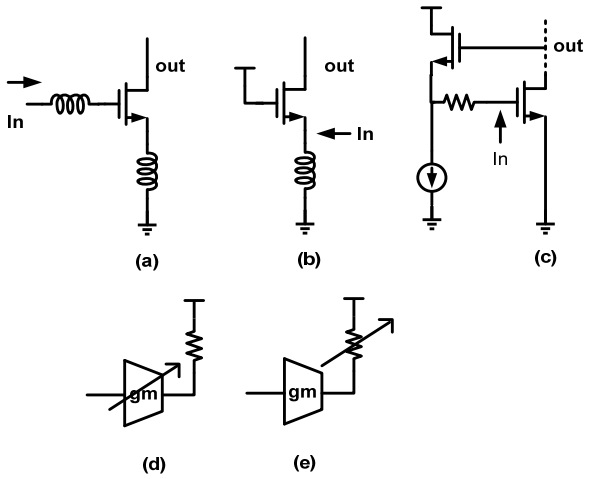

Fig. 3. **(a)** Inductive-degenerated common source stage. **(b)** Common gate stage. **(c)** Active feedback stage. **(d)** Varying the gain through tuning g_m. **(e)** Varying the gain through tuning load.

Trade-offs can be made between these two kinds of extremes, which is shown in Fig. 2 (b). Two single-ended LNAs designed for low frequency band (0.2-2 GHz) and high frequency band (2-6 GHz) are placed in parallel to cover the whole 0.2-6 GHz range. Their outputs are connected to an on-chip active balun in order to convert the single-ended signal into differential type to drive the following double balanced mixer. In addition, the LNA's gain and power consumption are tunable by the digital signals from baseband so that the whole receiver system can adjust its operating conditions.

For wideband LNA design, input matching and low noise figure are the two most critical considerations. Three most frequently used input stage topologies are listed in Fig. 3 (a)-(c). Fig. 3(a) represents inductive-degenerated common source stage, which is widely used in traditional narrow band LNA design. Due to the relatively high quality factor of its input network, a wideband matching can't be achieved without complex LC filters [7]. Fig. 3 (b) is a simple common gate input stage with one inductor serving both as DC current sink and parallel resonant tank for input matching. Wideband input matching can be obtained without extra components since the quality factor of the input parallel resonant tank is relatively low. One drawback of such topology is that the noise figure of the stage is tied with the input impedance g_m^{-1} so that the NF of the LNA is bound to be higher than 3 dB. This limitation can be alleviated by advanced circuit techniques such as

g_m-boosting [8], [9] and noise canceling [10], [11]. However, this topology is not the best choice for low frequency band LNA, since the value of the inductor is too large to be implemented on-chip when the lowest frequency band can be as low as 200 MHz. Fig. 3(c) adopts shunt-shunt active feedback to implement wideband impedance matching. Since no explicit limitation of noise performance is bounded to this topology and no inductor is needed for matching, this topology is suitable for the implementation of low band (0.2-2 GHz) Software-Defined Radio receiver LNA.

Gain control scheme is another consideration in software defined radio applications. The gain of the LNA can be varied either by tuning the g_m stage or the load resistance as shown in Fig. 3 (d)-(e). Unlike its bipolar counterpart, the MOS transistor cannot achieve precisely linear-in-dB gain control simply through tuning the voltage between its gate and source (V_{gs}). In addition, since the input matching highly depends on the loop gain of the feedback, varying the gain of the amplifier may degrade the S_{11} (input matching). Proper gain control scheme that is able to deal with these issues is therefore highly desired.

This paper presents the design of a wideband inductor-less LNA with digital gain control. Section 2 describes the circuit structure and design considerations of the proposed LNA. Section 3 presents the measurements of the proposed circuit. The conclusion of the paper is given in Section 4.

2. Circuit Implementation

The proposed LNA is shown in Fig. 4.It is composed of a shunt-shunt feedback amplifier as fixed gain first stage and common source amplifier as a digital tuned variable gain reconfigurable second stage. M_1 and M_2 are the input stage transistors. M_2 is configured as current-bleeding branch in order to alleviate the voltage headroom problem of R_1 and also reuse the current for larger input g_m. Compared with the topology where the drain of M_2 is connected with the output node of the first stage in [12], the proposed circuit has a better bandwidth and gain performance. Firstly, the parasitic capacitance introduced by M_2 is placed at M_3'source node instead of its drain node. The latter node has low impedance so that it can tolerate more parasitic capacitance for the required bandwidth compared with the former one, which is a high impedance node. In addition, the g_m of M_2 is adopted as an extra part of the input stage so that the total gain of the first stage is enhanced without extra power consumption. M_3 is the cascode stage for better isolation of the input and output signals. M_4 works as the active feedback component for input impedance matching together with feedback resistor R_f. M_5 provides current source which biasing M_4. C_1, C_2 and C_3 are DC blocking capacitors. As analyzed before, variable gain cannot be implemented in the feedback amplifier without affecting its input matching. Thus a digital gain tuning scheme combines switched resistors tank R_2~R_5 and a current-steering branch M_8 is proposed and adopted in the second stage, which is composed of M_6 and M_7 as basic common source amplifier configuration. In order to maintain the linearity when the input signal is very strong, a novel by-pass scheme is proposed to shut down the first stage and reconfigures the second stage. The input signal is directly conveyed to the second stage through switch transistor M_{11}. This control signal also shut down the first stage by pulling the bias transistor M_9 for input stage to ground through M_{10}.

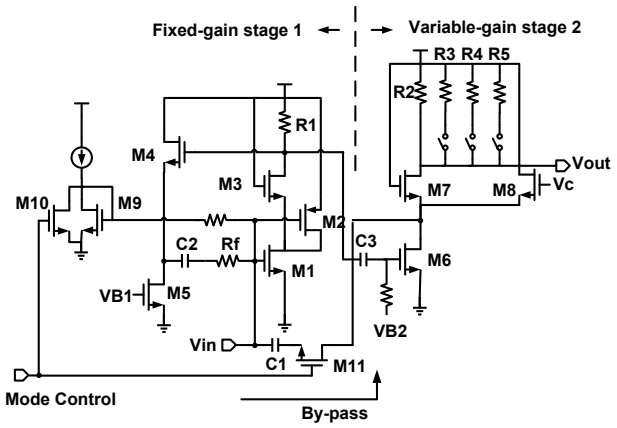

Fig. 4. Schematic of the proposed two stages Low Noise Amplifier.

2.1 Input Matching

As the LNA is designed for two modes as high gain and low gain (by-pass), the input matching requirements should be met under both the two conditions.

When working in the high gain mode, according to [13] and shown in Fig. 5 (a), the input impedance of an amplifier in shunt-shunt feedback configuration is

$$Z_{in\_closed} = \frac{Z_{in\_open}}{1+A_v} \tag{1}$$

where Z_{in_open} and Z_{in_closed} are the open and closed loop input impedance of the amplifier respectively. A_v represents the loop gain. In the proposed first stage

$$\begin{aligned} Z_{in\_open} &= R_f + 1/g_{m4}, \\ A_v &= (g_{m1}+g_{m2})R_1 \end{aligned} \tag{2}$$

where g_{mi} represents the transconductance of transistor M_i. For input matching, the closed loop input impedance should be equal to the source impedance R_s, which leads to

$$R_s = \frac{R_f + 1/g_{m4}}{1+(g_{m1}+g_{m2})}. \tag{3}$$

For a pre-determined open loop gain A_v, a proper choice of R_f and $1/g_{m4}$ should consider not only (3), but also noise and linearity performance, which will be analyzed in the following section.

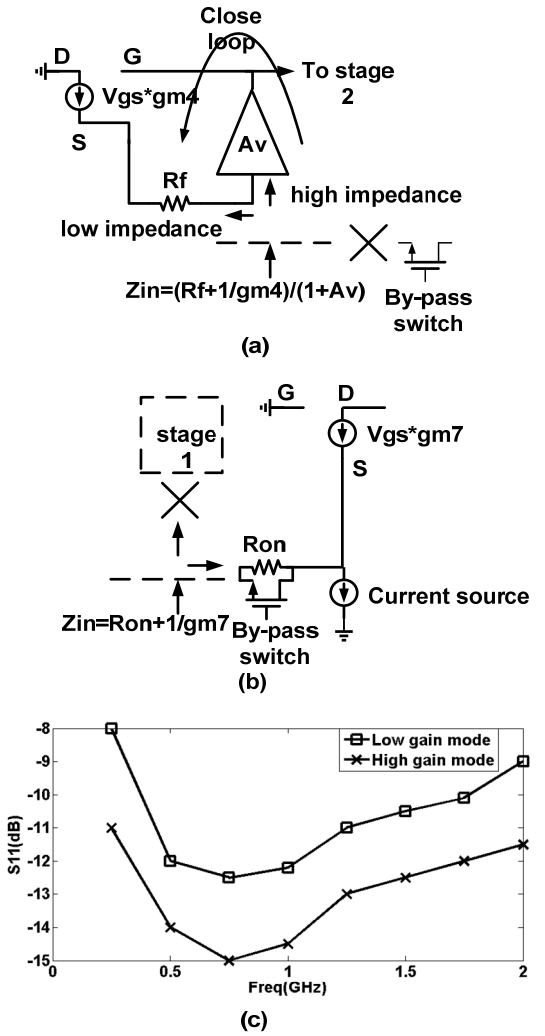

Fig. 5. **(a)** The input impedance at high gain mode. **(b)** The input impedance at low gain mode (when the first stage is by-passed). **(c)** Simulated S11 performance at high gain and low gain mode separately.

When the first shunt-shunt amplifier is by-passed and the input signal is sent directly to the second stage, the input matching is still required to remain at an acceptable level so that a proper SNR of the whole system can be attained. However, many of the by-pass schemes in previous publications directly connect the input signal to the gate of the common source amplifier M_6, of which the input matching is ruined. A novel by-pass scheme is proposed here which remains the S_{11} performance by reconfiguring the second stage. As shown in Fig. 6(a)-(b), when the first stage is at work, its output signal is sent to the gate of M_6. In this way, the second stage works as a common gate amplifier, and M_7 works as a cascode current buffer. When the first stage is shut down, M_6's gate node becomes AC ground. Now the switch transistor M_{11} turns on and conveys the input signal directly to the drain of M_6. Since C_1 blocks the dc current of M_{11}, this transistor works in deep triode region and can be regarded as a linear resistor. In this way, the second stage is reconfigured as a common gate amplifier, of which M_6 works as the biasing current source and M_7 works no long as a cascode stage but as the common gate amplification stage. The input impedance shown in Fig. 5 (b) now becomes

$$Z_{in} = \frac{1}{\mu_n C_{ox}(W/L)_{11}(V_{DD} - V_{in})} + 1/g_{m7}. \quad (4)$$

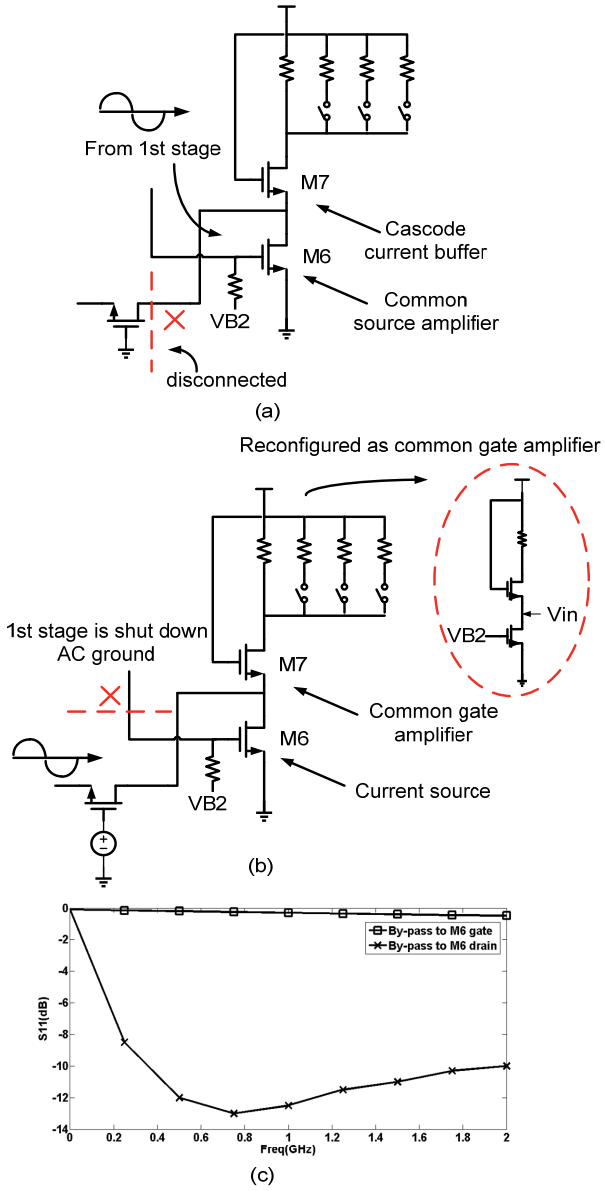

Fig. 6. **(a)** The 2nd stage works as common source amplifier when the 1st stage is at work. **(b)** The 2nd stage is reconfigured as common gate amplifier when the 1st stage is shut down.

As shown in Fig. 5 (c), through careful choice of W/L of M_{11} and g_m of M_7, a satisfied S_{11} performance can still be met when the first stage is by-passed. The S_{11} performances of by-passing the input signal to M_6's gate and drain are also given out in Fig. 6(c) respectively. While the gate node of M_6 provides very poor input matching and reflects input signal severely, the low impedance source node of M_6 provides wideband input impedance matching, which leads to satisfactory circuit performance and thus highly flexibility of the LNA.

2.2 Noise and Linearity

Noise performance is among the most critical requirements in LNA design. According to Friis equation, the total noise factor of the two stages LNA can be expressed as

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{A_v}. \tag{5}$$

From (5), it is obvious that the first stage of the LNA contributes much more than the second stage to the total NF if the output noises of the two stages are comparable. So the following noise analyses only consider noise of the first stage for simplicity.

The noise factor of the proposed LNA can be expressed as

$$F = F_{Rs} + F_{M_1+M_2} + F_{R_f} + F_{M_4} + F_{M_5}. \tag{6}$$

Thus the noise figure can be simplified as

$$\begin{aligned} F \approx & 1 + \frac{\gamma}{(g_{m1}+g_{m2})R_s} + \frac{R_f}{(1+A_v)^2 R_s} \\ & + \frac{\gamma}{1+A_v}\left(1 - \frac{R_f}{R_s(1+A_v)}\right) + \frac{1}{(g_{m1}+g_{m2})R_s A_v} \\ & + \gamma g_{m5} R_s \left(1 - \frac{R_f}{R_s(1+A_v)}\right)^2 \end{aligned} \tag{7}$$

where γ is defined as the thermal noise factor of MOS transistors. It can be concluded from (7) that increasing the loop gain A_v can improve the noise figure performance. However, increasing the gain of the input stage means additional biasing current, supposing a constant transistor overdrive voltage. Due to the limited voltage headroom in deep submicron CMOS technologies, large input stage current will cause severe voltage headroom problems on R_1. This problem can be alleviated by the proposed current bleeding and reused technique through M_2. Even though, the large size of the input transistor M_1 & M_2 will introduce large parasitic capacitance, so that ruins the input matching performance at high frequency. In addition, according to (2), A_v should be varied simultaneously with R_f and $1/g_{m4}$ in order to keep the input matching performance

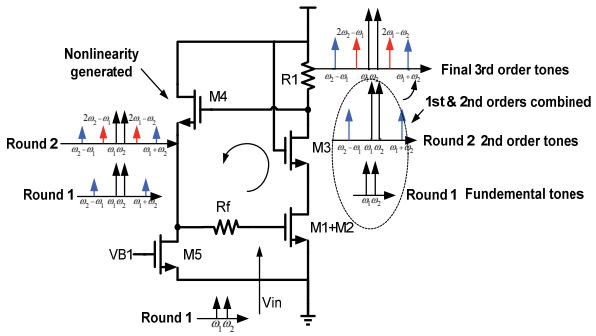

Fig. 7. The scheme how the severe third order nonlinear distortion is generated through the active feedback loop.

constant, which means the noise performance should be traded off with other circuit performances such as linearity and matching.

The linearity is another important design specification especially for wideband LNAs, since the self-modulation and cross-modulation problems prone to be more severe when no filtering through high quality factor LC tank is performed, compared with their narrowband counterparts.

According to Friis equation again, the IIP3 of the two stages LNA can be expressed as

$$\frac{1}{A^2_{IP3}} = \frac{1}{A^2_{IP3,1}}, + \frac{A^2_v}{A^2_{IP3,2}}. \tag{8}$$

It can be concluded from (8) that the nonlinearity of the second stage is more critical to the whole system compared with the first stage, supposing $A^2_{IP3,1} \approx A^2_{IP3,2}$. However, in the proposed LNA, the second stage is a common gate amplifier, the high linearity of which can be achieved by setting the overdrive voltage (V_{GS6}-V_{th6}) of M_6 high enough. On the contrary, the 2nd order distortion generated by the nonlinearity of the active feedback component M_4 is mixed and amplified with the fundamental tone in M_1 & M_2, and appears as severe 3rd order distortion at the output node, as shown in Fig. 7. Under such circumstance, the first part of (8) is comparable with the second part, indicating that the linearity performance of the first stage shunt-shunt feedback amplifier should be treated with equal importance as the second stage. Since the linearity performance of the second stage can be improved simply by increase the overdrive voltage of input transistor M_6 as mentioned before, our analysis will focus on the linearity performance of the first stage.

According to the detailed analysis given out in [12], the IIP3 of a shunt-shunt feedback amplifier can be calculated using Volterra Series, and the simplified expression can be given as

$$IIP_3 \approx \frac{1}{\left|K_{2g_{m4}}\right|} \frac{4\sqrt{2/3}(1+A_v)}{\sqrt{\left|(1+A_v+R_f/R_s)(1+A_v-R_f/R_s)\right|}} \tag{9}$$

where K_{2gm4} is the curvature of g_{m4} as:

$$K_{2g_{m4}} = \frac{1}{2}\frac{\partial^2 i_{DS}}{\partial v^2_{GS}}. \tag{10}$$

It can be concluded from (9) that the linearity of the active feedback LNA can be improved through increasing the overdrive voltage (V_{GS4}-V_{th4}) of M_4, increasing A_v and increasing R_f. M_4's overdrive voltage is limited by the voltage drop across R_1, and A_v should be pre-determined by system requirements. Thus the only parameter that can be effectively varied is R_f. Reconsider (3) and (7), the choice of R_f also affects the input matching and noise performances. To verify the impact of R_f on various aspects of the proposed circuit's performance, we vary the R_f among a set of reasonable values with a fixed A_v, and make g_{m4} change in a proper way so that a constant input matching perform-

ance can be maintained by (3). The noise figure and *IIP*3 of the shunt-shunt feedback LNA are checked through simulation and plotted in Fig. 8.

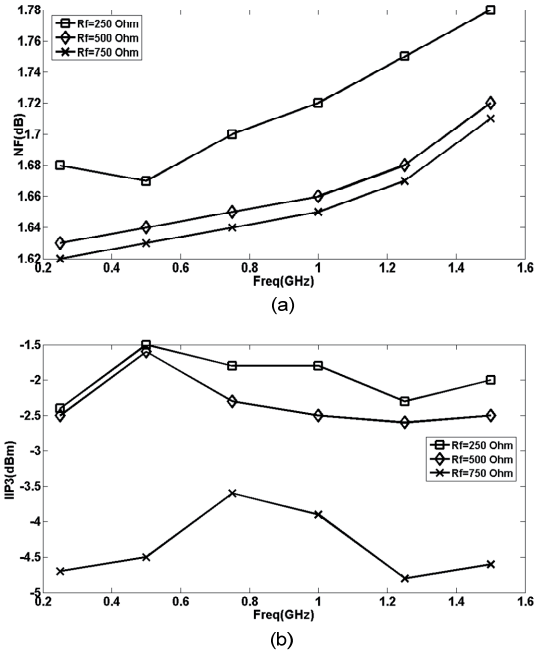

Fig. 8. The simulated noise figure and IIP3 performance of the active feedback amplifier when R_f is chosen as 250 Ohm, 500 Ohm and 750 Ohm.

Combining the simulation results in Fig. 8 together with (7) and (9), it can be concluded that increase R_f can increase the linearity of the amplifier and lower its noise figure simultaneously. When R_f is increased, the decrease of the noise from M_4 and M_5 surpasses the increase of the noise from R_f, so the total noise figure is reduced. However, the value of R_f cannot be arbitrarily large since the requirement of g_{m4} being positive bounds the upper limit of R_f's value as

$$R_f \le (1 + A_v)R_s . \tag{11}$$

In the design of the proposed circuit, R_f has been chosen by trading-off carefully among noise, gain and linearity performances.

2.3 Gain Variation

As mentioned before, gain variation should be provided by the LNA for Software-Defined-Radio applications in order to remain the linearity performance of the whole system when the input signal is very strong. Though the gain of the receiver system can be further adjusted in the following variable gain amplifier (VGA) in the analog baseband, to provide gain variation early in the receiver signal chain brings more flexibility to the whole system, which is very important for flexible digital intensive transceiver implementations.

There are two basic methods of tuning the gain of an amplifier, one of which is to tuning the g_m of the amplifier; the other is to tuning the load. For bipolar transistors, due to their exponential relationship between input voltage and g_m, linear-in-dB control [14], [15] can be easily implemented. Unfortunately, for CMOS transistors, g_m is linear with the input voltage. Precise linear-in-dB control can only be achieved by additional voltage generation blocks [16], which are largely increasing the complexity of the LNA. One simple method for CMOS implementations is to steer the output current from the g_m stage to a virtual ground, so that the effective g_m is reduced. However, since the gain variation is based on the W/L ratio of the g_m stage transistor and the current steering transistor, a fine gain control resolution cannot be easily achieved.

This problem can be solved by combining current-steering method together with load variation. As shown in Fig. 9(a), (b), there are two ways to construct a variable resistor, one of which is to use switches to connect the output node with different segments in a series resistor ladder [17], the other one is to switch in (or out) paralleled resistors. Since the switches are implemented as transistors, they introduce parasitic capacitance, which are represented as C_1-C_4 in Fig. 9 (a), (b).

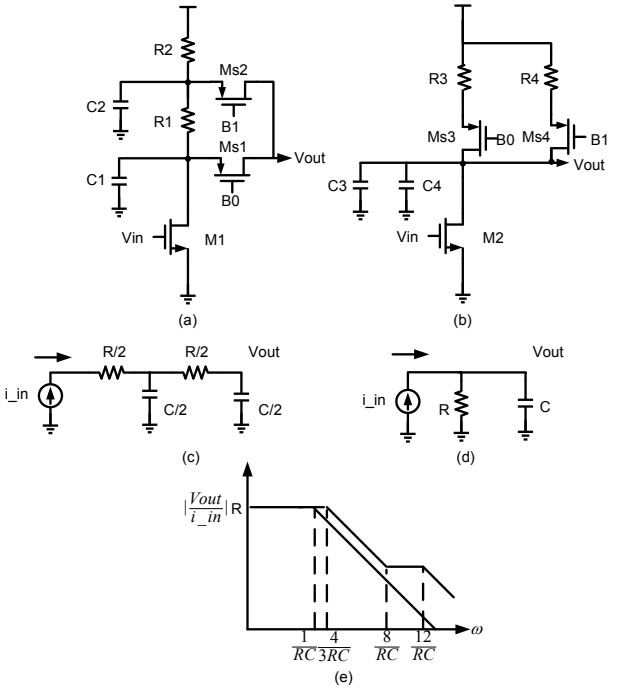

Fig. 9. **(a)**Variable resistors bank in series configuration. **(b)**Variable resistors bank in parallel configuration. **(c)** Small signal model of '(a)'. **(d)** Small signal model of '(b)'. **(e)** Bode plot of the transfer function from output current of the g_m stage to output voltage.

In order to fairly compare the frequency response of the two topologies when parasitic capacitance is introduced, the digital control signals of the two topologies are set as B0B1='01' for (a) and B0B1='01'for (b) respectively, so that both of them have the same low frequency gain value. For simplicity, suppose $R_1 = R_2 = R/2$, $R_3 = R_4 = R$, $C_1 = C_2 = C_3 = C_4 = C/2$. In such a way, the variation ranges of the two topologies are therefore the same. The small

signal models of the two topologies are shown in Fig. 9 (c), (d). The transfer function of output voltage to the output current from g_m stage can thus be derived as

$$\left|\frac{V_{out}}{i\_in}\right|_a = R\frac{\frac{RC}{8}s+1}{\frac{(RC)^2}{16}s^2+\frac{3}{4}RCs+1}, \quad (12)$$

$$\left|\frac{V_{out}}{i\_in}\right|_b = R\frac{1}{1+RCs}. \quad (13)$$

It can be concluded that there are two real poles and one zero in (12) and a single pole in (13) as

$$p_{1a}=\frac{4}{3RC}, p_{2a}=\frac{12}{RC}, z_{1a}=\frac{8}{RC}, \quad (14)$$

$$p_{1b}=\frac{1}{RC}. \quad (15)$$

The Bode plot of (12) and (13) is shown in Fig. 9 (e). It can be concluded that since the second pole and zero of topology (a) is far away from its first pole, their impacts are minor enough at the frequency band of interest, which is within the first pole. The 1st pole of topology (a) and (b) is very nearby with each other, so that a similar frequency response at the interested frequency band can be expected.

However, supposing a constant DC biasing current I for the g_m stage, the resistor tank DC power consumption of the two topologies are

$$P_a = I^2 R_{total}, P_b = I^2 R_{varied} \quad (16)$$

where R_{total} dedicates that the DC biasing current always flows through the whole series resistor ladder no matter which segment is switched out. From this point of view, topology (a) is not power efficient especially when low gain is chosen. On the contrary, for topology (b), the number of resistors consuming DC power varies in the same trend as the gain of the amplifier. When low gain is selected, R_{varied} decreases so that a lower DC power consumption can be achieved.

Fig. 10 plots the power consumption of the two types of variable resistors under different output gain values, supposing same amount of current flowing into each resistor bank. The power consumption has been scaled by its highest value, which is achieved when the variable resistors are tuned to their largest values. As predicted by (16), while the power consumption of the series topology remains unchanged all the time, the power consumption of the parallel topology decreases as the gain decreases. A maximum of 50% power can be saved by the parallel topology compared with its series counterpart when working at their lowest gain setting.

Therefore, topology (b) is adopted as variable resistor load. Together with the proposed by-pass first stage scheme and current-steering technique, a large tuning range with fine digital tuning step can be achieved as well.

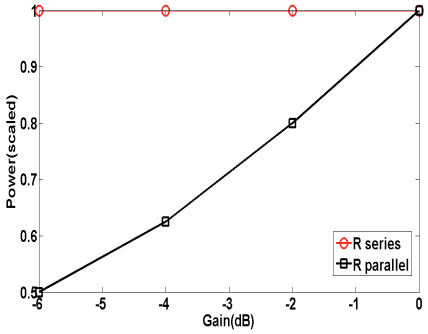

Fig. 10. Power consumption of the variable resistor tanks in series and parallel configurations.

As shown in Fig. 11, the by-pass scheme gives an attenuation of the LNA's gain by A_v, which is the gain of the first stage and equals to about 18 dB. The second stage combines current-steering as coarse tuning and variable resistor as fine tuning. As shown in Fig. 4, M_8 functions as the steering transistor and owns the same W/L ratio as M_7. When Vc='1', half of the output current from g_m stage is conducted to VDD, so that the gain is halved, (or decreased by 6 dB). The switch resistor tank consists of R_2-R_5 that provides 3 steps fine gain control with 2 dB each step. The second stage thus provides a continuous 12 dB variable gain with 2 dB gain precision when controlled by 4bits digital signals. In this way, the two stages LNA can provide a variable gain of 6 dB-18 dB in high gain mode and -12 dB to 0 dB in low gain mode with 2 dB fine step.

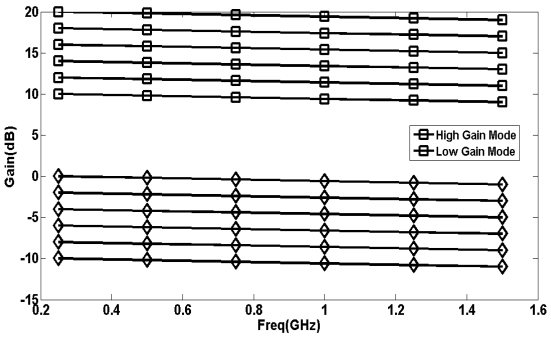

Fig. 11. 4 digital bits controlled variable gain of the proposed LNA: 6 dB-18 dB in high gain mode; -12 dB-0 dB in low gain mode. The by-pass, coarse and fine tuning steps are 18 dB, 6 dB and 2 dB separately.

3. Experimental Results

The proposed inductor-less wideband LNA with digital controllable gain is fabricated in a standard 0.18 μm CMOS technology. The chip photograph is shown in Fig. 12. Differential pair style open drain buffer is integrated on chip to deliver the output signal to the measurement equipments without severe gain loss and noise performance degeneration. On-wafer measurement is performed to characterize the proposed LNA.

The measured scattering (S) parameters are plotted in Fig. 13 and Fig. 14. Since the low band (0.2-2 GHz) of Software-Defined-Radio includes many of the mobile TV

tuner standards such as DVB-H (470-860 MHz, 1670 to 1675 MHz), MediaFLO (712-722 MHz), etc., the proposed LNA is initially designed for 75 Ohm characteristic impedance, which is widely adopted in tuner system. However, the measurement equipment can only offer 50 Ohm source and load impedance, which leads to a degeneration of the circuit's performance in measurement. In the high gain mode, the S_{11} of the proposed LNA remains below -10 dB until 1.3 GHz, while raises to -6 dB at 2 GHz. The gain of the LNA has a -3dB bandwidth of 2 GHz and a highest achievable value of 18 dB, which is 2 dB lower than the post-layout simulation result. The gain is varied during testing through digital controlled bits and a pre-defined coarse tuning of almost 6 dB and fine tuning step of 2 dB can be achieved. In the low gain mode, the S_{11} remains below -5 dB in 0.2-2 GHz working band. The gain has a similar -3dB bandwidth of about 2 GHz, as compared to the high gain mode, and exhibits highest gain of 0 dB.

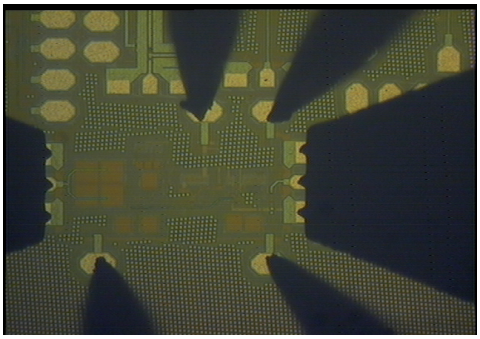

Fig. 12. Chip photograph of the proposed LNA.

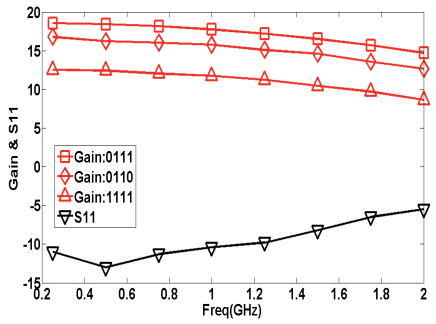

Fig. 13. The measured S_{11} and gain performance of the proposed LNA in high gain mode.

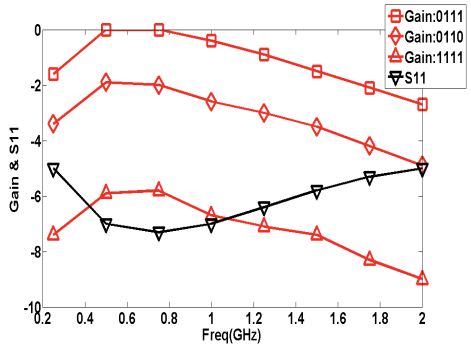

Fig. 14. The measured S_{11} and gain performance of the proposed LNA in low gain mode.

Due to partly degradation of S_{11} performance caused by the 50 Ohm to 75 Ohm conversion problem during testing, the tested noise figure performance is 1.5 dB higher than the post-layout simulation result in average. It maintains between 3.5-4.5 dB in the 0.2-2 GHz frequency band in high gain mode, as shown in Fig. 15.

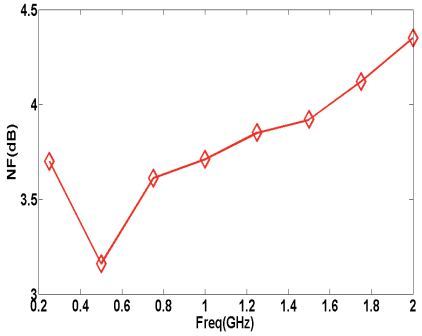

Fig. 15. The measured noise figure performance of the proposed LNA in high gain mode.

The post-layout simulated IIP3 of the proposed LNA is -7 dB excluding the open drain buffer. The testing of the linearity has not been performed and not reported here due to the limitation of our testing equipments.

The proposed LNA consumes 20 mW from 1.8V supply excluding the power of the output buffer. Due to its inductor-less characteristic, the circuit is area-efficient and takes up a silicon-area of 600 μm × 300 μm including the on chip buffer and testing pads.

4. Conclusion

An inductor-less wideband LNA with digital controlled gain for low band (0.2-2 GHz) Software-Defined-Radio applications has been presented. The first stage of the LNA utilizes active feedback for wideband input impedance matching and low noise figure. Current-reuse technique is adopted to alleviate the limited voltage headroom problem and also enhance the gain of the first stage. A combined digital controlled gain tuning scheme is proposed using a novel by-pass scheme, current-steering coarse tuning and variable resistor fine tuning techniques. In this way, a large and precise variable gain range of 6 dB-18 dB and -12 dB-0 dB can be achieved without degrading the input impedance matching performance. The reconfigurable second stage provides much flexibility when the LNA works at different modes. The proposed LNA achieves a -3dB bandwidth of 2 GHz and a noise figure of 3.5-4.5 dB when the highest gain is set.

Acknowledgements

This work is supported by the Fundamental Research Funds for the Central Universities, Program No. 2009QNA4015.

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