New Squarer Circuits and a Current-Mode Full-Wave Rectifier Topology Suitable for Integration

Shahram MINAEI [1], *Erkan YUCE* [2]

[1] Dept. of Electronics and Communications Engineering, Dogus University, Acibadem, 34722 Kadikoy, Istanbul, Turkey
[2] Dept. of Electrical and Electronics Engineering, Pamukkale University, 20 017 Kinikli-Denizli, Turkey

sminaei@dogus.edu.tr, erkanyuce@yahoo.com

Abstract. *In this paper, three squarer configurations and a current-mode (CM) full-wave rectifier circuit are suggested. The first and second squarer configurations respectively use two PMOS and two NMOS transistors while the third one employs three PMOS and one NMOS transistors. A CM full-wave rectifier with high output impedance current is developed. All of the proposed circuits provide several advantages such as low number of components and less power consumption. The proposed circuits are simulated using SPICE program to demonstrate their performance and workability.*

Keywords

CMOS, squarer circuit, rectifier, current-mode.

1. Introduction

MOS-based analog squarer circuits may have voltage inputs and current outputs, and find wide application areas such as neural and image processing [1]. Recently, a squarer topology using a number of CMOS transistors has been reported [2]. Apart from these, it is well-known that a current-mode (CM) approach offers certain potential advantages such as higher usable gain, greater linearity, lower power consumption, wider bandwidth, lower number of components and larger dynamic range when compared to its voltage-mode (VM) counterpart [3]-[5]. CM and VM full-wave rectifiers are widely used in analog signal processing, analog communication systems, conditioning and instrumentation of low-level analog signals as well as dc converters. However, only a few CM rectifiers were previously published in the open literature [6]-[10].

In this paper, three new circuits for providing squared analog output currents are proposed. All of the introduced squarer structures are simple, and dissipate less power when compared to that of [2] because of the fact that two of the proposed squarer circuits use only two MOS transistors while the other one employs four MOS transistors. Further, all of the squarer circuits operate in class B. A full-wave rectifier circuit employing only six MOS transistors dissipating less power is also introduced. Contrary to the CMOS-based CM rectifiers given in [7]-[10], the developed CM rectifier can provide gain at output current. However, all the developed circuits need bias voltages which can be obtained by bias voltage generators.

The rest of the paper is organized as follows. The proposed squarer circuits are presented in Section 2. A simple CMOS-based CM full-wave rectifier is given in Section 3. The simulation results of the introduced circuits based on SPICE program are given in Section 4 and finally some concluding remarks are drawn in Section 5.

2. Proposed Squarer Circuits

The drain current of a long-channel PMOS/NMOS transistor operating in saturation region can be respectively given by the square-law relation as:

$$I_D = \frac{1}{2} k_p (V_{SG} - |V_{TP}|)^2, \tag{1}$$

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{TN})^2 \tag{2}$$

where $k_p = \mu_p C_{ox}(W/L)$ and $k_n = \mu_n C_{ox}(W/L)$, μ_p and μ_n are respectively surface mobilities of PMOS and NMOS transistors, C_{ox} is the gate capacitance per unit area, and W/L is the aspect ratio (channel width/channel length) of the transistor [11]. The threshold voltages V_{TP} and V_{TN} are respectively expressed as

$$V_{TP} = V_{TP0} + \gamma_p \left(\sqrt{2\phi_{Fn} + V_{BS}} - \sqrt{2\phi_{Fn}} \right), \tag{3.a}$$

$$V_{TN} = V_{TN0} + \gamma_n \left(\sqrt{|2\phi_{Fp}| + V_{SB}} - \sqrt{|2\phi_{Fp}|} \right) \tag{3.b}$$

where V_{TP0} (V_{TN0}) is the threshold voltage with V_{SB}=0 (V_{BS}=0), $2\phi_{Fn}$ ($2\phi_{Fp}$) is the bulk surface potential and γ_p (γ_n) is the body-effect coefficient of the PMOS (NMOS) transistor. Note that $2\phi_{Fn}$ and γ_n are positive while $2\phi_{Fp}$ and γ_p are negative.

The introduced squarer circuits with two PMOS/NMOS transistors are shown in Figs. 1 and 2, respectively. If the input voltage signal in Fig. 1 is in

positive cycle, M_1 is OFF while M_2 operates in saturation region. Here $\pm V_{TP}$ are the dc bias voltages. Likewise, if the input is in negative cycle, M_2 is OFF and M_1 operates in saturation region. For the circuit of Fig. 2 which is biased with $\pm V_{TN}$ voltages, if the input voltage signal is in positive cycle, M_3 is OFF while M_4 operates in saturation region. Similarly, if the input signal is in negative cycle, M_4 is OFF and M_3 operates in saturation region.

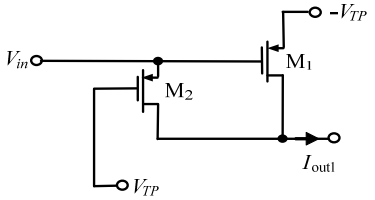

Fig. 1. The proposed PMOS-based squarer circuit.

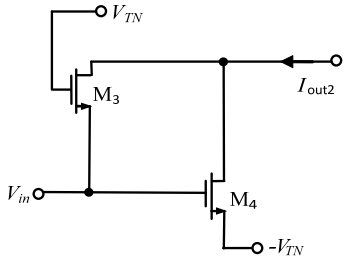

Fig. 2. The proposed NMOS-based squarer circuit.

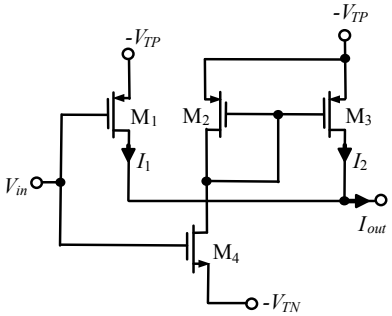

Fig. 3. The proposed CMOS squarer circuit.

The output of the PMOS squarer of Fig. 1 and NMOS squarer of Fig. 2 can be normally connected to, respectively, NMOS and PMOS current mirrors, or can be grounded. Assuming MOS square-law characteristic for the MOS transistors, the output currents of the squarer topologies given in Figs. 1 and 2 can be respectively evaluated as

$$I_{\text{out1}} = \frac{1}{2} k_p V_{in}^2 \,, \tag{4}$$

$$I_{\text{out2}} = \frac{1}{2} k_n V_{in}^2 \,. \tag{5}$$

Here $k_{p1} = k_{p2} = k_p$ and $k_{n3} = k_{n4} = k_n$. Another squarer configuration is given in Fig. 3, which has high input and output impedances resulting easy cascadability with other circuits. The output current of the squarer topology given in Fig. 3 is evaluated as

$$I_{out} = \frac{1}{2} k V_{in}^2 \,. \tag{6}$$

Here, $k = k_{n4} = k_{p1}$. Moreover unity current gain is assumed for the current mirror composed of transistors M_2 and M_3 ($k_{n2} = k_{p3}$) to ensure equal cycles at the output current. Considering mismatch between bias voltages and threshold voltages of the transistors, the output current of the squarer topology given in Figs. 1-3 can be expressed as

$$I_{out} = \begin{cases} \frac{1}{2} k \left(V_{in} - \Delta \mathrm{V}_1 \right)^2 & V_{in} > 0 \\ \frac{1}{2} k \left(V_{in} - \Delta \mathrm{V}_2 \right)^2 & \text{otherwise} \end{cases} \tag{7}$$

In (7), undesired components, ΔV_1 and ΔV_2, are voltage differences between corresponding bias voltages and threshold voltages. The output current, I_{out}, in (7) can be rewritten as

$$I_{out} = \begin{cases} a_2 V_{in}^2 + a_1 V_{in} + a_0 & V_{in} > 0 \\ b_2 V_{in}^2 + b_1 V_{in} + b_0 & \text{otherwise} \end{cases} \tag{8}$$

where a_1, b_1, a_0 and b_0 given below are ideally equal to zero.

$$\begin{aligned} & a_2 = b_2 = \frac{k}{2}, \\ & a_1 = -k\Delta \mathrm{V}_1,\ b_1 = -k\Delta \mathrm{V}_2, \\ & a_0 = \frac{k}{2} \Delta \mathrm{V}_1^2,\ b_0 = \frac{k}{2} \Delta \mathrm{V}_2^2. \end{aligned} \tag{9}$$

If ΔV_1 and ΔV_2 in (9) are set to zero, the suggested circuits have approximately zero dc current yielding very low power dissipation. In other words, the developed squarer structures can ideally be operated in class B mode.

For providing the bias voltages required in the proposed squarer circuits, one can use the biasing circuit topologies described in [12]. As an example the following relationships can be written for the biasing circuit shown in Fig. 4.

$$I = \frac{1}{2} k_{n1} \left(V_{DS1} - \mathrm{V}_{\text{TN}} \right)^2 = \frac{1}{2} k_{n2} \left(V_{DS2} - \mathrm{V}_{\text{TN2}} \right)^2, \tag{10}$$

$$V_{DS1} + V_{DS2} = V_{DD} \,. \tag{11}$$

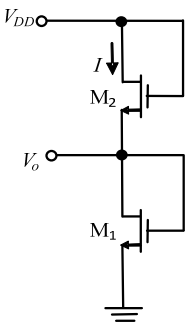

Fig. 4. Bias voltage generator circuit.

The output voltage of the circuit in Fig. 4 is found as

$$V_o = \frac{\sqrt{k_{n1}}}{\sqrt{k_{n1}}+\sqrt{k_{n2}}} \mathrm{V_{TN1}} + \frac{\sqrt{k_{n2}}}{\sqrt{k_{n1}}+\sqrt{k_{n2}}} (V_{DD} - \mathrm{V_{TN2}}). \quad (12)$$

If $k_{n1} >> k_{n2}$ thus $V_o \cong V_{TN1}$. Thus the circuit of Fig. 4 can be used to extract the threshold voltage V_{TN}. Alternative circuits for extracting V_{TN} and V_{TP} voltages can be found in [13], [14].

3. Current-Mode Rectifier

In this section a new CMOS-based CM full-wave rectifier is proposed as shown in Fig. 5. If the CM input signal is in the positive cycle, M_1 and M_2 are OFF while others are in saturation region; thus, the input signal is transferred from the transistors M_5, M_6, and M_3 to the transistor M_4 in the same direction as I_{rect+} Similarly, if the input signal is in the negative cycle, transistors M_3, M_4, M_5 and M_6 are OFF while M_1 and M_2 operate in saturation region; accordingly, this signal can pass in the opposite sign from M_2(I_{rect-}). The output current which can be obtained by connecting I_{rect+} and I_{rect-} together is calculated as follows:

$$I_{out} = I_{\mathrm{rect}+} + I_{\mathrm{rect}-} = |I_{in}|. \quad (13)$$

Here I_{rect+} and I_{rect-} are respectively defined as

$$I_{\mathrm{rect}+} = \begin{cases} I_{in} & I_{in} \geq 0 \\ 0 & \text{otherwise} \end{cases} \quad (14)$$

$$I_{\mathrm{rect}-} = \begin{cases} -I_{in} & I_{in} \leq 0 \\ 0 & \text{otherwise} \end{cases} \quad (15)$$

It is important to note that by changing the aspect ratios of M_2 and M_4, the magnitude of I_{out} in (13) can be set to any value. In other words, the output current in (13) can be given as

$$I_{out} = aI_{\mathrm{rect}+} + bI_{\mathrm{rect}-} \quad (16)$$

where, a and b are positive real numbers whose values depend on the aspect ratios of CMOS transistors of Fig. 5.

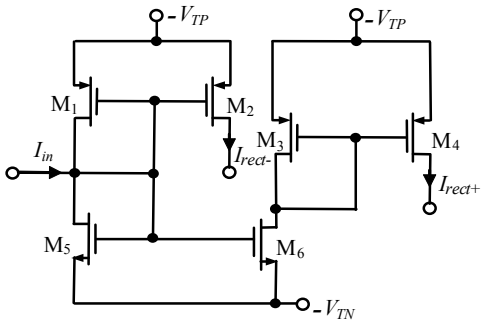

Fig. 5. Developed CMOS-based current-mode full-wave rectifier circuit.

4. Simulation Results

In this section, simulation results of the proposed circuits obtained through SPICE program using BSIM 3v3, 0.18 μm TSMC CMOS technology parameters (V_{TN0}= 0.3725 V, V_{TP0}= –0.3948 V, μ_{0N}= 259.53 cm^2/V-s, μ_{0P}= 109.976 cm^2/V-s, T_{OX}= 4.1 nm), are given. Aspect ratios of MOS transistors of the squarer circuits are given in Tab. 1.

PMOS Transistors	W(μm)/L(μm)
M_1	9.54/1.08
M_2	8.64/1.08
NMOS Transistors	W(μm)/L(μm)
M_3	3.6/1.08
M_4	3.78/1.08

Tab. 1. Dimensions of the transistors used for the squarer circuits of Figs. 1 and 2.

A sinusoidal voltage signal with 150 mV peak value at 250 kHz is applied to the inputs of the developed squarer topologies in Figs. 1 and 2 to obtain the squared output currents as shown in Fig. 6. The input-output transfer characteristics of the proposed squarer circuits are depicted in Fig. 7. As it can be seen from the characteristics shown in Fig. 7, a subthreshold current of approximately 200 nA flows through the transistors for zero input voltage. Additionally, the total power dissipations of the circuits in Figs. 1 and 2 (excluding biasing circuitry) are found approximately equal to 0.08 μW. The circuit of Fig. 1 is selected as an example to demonstrate the transistor mismatch effects on the performance of the squarer. The channel widths of the transistors M_1 and M_2 in Fig. 1 are changed respectively from 9.18 μm to 10.08 μm and 8.1 μm to 9 μm by 0.18 μm increments. The resulted output waveforms are shown in Fig. 8.

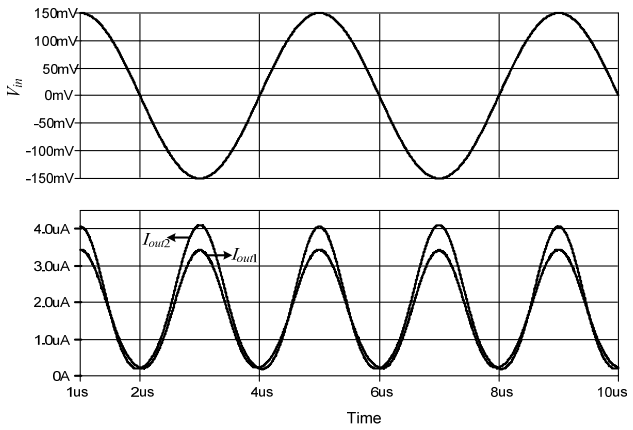

Fig. 6. Output currents of the squarer circuits of Figs. 1 and 2.

Aspect ratios of CMOS transistors in the rectifier circuit of Fig. 5 are given in Tab. 2. A CM sinusoidal signal with 20 μA peak value at 1 MHz is applied to the input of the developed rectifier depicted in Fig. 5 to obtain the full-

wave rectified output current as shown in Fig. 9. In addition the output current of the suggested rectifier against the applied input current is drawn in Fig. 10. Note that the proposed rectifier can operate well up to 20 MHz.

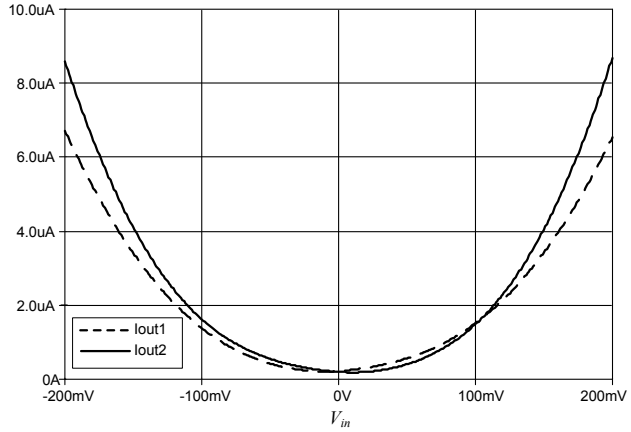

Fig. 7. Transfer characteristics of the squarer circuits of Figs. 1 and 2.

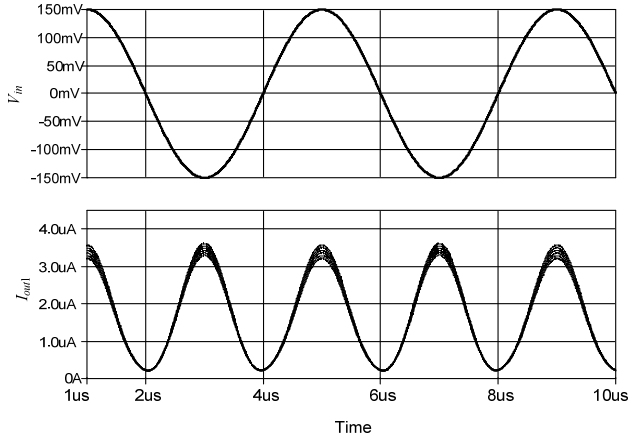

Fig. 8. Input voltage and output current waveforms of the squarer circuit of Fig. 1 under transistor mismatch.

It is seen from Figs. 6-10 that the simulation results are in good agreement with theoretical ones as expected. However, the slight discrepancy between ideal and simulation output currents of the proposed squarer and rectifier circuits mainly arises from the non-idealities of the CMOS transistors.

PMOS Transistors	***W*(μm)/*L*(μm)**
M_1 and M_3	10.8/0.18
M_2	12.06/0.18
M_4	15.48/0.18
NMOS Transistors	***W*(μm)/*L*(μm)**
M_5 and M_6	3.6/0.18

Tab. 2. Dimensions of the transistors used for the rectifier topology of Fig. 5.

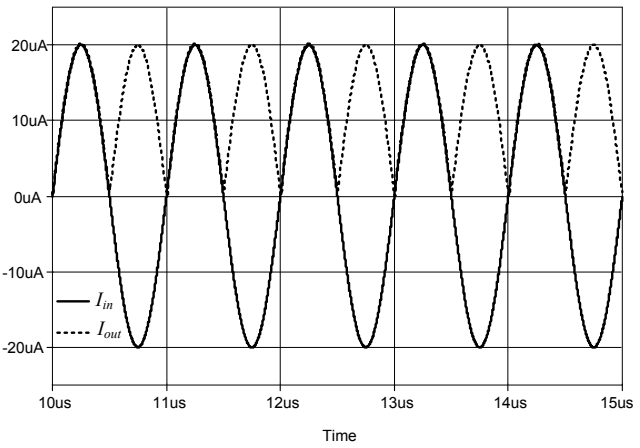

Fig. 9. Input and output currents of the rectifier circuit in Fig. 5.

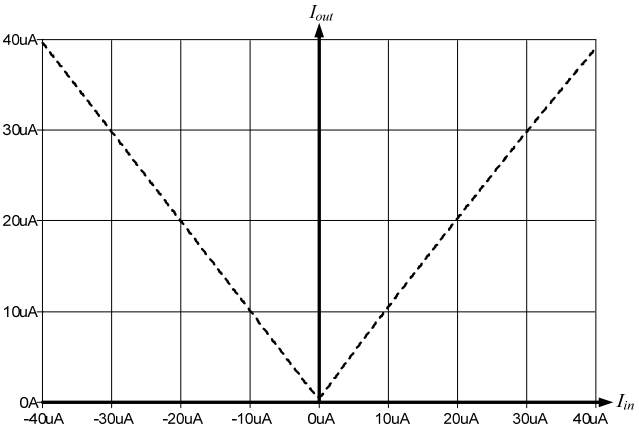

Fig. 10. Input-output characteristic of the proposed current-mode full-wave rectifier circuit.

5. Conclusion

In this paper new squarer and CM rectifier circuits are presented. The introduced CMOS-based squarer and rectifier circuits are simple, and consume low power; accordingly, they are suitable for integrated circuit technology. Simulation results using SPICE program with 0.18 μm TSMC CMOS technology parameters verify the theory well as desired.

References

[1] FIKOS, G., SISKOS, S. Analogue CMOS vector normalisation circuit. *Electronics Letters*, 1999, vol. 35, no. 25, p. 2197-2198.

[2] LOPEZ-MARTIN, A. J., RAMIREZ-ANGULO, J., CHINTHAM, R., CARVAJAL, R. G. Class AB CMOS analogue squarer circuit. *Electronics Letters*, 2007, vol. 43, no. 20, p. 336-338.

[3] WILSON, B. Recent developments in current conveyors and current-mode circuits. *IEE Proceedings Circuits, Devices and Systems*, 1990, vol. 137, no. 2, p. 63-77.

[4] TOUMAZOU, C., LIDGEY, F. J., HAIGH, D. G. *Analog IC Design: The Current-Mode Approach*. London: Peter Peregrinus, 1990.

[5] ROBERTS, G. W., SEDRA, A. S. All current-mode frequency selective circuits. *Electronics Letters*, 1989, vol. 25, no. 12, p. 759-761.

[6] BIOLEK, D., HANCIOGLU, E., KESKIN, A. U. High-performance current differencing transconductance amplifier and its application in precision current-mode rectification. *AEU-International Journal of Electronics and Communications*, 2008, vol. 62, no. 2, p. 92-96.

[7] WANG, Z. Novel pseudo RMS current converter for sinusoidal signals using a CMOS precision current rectifier. *IEEE Transactions on Instrumentation and Measurement*, 1990, vol. 39, no. 4, p. 670-671.

[8] RAMIREZ-ANGULO, J., CARVAJAL, R. G., TOMBS, J., TORRALBA, A. Very low-voltage class AB CMOS and bipolar precision current rectifiers. *Electronics Letters*, 1999, vol. 35, no. 22, p. 1904-1905.

[9] CHANG, C.-C., LIU, S.-I. Current-mode full-wave rectifier and vector summation circuit. *Electronics Letters*, 2000, vol. 36, no. 19, p. 1599-1600.

[10] WILSON, B., MANNAMA, V. Current-mode rectifier with improved precision. *Electronics Letters*, 1995, vol. 31, no. 4, pp. 247-248.

[11] SEDRA, A. S., SMITH, K. C. *Microelectronic Circuits.* Fifth edition. New York: Oxford University Press, 2004.

[12] MALOBERTI, F. *Analog Design for CMOS VLSI Systems*. Boston: Kluwer Academic Publishers, 2001, p. 197-198.

[13] MANARESI, N., FRANCHI, E., GNUDI, A., BACCARANI, G. MOSFET threshold extraction circuit. *Electronics Letters*, 1995, vol. 31, no. 17, p. 1434-1435.

[14] CILINGIROGLU, U., HOON, S. K. An accurate self-bias threshold voltage extractor using differential difference feedback amplifier. In *IEEE International Symposium on Circuits and Systems*. Geneva (Switzerland), 2000, vol. 5, p. 209-212.

About Authors …

Shahram MINAEI received the B.Sc. degree in Electrical and Electronics Engineering from Iran University of Science and Technology, Tehran, Iran, in 1993 and the M.Sc. and Ph.D. degrees in Electronics and Communication Engineering from Istanbul Technical University, Istanbul, Turkey, in 1997 and 2001, respectively. He is currently a Professor at the Department of Electronics and Communication Engineering, Dogus University, Istanbul, Turkey. He has more than 80 publications in scientific journals or conference proceedings. His current field of research concerns current-mode circuits and analog signal processing.

Dr. Minaei has served as a reviewer for several international journals and conferences. He is a senior member of the IEEE, an associate editor of the Journal of Circuits, Systems and Computers (JCSC), and an area editor of the International Journal of Electronics and Communications (AEÜ).

Erkan YUCE was born in 1969 in Nigde, Turkey. He received the B.Sc. degree from the Middle East Technical University, the M.Sc. degree from Pamukkale University and the PhD. degree from Bogazici University all in Electrical and Electronics Engineering in 1994, 1998 and 2006, respectively. He is currently an Assistant Professor at the Electrical and Electronics Engineering Department of Pamukkale University. His current research interests include analog circuits, active filters, synthetic inductors and CMOS based circuits. He is the author or co-author of about 80 papers published in scientific journals or conference proceedings.