All-Pass Sections with High Gain Opportunity

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Abstract. *In this paper, two new circuits for realizing first-order voltage-mode (VM) all-pass section (APS) with variable gain are presented. The first proposed filter uses a single differential difference current conveyor (DDCC), one grounded capacitor and three resistors. The second proposed filter consists of two DDCCs, three grounded resistors and one grounded capacitor. It provides high-input and low-output impedances and can provide high gain. Both of the proposed circuits do not require any element matching condition. Moreover, oscillator circuits with minimum number of active and passive elements are derived from the proposed APSs. The proposed circuits are tested experimentally or by simulation using SPICE program to confirm the theory.*

Keywords

All-pass section, DDCC, voltage-mode, oscillator.

1. Introduction

Since they offer an attractive method of matching phase and producing delay in electronic systems, the first and higher-order all-pass sections (APSs) have been received attention. Many voltage-mode (VM) first-order APS (or all-pass filter) topologies employing various types of active elements have been presented in the literature [1]-[29]. A good design of all-pass filter should possess the following features:

- Employing minimum number of active and passive elements, i.e., one active element, one resistor (or three resistors if provides variable gain) and one capacitor.
- Use of grounded passive elements (particularly capacitors) which is important from integration point of view. In addition, they can absorb equivalent shunt resistive/capacitive parasitic.
- Realizing all-pass function without requiring matching condition between passive element values.
- Having both of high input and low output impedances which are important for cascading.
- Producing a gain to provide both filtering and amplification operations simultaneously.
- Achievement of positive and negative types of APS from the same topology.
- Electronic tunability of the pole frequency.
- Low sensitivities.

The all-pass filters reported in [2]-[7], [10], and [13]-[15] employ single active element but do not provide gain and require matching conditions. On the other hand the circuits in [1], [7], and [9] provide gain but still suffer from the need of matching conditions. The circuits in [6] and [23] have a gain of less than unity and/or require matching condition. Some of the filters in [8] are constructed with minimum number of passive and active elements but the gain is unity. The other filters in [8] require matching condition without providing gain. The all-pass filters in [11], and [12] are attractive circuits with high input impedances and all grounded passive elements. However, they use two active elements and require matching conditions without providing gain. The proposed filters in [16] employ a fully differential current conveyor (FDCCII) as active element and enjoy the low output impedance feature. Although the filters in [16] do not require matching conditions, their gains are unity. On the other hand, the all-pass filters in [17]-[20] are based on using single differential difference current conveyor (DDCC) [30] and minimum number of passive elements (only one resistor and one capacitor) without requiring any matching conditions. However, all of these filters have unity gain and do not provide both high input and low output impedances simultaneously. All-pass filters employing two differential voltage current conveyors (DVCCs) [31] and minimum number of passive elements with low output impedance are presented in [21], [22]. The filter in [21] uses the intrinsic resistance of the X terminal of the DVCC instead of using external resistor which provides tunability for the filter. However, both of the filters in [21] and [22] do not provide voltage gain. Similarly, an APS employing two DDCCs, one grounded resistor and one grounded capacitor is presented in [29] but only unity gain is obtained. Note that, amplifying a weak signal during the filtering operation is very important in electronic and communication systems.

In a recently published paper [24] a gain-variable VM all-pass filter is obtained from a CM all-pass filter. It employs low number of passive elements (i.e. three grounded resistors and a single grounded capacitor) but

requires two dual-output second-generation current conveyors (DO-CCIIs) as active elements. Besides, it provides a variable gain in the form of two resistors ratio but it is not suitable for providing very high gain since the spread of the resistance values becomes large, which is an undesired feature in the integrated circuit implementation. Unity-gain DVCC-based APSs with high-input and low-output impedances employing minimum number of passive elements without matching condition requirement are also proposed in [28]. Adding two extra resistors to the first proposed circuit of [28] a gain-variable APS is obtained, but similar to the VM filter in [24] it is not suitable for achieving very high gain due to the requirement of large spread values of the resistances. The proposed circuit in [25] achieves positive and negative types of APS from the same topology simultaneously. However, the circuit suffers from the use of two different types of active elements; a universal voltage conveyor (UVC) and an operational transconductance amplifier (OTA). Moreover it employs a floating capacitor. The all-pass circuit in [26] uses only one active element named voltage differencing differential input buffered amplifier (VD-DIBA) which can be implemented by one OTA and one differential-input voltage buffer. It employs only one grounded capacitor and achieves high input and low output impedances but does not provide any gain opportunity. In [27] new APSs using single current differencing buffered amplifier (CDBA) as active element are proposed. Possible drawbacks of the circuits in [27] can be mentioned as use of floating capacitors and lack of high input impedance for VM operation.

In this work two new topologies for VM-APS are proposed. The first proposed configuration uses only one DDCC, one grounded capacitor and two/three resistors (two resistors if intrinsic terminal resistance of the DDCC is used). The second proposed VM-APS employs two DDCCs, one grounded capacitor and three grounded resistors. The main advantage of the second proposed APS is that it can provide very high gain without requiring large spread values for the resistances. It should be noted that the grounded or floating resistors of the proposed circuits can be easily realized with electronically controllable CMOS-based resistors [32]-[34]. Thus, electronic tunability for the pole frequency and gain of the filters can be provided. Both of the proposed circuits do not require matching condition for passive elements. The non-ideally effects of the DDCC on the proposed filters are investigated. In addition, two oscillators each based on one of the two proposed APSs are suggested as applications. The first proposed APS is experimentally tested while the second one and the derived quadrature oscillator are simulated using SPICE program to confirm their functionality.

2. Proposed Gain-Variable APSs

The DDCC is an active element with terminals namely Y1, Y2, Y3, X and Z. The terminal voltage-current relationships of a DDCC can be expressed as [30]:

$$I_{Y1} = I_{Y2} = I_{Y3} = 0\,, \tag{1a}$$

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} + \beta_3 V_{Y3}\,, \tag{1b}$$

$$I_Z = \pm \alpha I_X\,. \tag{1c}$$

Here it is assumed that all of the terminal currents flow into the active element. The Y terminals are high-impedance voltage inputs, Z is the high-impedance current output and X terminal of the DDCC exhibits a low-impedance whose value depends on the biasing current (voltage). The coefficients β_i (i = 1, 2, 3) are the voltage gains and α is the current gain of the DDCC, ideally all equal to unity. Note that the plus and minus signs of α in (1c) indicate the non-inverting (DDCC+) and inverting (DDCC−) type of DDCC, respectively.

2.1 The First Proposed Configuration

Considering the X terminal resistance (R_x) of the DDCC, (1b) (with α and β parameters equal to unity) is modified as

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} + I_x R_x\,. \tag{2}$$

Using a single DDCC+, one grounded capacitor and three resistors a gain-variable VM first-order APS is obtained as shown in Fig. 1. The proposed filter does not require passive element matching. Its transfer function (TF) can be obtained as

$$\frac{V_{out}}{V_{in}} = \frac{R_3}{R_2 + R_x} \cdot \frac{1 - sCR_1}{1 + sCR_1} \tag{3}$$

which results in a pole frequency of ω_o=1/(R_1C). The phase response of the filter is found as

$$\varphi(\omega) = -2\arctan(\omega C R_1)\,. \tag{4}$$

From (3) and (4) it can be realized that the gain of the filter can be controlled by changing R_3, R_x and R_2 without disturbing the phase response of the filter. Moreover, since R_x and R_2 are connected in series, one can easily remove R_2 to obtain a simpler circuit. In this case the TF in (3) becomes

$$\frac{V_{out}}{V_{in}} = \frac{R_3}{R_x} \cdot \frac{1 - sCR_1}{1 + sCR_1}\,. \tag{5}$$

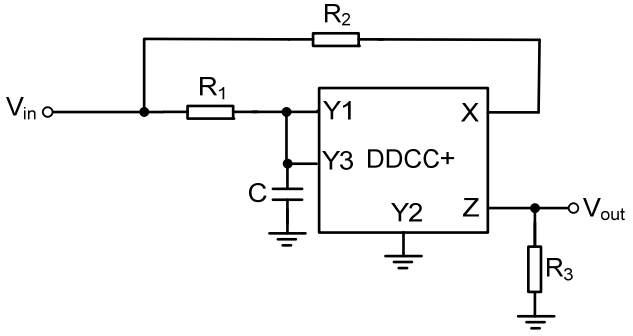

Fig. 1. The first proposed gain-variable first-order APS.

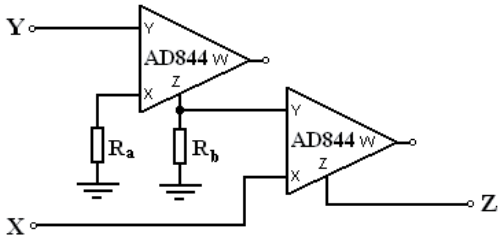

Fig. 2. Realization of a CCII+ with variable voltage gain using AD844s.

Note that since the R_x resistance of the X terminal is very low (ideally zero) the proposed filter without using R_2 can be used for obtaining very high gain values. Moreover, by interchanging R_1 and C in the circuit of Fig. 1 a negative-type all-pass filter with variable gain is obtained. Considering the non-ideal gains of the DDCC+, the TF of the proposed filter in Fig. 1 is found as

$$\frac{V_{out}}{V_{in}} = \frac{R_3}{R_2 + R_x} \cdot \frac{\alpha(\beta_1 + \beta_3 - 1 - sCR_1)}{1 + sCR_1}. \tag{6}$$

It can be seen that the non-ideal current and voltage gains of the DDCC+ does not disturb the pole frequency of the proposed filter. The phase response of the filter can also be obtained as

$$\varphi(\omega) = -\arctan\left(\frac{CR_1\omega}{\beta_1 + \beta_3 - 1}\right) - \arctan(CR_1\omega). \tag{7}$$

It is worthy to note that the DDCC+ in the all-pass filter of Fig. 1 operates as a positive-type second generation current conveyor (CCII+) with a voltage gain of two. Alternatively, one can use commercially available integrated circuits AD844s (IC of Analog Devices) together with external resistor to obtain a gain-variable CCII as shown in Fig. 2. For the circuit shown in Fig. 2 if $R_b = 2R_a$ is selected a CCII+ with $\beta = 2$ is obtained.

The sensitivities of the pole frequency and the gain $K = R_3/(R_2 + R_x)$ with respect to passive elements for the proposed circuit of Fig. 1, are calculated as

$$S_{R_1}^{\omega_o} = S_C^{\omega_o} = -1,\ S_{R_3}^{K} = 1,\ S_{R_2}^{K} = \frac{-R_2}{R_2 + R_x}, S_{R_x}^{K} = \frac{-R_x}{R_2 + R_x}.$$

Thus all of the sensitivities are equal or less than unity in magnitude.

2.2 The Second Proposed Configuration

The second new topology proposed for VM-APS with high gain opportunity is shown in Fig. 3. It employs two DDCC+s, three grounded resistors and one grounded capacitor. The TF of the filter in this case is found as:

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_2 - R_3}\frac{1 - sR_1C}{1 + sR_1C} \quad \text{for } R_2 > R_3. \tag{8}$$

Thus, the phase response of the filter is found as:

$$\varphi(\omega) = \pi - 2\arctan(\omega CR_1). \tag{9}$$

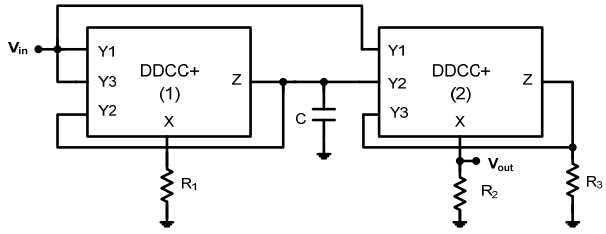

Fig. 3. The second proposed VM-APS with high gain opportunity.

Note that realization of the positive-type APS is simply achieved by interchanging the connection of Y1 and Y2 terminals of the second DDCC+ without interchanging of the resistor and the capacitor. Considering the non-ideal gains of the DDCC+, the TF given in (8) is found as

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_2 - \alpha_2\beta_{32}R_3}\frac{(\beta_{11}\beta_{22} - \beta_{12}\beta_{21} + \beta_{22}\beta_{31})\alpha_1 - \beta_{12}sR_1C}{\beta_{21}\alpha_1 + sR_1C}. \tag{10}$$

Thus, the phase response becomes:

$$\varphi_1(\omega) = \pi - \arctan\left(\frac{\beta_{12}\omega CR_1}{(\beta_{11}\beta_{22} - \beta_{12}\beta_{21} + \beta_{22}\beta_{31})\alpha_1}\right) - \arctan\left(\frac{1}{\beta_{21}\alpha_1}\omega CR_1\right) \tag{11}$$

Here, β_{1k}, β_{2k}, β_{3k} and α_k (k = 1, 2) are mentioned parameters associated with the k^{th} DDCC+. From (10) and (11) it is obvious that the TF and consequent phase response of the filter are altered due to the non-ideal gains of the DDCC+s. Note that a high voltage gain can be achieved at the filter's output by adjusting the difference between resistor values R_2 and R_3. To the best knowledge of the authors, the proposed circuit of Fig. 3 is the first all-grounded passive elements APS which can provide very high gain without requiring large spread of resistance values and passive element matching. Moreover, since each of the resistors R_1 and R_2 is connected to the X terminal of the active elements the value of the intrinsic X terminal resistance (R_x) of the DDCC+s can be omitted or added to the connected resistors.

The sensitivities of the pole frequency and the gain $K = R_2/(R_2 - R_3)$ with respect to passive elements for the proposed circuit of Fig. 3, are calculated as

$$S_{R_1}^{\omega_o} = S_C^{\omega_o} = -1,\ S_{R_3}^{K} = -S_{R_2}^{K} = \frac{R_3}{R_2 - R_3}.$$

Thus the gain of the filter in Fig. 3 is sensitive with respect to the values of R_2 and R_3.

3. Proposed Oscillator Circuits

Replacing the resistor R_3 in the all-pass circuit of Fig. 1 with a capacitor and cascading it with an inverting amplifier results in an oscillator circuit as shown in Fig. 4. The loop gain of the first proposed oscillator is obtained as:

$$T(s) = \frac{-1}{sC_2(R_x + R_2)} \cdot \frac{1 - sC_1R_1}{1 + sC_1R_1}. \quad (12)$$

Equating $T(s) = 1$ results in the following oscillation condition and oscillation frequency

$$R_1C_1 \geq (R_2 + R_x)C_2, \quad (13)$$

$$\omega_o = \frac{1}{\sqrt{R_1C_1(R_2 + R_x)C_2}}. \quad (14)$$

As it can be seen from Fig. 4, the proposed oscillator contains an inverting amplifier. A possible realization for the inverting amplifier consisting only two NMOS transistors is given in [23].

The second proposed oscillator is obtained by replacing R_3 in the APS of Fig. 3 with a second capacitor (C_2), removing the feedback from Z to Y3 terminal of the second DDCC and performing a feedback from Z terminal of the second DDCC+ to the input as shown in Fig. 5. Note that it is obtained directly from the APS of Fig. 3 without using any additional active elements; an advantageous feature compared to the first proposed oscillator and the APS-based quadrature oscillators given in [11], [14], and [18]. The oscillation frequency and oscillation condition of the proposed oscillator of Fig. 5 are found respectively as:

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}}, \quad (15)$$

$$R_1C_1 \geq R_2C_2. \quad (16)$$

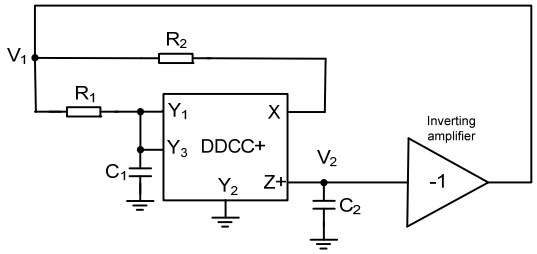

Fig. 4. The first oscillator circuit derived from the first proposed APS.

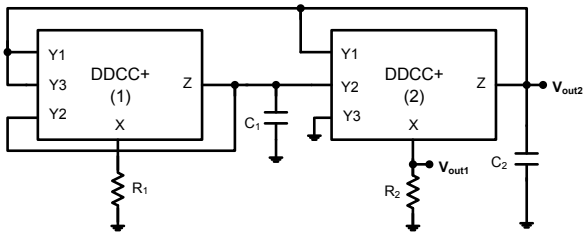

Fig. 5. The quadrature oscillator based on the second proposed APS.

4. Experimental and Simulation Results

The first proposed filter of Fig. 1 is constructed practically. Two AD844s are used to obtain a CCII+ of gain 2 as shown in Fig. 2 selecting R_a= 10 kΩ and R_b= 20 kΩ. Then it is used to construct the first proposed APS with passive element values as: R_1= 10 kΩ, R_2= 2 kΩ (ignoring $R_x \cong 50\ \Omega$ for AD844), R_3= 20 kΩ and C = 1 nF, which results in a pole frequency of $f_o = \omega_o/(2\pi)$ = 15.9 kHz and a gain of 10. The input and output waveforms of the filter are shown in Fig. 6 where the gain is computed as 9.46. The gain and frequency deviations are due to the non-idealities of AD844s and tolerances of the passive elements.

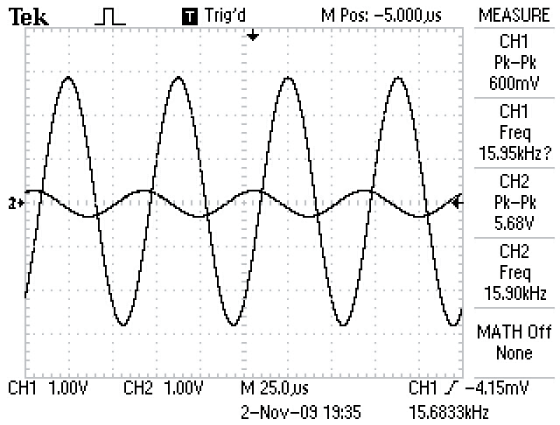

Fig. 6. Experimental result for the first proposed APS with a gain of approximately 10.

The second proposed VM–APS is simulated with SPICE program using 0.25 µm TSMC CMOS technology parameters. The CMOS implementation of the DDCC+ is shown in Fig. 7, which is adopted from the circuit proposed in [30]. The supply and bias voltages are chosen as $V_{DD} = -V_{SS}$= 1.25 V and $V_{BB} = -0.8$ V. The dimensions of the CMOS transistors employed in DDCC+ are depicted in Tab. 1. The passive elements of the APS given in Fig. 3 are selected as C = 10 pF, R_1= 10 kΩ, R_2= 20 kΩ and R_3= 18 kΩ. Hence a gain of 10 and a pole frequency of $f_o \approx 1.59$ MHz are obtained. The simulation results are shown in Fig. 8. In addition, the simulation result for the second proposed APS-based oscillator is given in Fig. 9 for an oscillation frequency of 159 kHz, where R_1= 10 kΩ, R_2= 9.8 kΩ and $C_1 = C_2$= 100 pF are chosen.

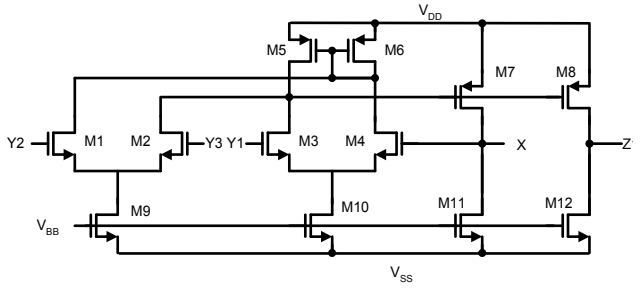

Fig. 7. The CMOS implementation of the DDCC+.

The large signal behavior of the circuit in Fig. 3 is tested with investigation of the dependence of its output harmonic distortion on the amplitude of the sinusoidal output signal at 1.59 MHz. As it can be seen from the results given in Tab. 2, the total harmonic distortion (THD)

for a sinusoidal output voltage with peak value of 215 mV at 1.59 MHz is equal to 5.69%. Also, it is observed that the harmonic distortion increases rapidly for the peak output signal amplitude beyond 110 mV. Fig. 10 shows the time-domain response of the filter with a gain of approximately 10 for a sinusoidal input with peak voltage of 20 mV and frequency of 1.59 MHz.

Transistor	W (μm)	L (μm)
M1-M4	10	0.5
M5-M6	4.5	0.5
M7-M8	8.5	0.5
M9-M10	27.5	0.5
M11-M12	44	0.5

Tab. 1. Transistor dimensions of the DDCC+ circuit in Fig. 7.

Output Voltage (peak) (mV)	THD (%)
10	0.6
30	0.73
50	0.74
80	0.62
110	0.7
140	1.24
165	1.87
190	2.81
205	4.33
215	5.69

Tab. 2. Dependence of output harmonic distortion of the second VM-APS of Fig. 3 on output signal amplitude.

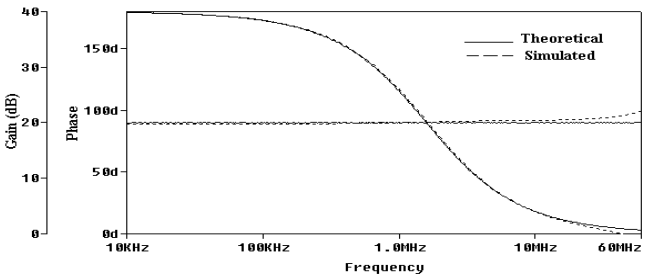

Fig. 8. Frequency responses of gain and phase of the second VM-APS of Fig. 3.

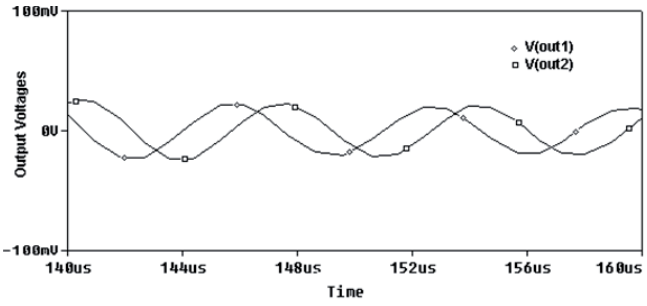

Fig. 9. The output waveforms of the quadrature oscillator in Fig. 5.

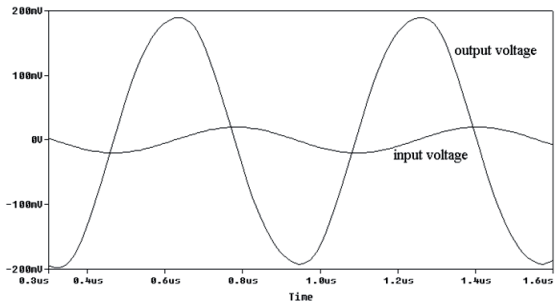

Fig. 10. Time-domain response of the second VM-APS of Fig. 3 with a gain of approximately 10 for an input peak voltage of 20 mV.

5. Conclusion

In this work, two VM-APS circuits have been presented. The first circuit employs only one DDCC+ together with one grounded capacitor and two or three resistors. No passive component matching constraints are required for the proposed circuit. The gain of the filter can be adjusted through biasing voltage of the DDCC+ which changes its X terminal intrinsic resistance (R_x), or changing the external resistor values without disturbing the pole location of the filter. The second proposed circuit employs two DDCC+s, one capacitor and three resistors. The second APS circuit enjoys the following advantages:

- High input impedance which is important for cascade connections.
- Use of only grounded passive elements which is attractive in integrated circuit implementation.
- Both the positive and the negative type of first-order VM-APSs can be realized from the same topology by interchanging of two connection terminals of the second DDCC+ (Y1 and Y2).
- No matching conditions are required.
- Possibility of achieving a high variable gain.
- Deriving a quadrature oscillator from the proposed APS without using an additional active element.

One can obtain the feature of electronic tunability of the pole frequency and the gain for both of the proposed filters by using CMOS-based resistors instead of the external resistors. In addition, both of the proposed circuits enjoy low pole frequency sensitivity and no capacitor is connected in series to the X terminal of the DDCC+s, which improves their high frequency performances [35]. Because of the above features, both of the proposed circuits are considered to be the most attractive VM-APSs among the previously reported prototypes.

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