Supplementary Inductance Simulator Topologies Employing Single DXCCII

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Abstract. *In this study, six grounded inductance simulator circuits are presented including additional useful features in comparison to previous dual-X current conveyor (DXCCII) based implementations. To demonstrate the performance and usefulness of the presented circuits, one of them is used to construct a fifth order Butterworth high-pass filter and a current-mode multifunction filter as application examples. Simulation results are given to confirm the theoretical analysis. The derived DXCCII and its applications are simulated using CMOS 0.35 μm technology.*

Keywords

DXCCII, inductance simulator, dual-X current conveyor.

1. Introduction

The behavior of physical inductors are not sufficiently close to ideal component behavior compared with resistors and capacitors and in terms of spatial dimensions they are larger than the other circuit elements, unless the inductance value is very small. The advent of integrated circuits has encouraged the design of synthetic inductances, which can be used instead of the bulky inductors in passive filters. The inductance simulators [1-24] can be used in many applications such as active filter design, oscillator design, analog phase shifters and cancellation of parasitic element.

In the last decade, attention is extensively focused on the inductance simulation using different current-mode active building blocks like second-generation current conveyor (CCII) [1-3], negative impedance converter [4], fully differential second-generation current conveyor (FDCCII) [5], differential voltage current conveyor (DVCC) [6], [7], differential difference current conveyor (DDCC) [8], operational transconductance amplifier (OTRA) [9], four terminal floating nullor (FTFN) [10], [11], current feedback operational amplifier (CFOA) [12-14], OTA [15], [16], current differencing buffered amplifier (CDBA) [17], [18], current differencing transconductance amplifier [19-21], current backward transconductance amplifier (CBTA) [22], and DXCCII [23-26].

In this study we present grounded inductance simulator topologies with additional useful features in comparison to previous DXCCII based inductor simulator circuits [23], [24]. For example, the number of active elements reduced by one compared to [23]. Also, advantage of using DXCCII in the design of resistor-inductor (RL) circuit in series is shown in this study in comparison to [23], [24]. Also two of the proposed circuits have minimum number of active and passive elements like the circuits in [24]. Furthermore, some of the proposed circuits have parasitic compensation or electronic tunability features in the expense of an additional resistor different from [24]. Moreover, although ref. [24] presents five different topologies, only one of them is a pure inductance simulator. In our study five of the six topologies provide pure inductance configuration. Therefore, the study provides further possibilities for the designers in the DXCCII based designs. Finally, one of the proposed grounded inductance simulators is used in a fifth-order Butterworth high-pass ladder filter and in a parallel resonant circuit as application examples. Although the presented circuits include floating capacitors, they can be realized even in integrated circuit technology of a decade ago with a CMOS process that offers a second poly layer [27]. Frequency and time domain responses are given to illustrate the performance of the proposed circuit.

2. DXCCII and Proposed Circuits

The DXCCII is conceptually a combination of the regular CCII and the inverting current conveyor (ICCII±) [28]. The DXCCII symbol is illustrated in Fig.1.

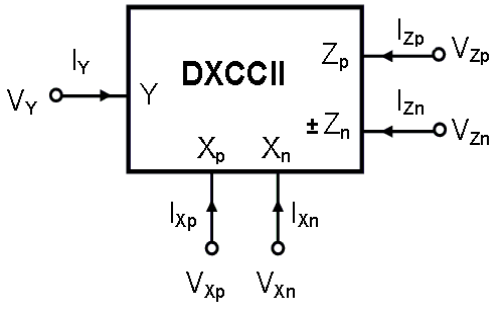

Fig. 1. The symbol of the DXCCII.

It has two X terminals, namely Xp (non-inverting X terminal) and Xn (inverting X terminal). The Xp and Xn terminal currents are reflected to the respective Z terminals, namely Zp and Zn. (It is worth emphasizing that, for this device, there is no direct relation between the Zp and Zn terminal currents).

The port relations of an ideal DXCCII shown in Fig.1 can be characterized by

$$\begin{bmatrix} I_Y \\ V_{Xp} \\ V_{Xn} \\ I_{Zp} \\ I_{Zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & \pm 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{Xp} \\ I_{Xn} \end{bmatrix} \tag{1}$$

The proposed circuits for realizing grounded inductor simulators are shown in Fig. 2. Routine analyses of the circuits in Fig.2 are given in Tab. 1.

The proposed circuits present various useful features. For example, the circuit in Fig. 2a and Fig. 2b are canonical in the number of passive as well as active elements as in [24]. Furthermore, the proposed circuits in Fig. 2c and Fig. 2d are convenient for the compensation of the undesired parasitic resistances of the DXCCII different from circuits in [24]. The circuit in Fig. 2c has resistors in series to Xp and Xn terminals. If they are chosen sufficiently higher than the parasitic resistors at the Xp and Xn terminals, undesired effects arising from these parasitics can be compensated. In Fig. 2d, all resistors are grounded and parallel to the terminals of the DXCCII which compensates for parasitic resistors at the high impedance ports of the DXCCII. Moreover, the grounded resistors in Fig. 2d can be implemented by MOSFET transistors [29], so it has easy implementation and electronic tunability advantage over the circuits in [24]. Lastly, the circuits in Fig. 2b and Fig. 2f provide a series RL realization different from the circuits in [24]. On the other hand, indeed ref. [24] includes only one pure inductor circuit, because the most of the topologies lead to negative inductance or resistor realizations. However, our study presents five different pure inductance simulator topologies. Consequently, the circuits presented in this study have advantageous features over previous DXCCII based designs and improve design capabilities of DXCCII.

3. Simulations

The DXCCII is constructed using the schematic implementation in Fig. 3 with DC supply voltages equal to ±2.5 V and bias voltages equal to V_{bn}= V_{bp}= 0 V and V_{bias}= 1.44 V. The MOS transistors are simulated using TSMC CMOS 0.35μm process model parameters. The aspect ratios of the transistors are given in Tab. 2. The main performances of the classical [25] and constructed DXCCII are summarized in Tab. 3. From Tab. 3 it can be seen that the performance of the proposed DXCCII is

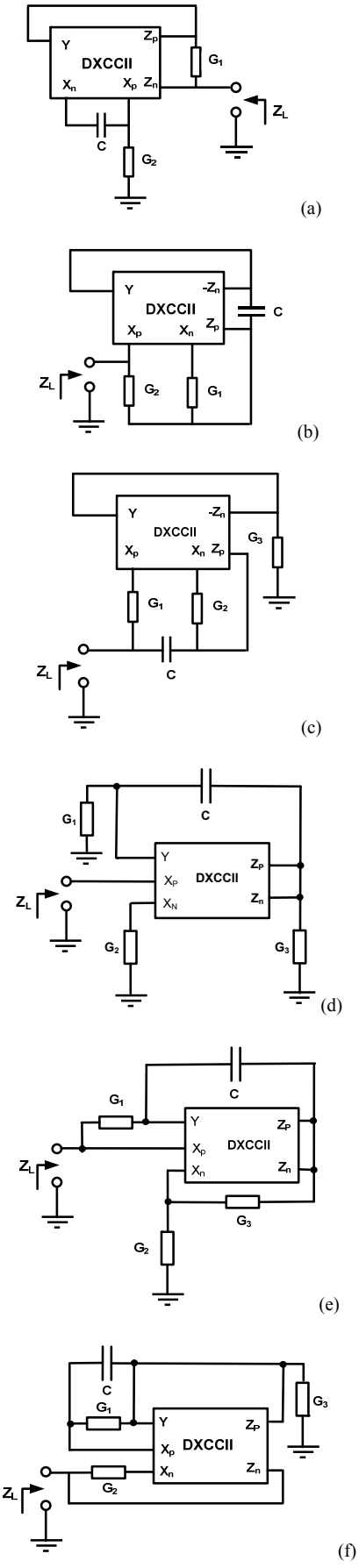

Fig. 2. Inductance simulators realized using single DXCCII.

improved in terms of the linearity, the accuracy of the current gain (α) and voltage gain (β), and the output resistance (R_Z). The proposed circuit shown in Fig. 2a is simulated with the following passive element values: $G_1 = G_2 = 0.1$ mS ($R_1 = R_2 = 10$ kΩ) and $C = 25$ pF, which results in $L_{eq} = 5$ mH. The frequency responses of the impedances of the proposed inductance simulator in Fig. 2a and an ideal inductance are shown in Fig. 4. As it can be observed from Fig. 4, the proposed inductance simulator circuit operates up to 10 MHz.

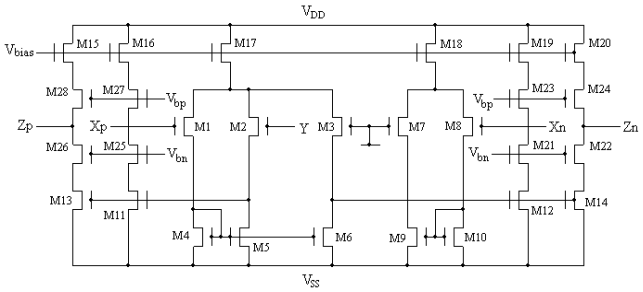

Fig. 3. The cascode dual-X current conveyor (DXCCII).

No	Type	Matching condition	L_{eq}	R_{eq}	Circuit
1	Pure L	$G_1 = G_2$	$L_{eq} = 2C/G_1^2$	-	Fig. 2a
2	Series RL	No	$L_{eq} = C/(4G_1G_2)$	$R_{eq} = 1/(4G_2)$	Fig. 2b
3	Pure L	$G_1 = G_3$, $3G_2 = 2G_3$	$L_{eq} = C/(2G_1^2)$	-	Fig. 2c
4	Parallel RL	$G_1 = G_3$, $3G_2 = G_3$	$L_{eq} = 2C/G_1^2$	$R_{eq} = 2/(3G_1)$	Fig. 2c
5	Parallel RL	No	$L_{eq} = C/(G_1G_3)$	$R_{eq} = 1/(G_1 - G_2 + G_3)$	Fig. 2d
6	Pure L	$G_1 = G_2 - G_3$	$L_{eq} = C/(G_1G_3)$	-	Fig. 2d
7	Parallel RL	No	$L_{eq} = C/(4G_1G_3)$	$R_{eq} = 1/(4G_1 - G_2)$	Fig. 2e
8	Pure L	$G_2 = 4G_1$	$L_{eq} = C/(4G_1G_3)$	-	Fig. 2e
9	Series RL	No	$L_{eq} = 2C/(G_2G_3)$	$R_{eq} = (2G_1 - G_2 + G_3)/(G_2G_3)$	Fig. 2f
10	Pure L	$G_2 = 2G_1 + G_3$	$L_{eq} = 2C/[G_2(G_2 - 2G_1)]$	-	Fig. 2f

Tab. 1. Various types of inductors realized with the presented circuits.

Transistors	W [μm]	L [μm]
M_1-M_2	1.4	0.7
M_3, M_7-M_8	2.8	0.7
M_4-M_5	2.4	0.7
M_6, M_9-M_{10}	4.8	0.7
M_{11}-M_{28}	9.6	0.7

Tab. 2. Transistors aspect ratios for the proposed circuit.

Parameters	Classical DXCCII	Proposed DXCCII
Linearity V_X/V_Y	±0.8 V	±0.8 V
Linearity I_Z/I_X	-140-150 μA	-140-150 μA
V_X/V_Y gain (α)	0.99	0.99
I_Z/I_X gain (β)	0.99	0.99
V_X/V_Y f_{-3dB}	0.76 GHz	1.2 GHz
I_Z/I_X f_{-3dB}	0.60 GHz	1.08 GHz
Output resistance (R_Z)	240 kΩ	32.5 MΩ

Tab. 3. Circuit performances of the classical [25] and proposed DXCCII.

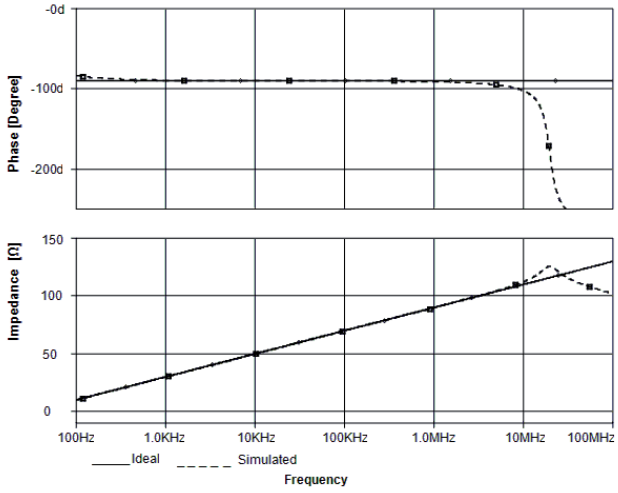

Fig. 4. Ideal and simulated frequency responses of impedance of inductance.

To demonstrate the performance of the inductance simulator proposed in Fig. 2a, we use it in the structure of a fifth-order Butterworth high-pass ladder filter shown in Fig. 5. The passive elements are selected as $C_1 = C_2 = 0.1$ nF, $C_3 = 0.2$ nF, $R_L = R_s = 1$ kΩ, and synthetic inductors $L_{eq1} = 50$ μH, $L_{eq2} = 100$ μH, which results in a 3dB frequency of 1.59 MHz. Both ideal and simulated fifth-order high-pass ladder filter responses are shown in Fig. 6.

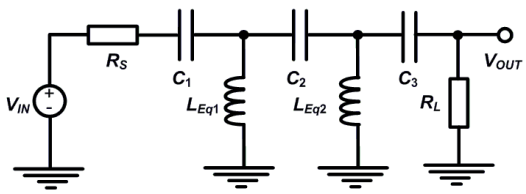

Fig. 5. Fifth-order high-pass ladder filter prototype.

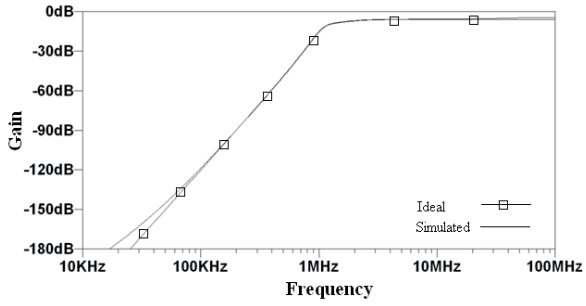

Fig. 6. Ideal and simulated frequency responses of the fifth-order Butterworth high-pass ladder filter.

To illustrate another application of the proposed inductance simulator, a current-mode multifunction filter was designed and simulated. The basic cell is an inductor simulator with a parallel capacitor C_L and resistor R_L to form parallel resonant circuit shown in Fig. 7. In this fig-

ure, actively simulated inductance simulator circuit in Fig. 2a replaces the parallel L circuit. The element values of the realized filter are chosen as follows: C_L= 50 pF, R_L= 10kΩ, R_1= 10 kΩ, R_2= 10 kΩ and C = 25 pF, thus an inductor with L_{eq}= 5 mH is obtained which results in pole frequency f_p= 0.321 MHz. The parallel resonant filter circuit in Fig. 7 is simulated with PSPICE program using a CMOS realization of DXCCII shown in Fig. 3. Simulated high-pass (I_{HP}), low-pass (I_{LP}), and band-pass (I_{BP}) responses of the parallel resonant circuit are given in Fig. 8.

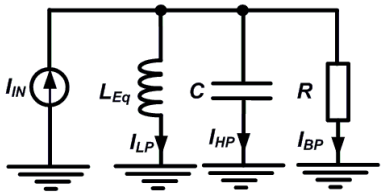

Fig. 7. Parallel resonant filter circuit.

To test the input dynamic range of the filter in Fig. 7, the simulation of the second-order high-pass filter output of the resonant filter application has been repeated for a sinusoidal input signal at f_o= 321 kHz. Fig. 9 shows time-domain analysis for a 60 μA peak-to-peak sinusoidal input signal. Fig. 10 shows that within the given input dynamic range the filter causes insignificant total harmonic distortion (THD).

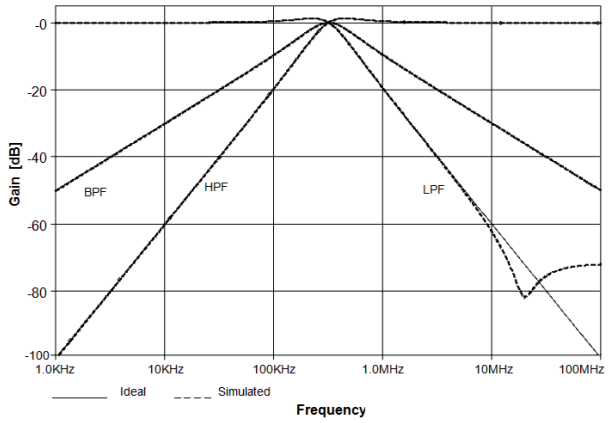

Fig. 8. Ideal and simulated high-pass, low-pass and band-pass responses of the parallel resonant filter circuit.

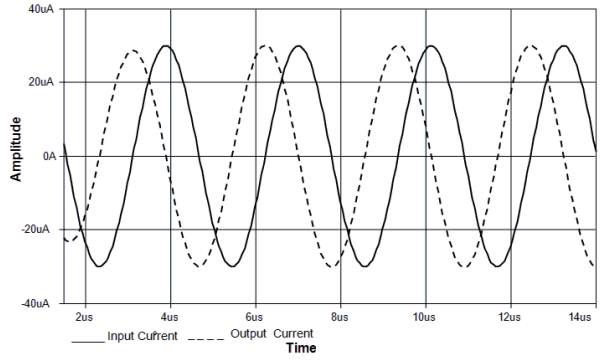

Fig. 9. The input and output waveforms of the parallel resonant high-pass filter example in Fig. 7.

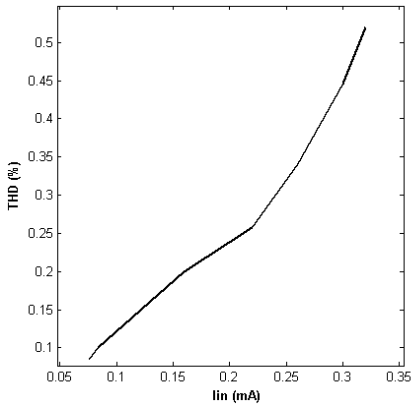

Fig. 10. Total harmonic distortion for various input current amplitudes for the parallel resonant high-pass filter application.

4. Conclusions

In this paper, we presented six novel grounded inductor simulator topologies, which have advantageous features over previous DXCCII based designs. A voltage mode fifth-order elliptic filter and a current mode multifunction filter are constructed and simulated using one of the presented inductance simulator circuits as application examples. We performed simulations with SPICE using 0.35 μm TSMC CMOS technology. Simulation results well confirm the theoretical analysis.

Acknowledgements

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