Realization of Resistorless Wave Active Filter using Differential Voltage Current Controlled Conveyor Transconductance Amplifier

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Abstract. *In this paper, a resistorless realization of high order voltage mode wave active filter based on differential voltage current controlled conveyor transconductance amplifier (DVCCCTA) is presented. The wave method is used for simulating reflected and incident wave for basic building block i.e. series inductor and configuring it for other passive element realization by making appropriate connection. The proposed structure uses grounded capacitors and possesses electronic tunability of cutoff frequency. The proposed approach is verified for a 4th order low pass filter through SPICE simulation using 0.25 μm TSMC CMOS technology parameters.*

Keywords

Differential voltage current controlled conveyor transconductance amplifier, wave Active Filter.

1. Introduction

The current mode approach for analog signal processing circuits and systems has emerged as an alternate method besides the traditional voltage mode circuits [1] due to their potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption and high operating speed. The current mode active elements are appropriate to operate with signals in current or voltage or mixed mode, and are gaining acceptance as building blocks in high performance circuit designs which are clear from the availability of wide variety of current mode active elements such as operational transconductance amplifier (OTA) [2], current feedback operational amplifier (CFOA) [3], current conveyors (CC) [4], [5], current controlled conveyor [6], differential voltage current conveyor (DVCC) [7] etc.

The recently proposed analog building blocks in open literature are obtained by cascading of various current conveyor blocks with transconductance amplifier (TA) block in monolithic chip for compact implementation of signal processing circuits and systems. Current conveyor transconductance amplifier (CCTA) [8], [9], current controlled current conveyor transconductance amplifier (CCCCTA) [10], differential voltage current conveyor transconductance amplifier (DVCCTA) [11], differential voltage current controlled conveyor transconductance amplifier DVCCCTA [12] are examples of such building blocks. The DVCCCTA has a powerful inbuilt tuning property similar to CCCCTA, and an additional high input impedance terminal which may be used for applications demanding differential and floating inputs [7], [13], [14].

This paper presents systematic design approach for realization of DVCCCTA based high order wave active filter. This method uses wave equivalent cascades for the simulation of resistively terminated LC ladder filter [15]-[17]. The wave equivalents consist of forward and reflected voltage waves present in the prototype filter. A DVCCCTA based wave equivalent is developed for an inductor in series branch which can be configured for other passive element realization by making appropriate connection. The proposed filter structure does not use any resistors in contrast to those proposed in [15]-[17] and also possesses an attractive feature of electronic tunability via bias currents of DVCCCTA. A fourth order Butterworth filter has been designed using the outlined approach and the functionality has been verified through SPICE simulation using 0.25 μm TSMC CMOS technology parameters.

2. Basic Wave Equivalent using DVCCCTA

2.1 DVCCCTA

The DVCCCTA [12] is based on DVCCTA [11] and consists of differential amplifier, translinear loop and transconductance amplifier. The port relationships of the DVCCCTA as shown in Fig. 1 can be characterized by the following matrix

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & R_x & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & g_m & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \\ V_O \end{bmatrix} \quad (1)$$

where R_x is the intrinsic resistance at X terminal and g_m is the transconductance from Z terminal to O terminal of the DVCCCTA.

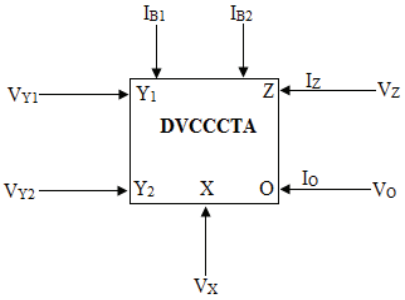


Fig. 1. Schematic Symbol of DVCCCTA.

The CMOS based internal circuit of DVCCCTA [12] in CMOS is depicted in Fig. 2. The values of R_x and g_m depend on bias currents I_{B1} and I_{B2} respectively, which may be expressed as

$$R_x = 1\Big/\left(\sqrt{2m_n C_{ox}(W/L)_{18,19} I_{B1}} + \sqrt{2m_p C_{ox}(W/L)_{16,17} I_{B1}}\right) \quad (2)$$

and

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)_{24,25} I_{B2}}\,. \quad (3)$$

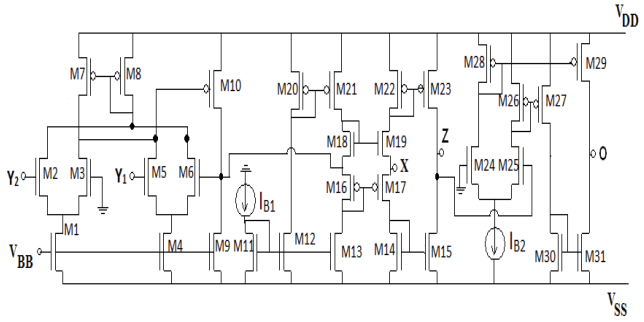


Fig. 2. CMOS implementation of DVCCCTA[12].

2.2 Basic Wave Equivalent

In wave method, the forward and reflected voltage waves are used to define the functionality of the filter. The incident and reflected voltage waves are depicted as A_j and B_j respectively for two port network of Fig. 3 and are related by the following relation:

$$A_j = V_j + I_j R_j\,, \qquad B_j = V_j - I_j R_j\,. \quad (4)$$

Equation (4) can be expressed in terms of scattering matrix S as

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = S \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}. \quad (5)$$

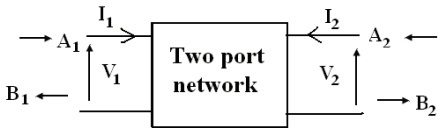


Fig. 3. Two Port Network with wave variables.

The basic element for the developing wave active filter is a series inductor L. It can be described in terms of scattering parameter as

$$S = \frac{1}{1+s\tau}\begin{bmatrix} s\tau & 1 \\ 1 & s\tau \end{bmatrix}. \quad (6)$$

The relationship between incident (A_j, j = 1,2) and the reflected wave (B_j, j = 1,2) of a series inductor may be obtained from (5) and (6) as

$$B_1 = A_1 - \frac{1}{1+s\tau}\left(A_1 - A_2\right), \quad (7)$$

$$B_2 = A_2 + \frac{1}{1+s\tau}\left(A_1 - A_2\right) \quad (8)$$

where $\tau = L/2R$ is time constant and R represents port resistance.

The implementation of wave equations (7) and (8) require three operations – lossy integration subtraction, summation and subtraction. These operations can easily be realized using DVCCCTA and are explained in the following section.

Lossy Integration Subtraction: The structure to implement lossy integration subtraction is depicted in Fig. 4. It uses a single DVCCCTA and a grounded capacitor. The output voltage V_o is given as

$$V_o = \left(V_{in1} - V_{in2}\right)\frac{1}{1+s\tau} \quad (9)$$

where $\tau = R_X C_d$ is time constant and $g_m R_X = 1$. Using (7), (8) and (9), the value of C_d may be computed as

$$R_X C_d = \frac{L}{2R}\,. \quad (10)$$

Assuming $R_X = R$, the value of capacitor C_d may be expressed as

$$C_d = \frac{L}{2R^2}\,. \quad (11)$$

Subtraction: The subtraction operation can be easily performed with DVCCCTA as it has two high input impedance terminals. Fig. 5 shows the topology that can be

used for voltage subtraction and the voltage output is given as

$$V_o = V_{in1} - V_{in2} \qquad \text{with} \quad g_m R_X = 1. \tag{12}$$

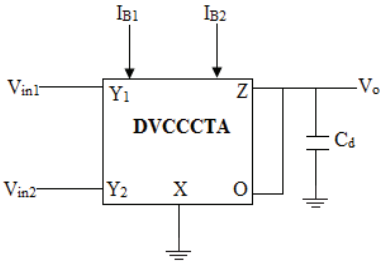


Fig. 4. Lossy Integration Subtraction using DVCCCTA.

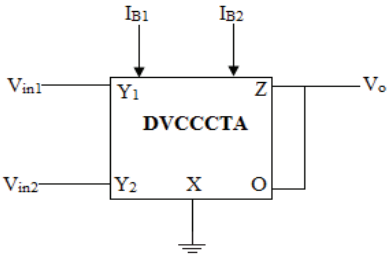


Fig. 5 Subtraction using DVCCCTA.

Summation: The circuit for summation is shown in Fig. 6. The first DVCCCTA inverts the inputs V_{in2} which is then subtracted from input V_{in1} by second DVCCCTA to provide output as

$$V_o = V_{in1} + V_{in2} \qquad \text{with} \quad g_m R_X = 1. \tag{13}$$

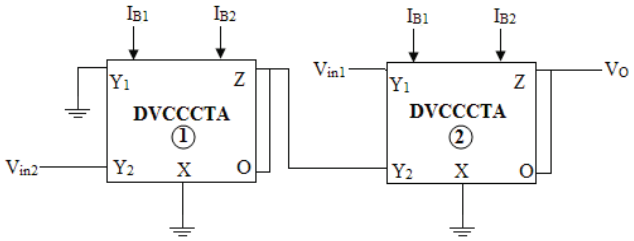


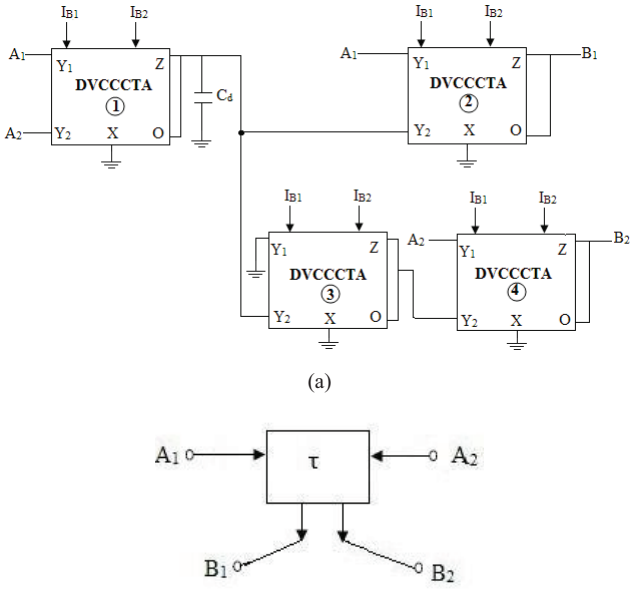
Fig. 6. Summation using DVCCCTA.

The complete schematic of wave equivalent for series inductor as given by (7) and (8) can be obtained by cascading the blocks of Figs. 4 to 6. The arrangement is shown in Fig. 7(a) and its symbolic representation [15]-[17] is shown in Fig. 7(b).

3. Realization of Passive Components

The structure shown in Fig. 7 can be used as the basic building block for deriving the wave equivalent of other reactive elements. The wave equivalent for series and shunt inductor and capacitor are given in Tab. 1 which can be obtained by swapping outputs and signal inversion. The schematic for subtraction as shown in Fig. 5 is used for signal inversion by making $V_{in1} = 0$.

The design of wave active filter starts with the selection of prototype filter based on specifications. The individual inductors or capacitors are replaced by their wave equivalents from Tab. 1 [15]-[17]. The complete filter schematic is then obtained by simply cascading the wave equivalents.



(a)

(b)

Fig. 7 (a) Complete schematic of DVCCCTA based wave equivalent of series inductor and (b) its symbolic representation.

4. Effect of Non-idealities

The frequency performance of the proposed voltage and current mode filter circuits may deviate from the ideal one due to non-idealities. The non-idealities effect may be categorized in two groups. The first comes from frequency dependence of internal current and voltage transfers of DVCCCTA. The modified port relationships may be written in matrix form as

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & R_x & 0 & 0 \\ 0 & 0 & \alpha & 0 & 0 \\ 0 & 0 & 0 & \gamma g_m & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \\ V_O \end{bmatrix}$$

where the voltage transfer functions are $\beta_1 = 1 - \varepsilon_{v1}$ and $\beta_2 = 1 - \varepsilon_{v2}$. The ε_{v1} and ε_{v2} denote voltage tracking errors from Y1 and Y2 terminals to X terminal respectively. The current transfer function is $\alpha = 1 - \varepsilon_i$, where ε_i denote current tracking error from X to Z terminal. The coefficient γ denotes current transfer function from Z terminal to O terminals. The current and voltage transfer functions apart from having non-unity values, also have poles at high frequencies. Their effect on filter performance can however be ignored if the operating frequencies are chosen

sufficiently smaller than voltage and current transfer pole frequencies of the DVCCCTA.

Considering these deviations in the voltage and current transfers the condition (with $\beta_1 = \beta_2 = \beta$)

$$g_m R_X = 1$$

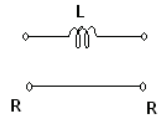
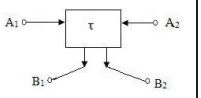
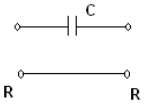
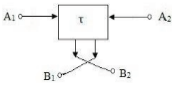
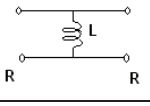
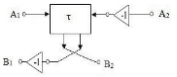
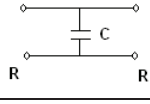
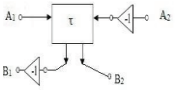
modifies to

$$g_m R_X = \gamma/(\alpha\beta) \tag{14}$$

and the value of C_d in (11) modifies to

$$C_d = \alpha\beta\frac{L}{2R^2} \tag{15}$$

The second group of non idealities comes from parasites of DVCCCTA comprising of resistances and capacitances connected in parallel at terminals Y1, Y2, Z and O (i.e. R_{Y1}, C_{Y1}, R_{Y2}, C_{Y2}, R_Z, C_Z, R_O, C_O). The effects of these parasites on filter response depend strongly on circuit topology. In the proposed structure the external capacitor appears in parallel to the parasitic capacitor, the effect of these may be accommodated by pre adjusting the external capacitor value.

Elementary two port	Port connection	Realized time constant; capacitor value for DVCCCTA based wave equivalent
		$\tau = \frac{L}{2R};\ C_d = \frac{L}{2R^2}$
		$\tau = 2RC;\ C_d = 2C$
		$\tau = \frac{2L}{R};\ C_d = \frac{2L}{R^2}$
		$\tau = \frac{RC}{2};\ C_d = \frac{C}{2}$

Tab. 1. Wave equivalent of elementary two port consisting of single element in series and shunt branch.

5. Simulation Results

To demonstrate the method outlined in Section 2 and 3, a fourth order low pass filter of Fig. 8 has been taken as prototype. The normalized component values are R_s = 1, L_1 = 0.7654, L_2 = 1.8485, C_1 = 1.8485, C_2 =0.7654 and R_L = 1 for maximally flat response.

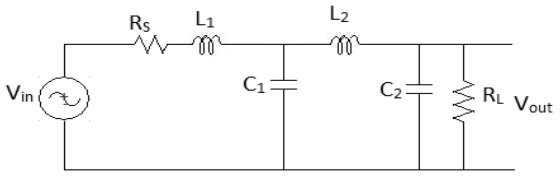


Fig. 8. 4th order Butterworth filter.

The wave equivalent topology of Fig. 8 may be constructed by replacing series inductor and shunt capacitor by wave equivalent of Tab. 1 and is shown in Fig. 9. For cut-off frequency f_o = 10 MHz, the bias currents I_{B1} and I_{B2} are taken as 25 µA and 200 µA respectively. The capacitor values for wave equivalent of series inductors (L_1, L_2) and shunt capacitors (C_1, C_2) are 4.2075 pF, 10.161 pF and 10.161 pF, 4.2075 pF respectively. The topology of Fig. 9 has been simulated using DVCCCTA based wave equivalent and inverter as discussed in Section 2 using 0.25 µm TSMC CMOS technology parameters and power supply of ±1.25 V. The aspect ratios of various transistors of DVCCCTA are listed in Tab. 2. Figs. 10 and 11 show the simulated low pass responses (V_{out}) and its complementary high pass response ($V_{out,c}$) respectively. The tunability of the filter response by varying bias current I_{B1} from 5 µA to 40 µA and I_{B2} from 40 µA to 320 µA ($I_{B2} = 8I_{B1}$ for $g_m R_x$ = 1) is also studied through simulations and the results are shown in Fig. 12. The practical tuning range depends on allowable bias current range for transistors to remain in saturation region, pole frequencies of various current and voltage transfers, and the parasitic resistances and capacitances at various ports. The simulations have been carried out for the outlined points. It is found that the allowable range for bias currents I_{B1} and I_{B2} is 5 µA to 154 µA and 10 µA to 320 µA respectively for transistors to remain in saturation region. The pole frequency for voltage transfer from Y1, Y2 to X is 244 MHz; current transfer from X to Z terminal is 885 MHz; and current gain from Z to O terminal is 606 MHz. The parasitics at Y, Z and O ports are R_Y = very high, C_Y = 20 pF, R_Z = 241 kΩ, C_Z = 33 fF, R_O = 68 kΩ, C_O = 9fF respectively. Based on the above findings the filter would operate satisfactorily for cut off frequency a decade below the minimum of current and voltage transfer pole frequencies i.e. below 25 MHz. Further the value of external capacitor should be sufficiently larger than parasitic capacitor and maximum values of bias current I_{B2} should be 320 µA.

To study the time domain behavior, input signal comprised of two frequencies of 5 MHz and 20 MHz is applied. Signal amplitude was 50 mV each. The transient response with its spectrum for input and output is shown in Fig. 13, which clearly shows that the 20 MHz signal is significantly attenuated. The proposed circuit is also tested to judge the level of harmonic distortion at the output of the signal. The %THD result is shown in Fig. 14 which shows that the output distortion is low and within acceptable limit of 5% [18] up to about 225 mV.

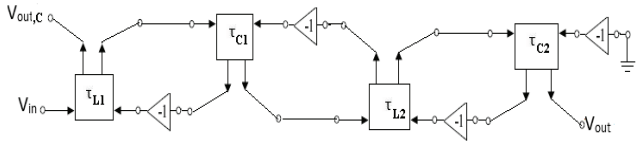


Fig. 9. Wave equivalent of prototype filter.

Transistors	Aspect ratio (W(μm)/L(μm))
M_1, M_4, M_9, M_{11}- M_{15}, M_{30} – M_{31}	3/0.25
M_2, M_3, M_5, M_6	1/0.25
M_7 - M_8, M_{20} – M_{23}, M_{26}, M_{28} – M_{29}	5/0.25
M_{10}	12.5/0.25
M_{16} – M_{17}	8/0.25
M_{18} – M_{19},	5/0.25
M_{24} – M_{25},	5/0.25
M_{27}	4.35/0.25

Tab. 2. Aspect ratio of various transistors.

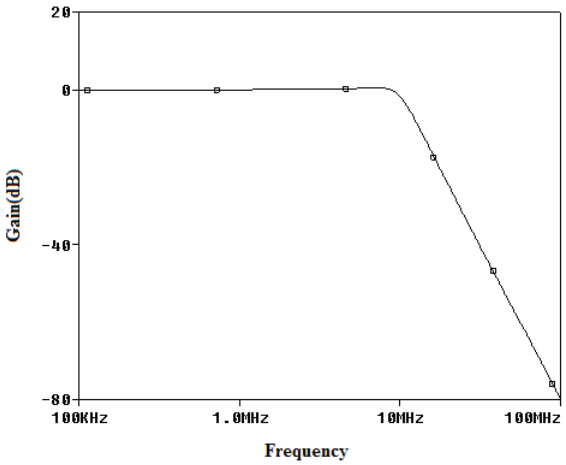


Fig. 10. Frequency response of 4th order low pass filter.

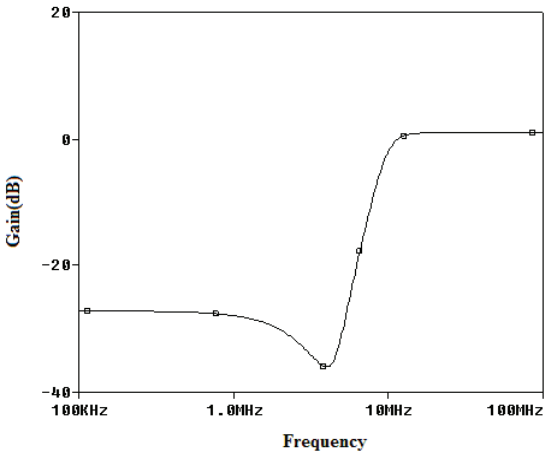
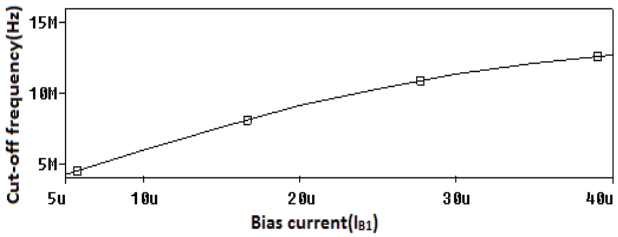


Fig. 11. Frequency response of complementary high pass filter.



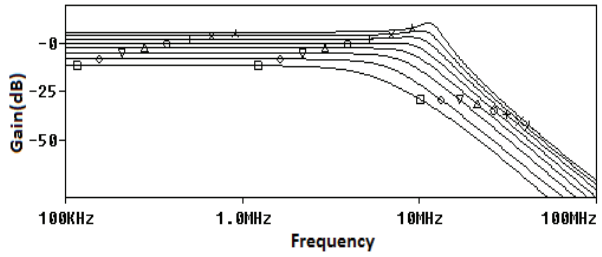
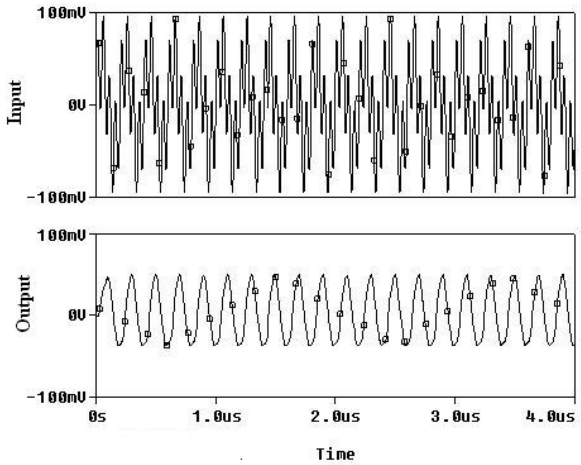
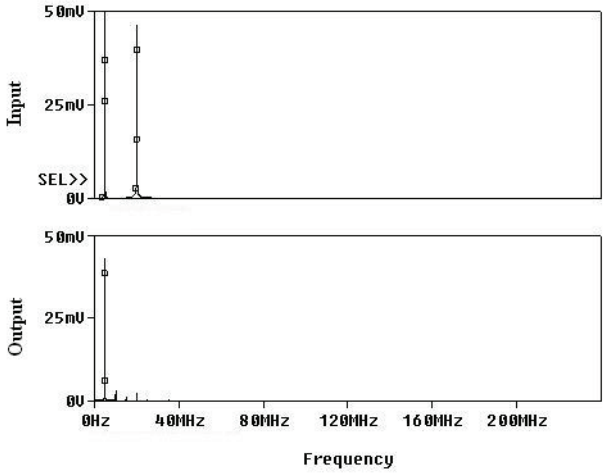


Fig. 12. Demonstration of electronic tunability.



(a)



(b)

Fig. 13. Transient response (a) input and output signals (b) Spectrum of input and output signals.

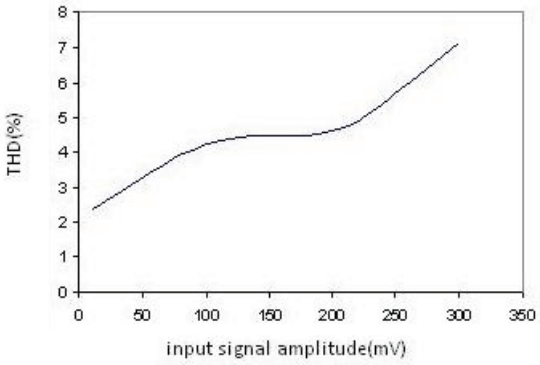


Fig. 14. Variation of % THD with input signal amplitude.

6. Conclusion

New DVCCCTA based high order voltage mode filter based on wave method is presented. The DVCCCTA based series inductor wave equivalent is proposed as it is the basic building block which is then configured for other passive element realization by making appropriate connections. The proposed structure uses grounded capacitors and possesses electronic tunability of cutoff frequency. The proposed approach is verified for a 4th order low pass filter through SPICE simulation using 0.25 µm CMOS technology parameters.

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