# Lossy/Lossless Floating/Grounded Inductance Simulation Using One DDCC

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**Abstract.** *In this work, we present new topologies for realizing one lossless grounded inductor and two floating, one lossless and one lossy, inductors employing a single differential difference current conveyor (DDCC) and a minimum number of passive components, two resistors, and one grounded capacitor. The floating inductors are based on ordinary dual-output differential difference current conveyor (DO-DDCC) while the grounded lossless inductor is based one a modified dual-output differential difference current conveyor (MDO-DDCC). The proposed lossless floating inductor is obtained from the lossy one by employing a negative impedance converter (NIC). The non-ideality effects of the active element on the simulated inductors are investigated. To demonstrate the performance of the proposed grounded inductance simulator as an example, it is used to construct a parallel resonant circuit. SPICE simulation results are given to confirm the theoretical analysis.*

## Keywords

DDCC, MDO-DDCC, inductance simulator, resonant circuit.

## 1. Introduction

An inductor is a required element in circuit design and can be used in many blocks such as filters, oscillators, phase shifters and impedance matching circuitry. Monolithic printed spiral inductors suffer from substrate resistive losses and capacitive couplings. In addition, process tolerances lead to component variations, which cannot easily be tuned in the passive case [1]. Therefore, in recent years, synthetic inductor realizations have been focused on the field of the integrated circuit design due to the resulting reduction in size and cost effectiveness. On the other hand, although on chip inductors in spiral form is a new research area, their values are very small, usually in the order of 1 nH, and their quality factors are limited [2]. Thus active circuits, which simulate the characteristic of a passive inductor, have received considerable attention. This attention is widely focused on the inductance simulation using different high-performance active building blocks such as Operational Transconductance Amplifiers (OTAs) [3], Current Feedback Operational Amplifiers (CFOAs) [4], Four-Terminal Floating Nullors (FTFNs) [5], Current Differencing Buffered Amplifiers (CDBAs) [6]-[7] and Current Conveyors (CCs) and their variants [8]-[18]. A literature survey shows that a large number of circuit realizations for lossless and lossy grounded and floating inductances based on CCs and their variants that have been proposed, in general, possess some weaknesses such as:

i) the use of an excessive number of active elements,

ii) excessive use of grounded and/or floating passive elements, and

iii) the use of ungrounded capacitors. It is worth noting that a circuit employing grounded capacitors has considerable advantages in integrated circuit (IC) implementation [2].

The proposed inductor topologies can be classified based on the number of active and passive elements employed and whether they realize a lossy or lossless kind of inductors. Most of these circuits employ two or more CCs to realize grounded inductance [9]-[12]. The proposed topologies in [13]-[15] employ a single CC but they do not realize pure inductances. Although the circuits reported in [16] and [17] realize pure inductance with only one modified inverting type second-generation current conveyor (MICCII) and a single minus-type modified inverting first-generation current conveyor (MICCI-), respectively, in addition to a grounded resistor both of the circuits employ a floating resistor and a floating capacitor. The five new lossless grounded inductance simulators recently presented in [18] employ only a single Fully Differential Second-Generation Current Conveyor (FDCCII), two grounded resistors and a grounded capacitor. Although these circuits seem to be the most attractive inductance simulators, the complicated CMOS structure of the FDCCII brings a drawback to them.

Differential difference current conveyor (DDCC) [19] and Differential voltage current conveyor (DVCC) [20] are proven to be useful in many voltage-mode (VM) and current-mode (CM) analog signal processing applications, such as VM filters, CM filters, mixed-mode filters, sinusoidal oscillators and immittance function simulators. The DDCC and DVCC allow CC applications to be extended to the domain of voltage differentiating functions. Therefore, such kinds of CCs give a higher degree of freedom to analog designers allowing the implementation of more functions using less active elements. A circuit with a minimum number of components is expected to simplify the design. A few circuits based on DDCC and DVCC for realizing grounded and/or floating synthetic inductances have been reported [20]-[22]. The circuit given in [20] involves two active elements. The circuits in [21] employ floating capacitor which is not desired in IC implementation [23]. In addition, the circuits in [22] use two or three active elements.

In this work, we present three new topologies for realizing a lossy floating inductor, a lossless floating inductor and lossless grounded inductor employing a single DDCC, two resistors, and one grounded capacitor. The floating inductors are based on ordinary DDCC with dual current output terminals (DO-DDCC) while the grounded lossless inductor is based on a modified dual-output differential difference current conveyor (MDO-DDCC). The proposed lossless floating inductor is obtained from the lossy one by employing a negative impedance converter (NIC). The DDCC is a non-tunable active element (its internal structure does not contain OTA with its transconductance $g_m$ or it is not based on current controlled CC, i.e. no intrinsic resistance $R_x$ is considered) and therefore, the proposed inductor simulators using two resistors and one grounded capacitor give the circuit solutions with minimum number of passive components. The proposed grounded inductance simulator circuit ideally provides lossless inductor realization. By taking into account non-ideal current and voltage gains of the MDO-DDCC, several kinds of grounded immittances can be obtained. Finally, using the proposed grounded inductance simulator, a parallel resonant circuit, as an example, is constructed. The SPICE simulations are given to illustrate the performance of the proposed synthetic inductance configurations.

## 2. Proposed Circuits

The DO-DDCC is an active element with terminals namely $Y_1$, $Y_2$, $Y_3$, X, Z+, and Z-. A symbolic representation of the DO-DDCC is shown in Fig. 1. The terminal voltage-current relationships of a DO-DDCC can be expressed as:

$$I_{Y1} = I_{Y2} = I_{Y3} = 0, \tag{1a}$$

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} + \beta_3 V_{Y3}, \tag{1b}$$

$$I_{Z+} = \alpha_1 I_X,\ I_{Z-} = -\alpha_2 I_X. \tag{1c}$$

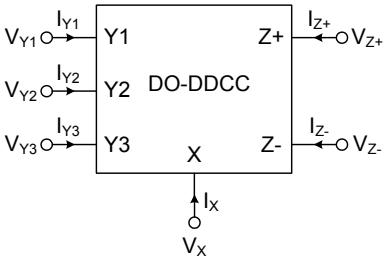


**Fig. 1.** Electrical symbol of the DO-DDCC.

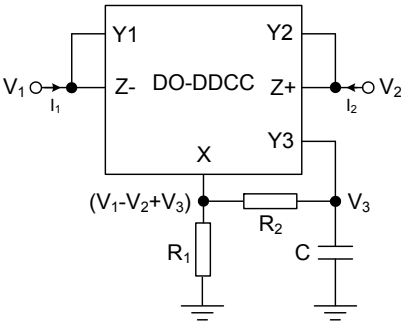


**Fig. 2.** Proposed floating lossy inductance simulator.

The Y terminals are high-impedance voltage inputs, Z terminals are high-impedance current outputs and X terminal exhibits a low-impedance. The $\beta_i$ ($i$ = 1, 2, 3) and $\alpha_j$ ($j$ =1, 2) represent the voltage and current gains of the DO-DDCC, respectively, which are ideally equal to unity.

The proposed lossy floating inductance simulator is shown in Fig. 2. It uses one DO-DDCC and three passive elements. Assuming ideal DO-DDCC and applying KCL at $V_1$ terminal of the circuit in Fig. 2, we obtain:

$$I_1 = \frac{V_1 - V_2 + V_3}{R_1} + \frac{V_1 - V_2}{R_2}. \tag{2a}$$

Applying KCL at terminal $V_3$, we get:

$$sCV_3 = \frac{V_1 - V_2 + V_3 - V_3}{R_2} \ \Rightarrow\ V_3 = \frac{V_1 - V_2}{sCR_2}. \tag{2b}$$

Substituting (2b) into (2a) yields:

$$I_1 = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{sCR_1R_2}\right)(V_1 - V_2). \tag{2c}$$

Considering that $I_2 = -I_1$, the following short-circuit admittance matrix is obtained:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \left(\frac{1}{R_{eq}} + \frac{1}{sL_{eq}}\right)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{3}$$

Thus, it can be observed that a lossy floating inductance with the value of $L_{eq} = CR_1R_2$ in parallel with a resistance with the value of $R_{eq} = R_1R_2/(R_1+R_2)$ is obtained from the circuit of Fig. 2.

Connecting the negative impedance convertor (NIC) given in Fig. 3(a) [24] or its equivalent circuit with DO-

DDCC given in Fig. 3(b) in series to $R_2$ in Fig. 2, and selecting $R_1 = R_2 = R$, a lossless floating inductance simulator can be obtained as illustrated in Fig. 4.

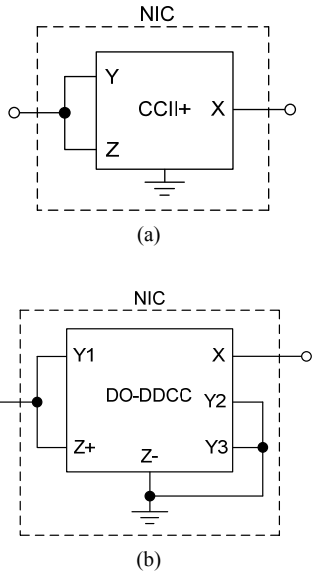


**Fig. 3.** (a) Negative impedance converter given in [23], (b) its equivalent using DO-DDCC.

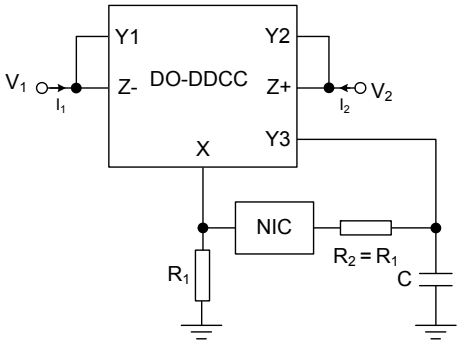


**Fig. 4.** Proposed floating lossless inductance simulator.

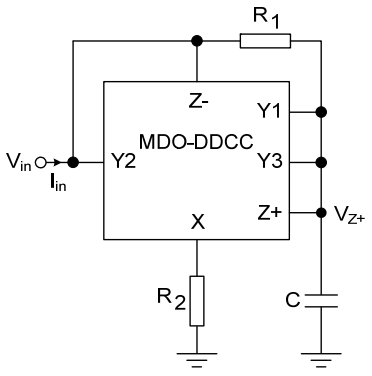


**Fig. 5.** Proposed grounded lossless inductance simulator.

The short-circuit admittance matrix of the circuit of Fig. 4 is given as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{sL_{eq}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{4}$$

Here, $L_{eq} = CR^2$. Note that by interchanging Z- and Z+ terminals of the DO-DDCC in Fig. 4, a negative lossless floating inductance with the value of $L_{eq} = -CR^2$ is obtained.

The proposed grounded lossless inductance simulator is based on a special type of the DO-DDCC which is called modified dual-output differential difference current conveyor (MDO-DDCC). The MDO-DDCC element has the same terminal voltage-current relations given in (1) except (1c) which is modified to:

$$I_{Z+} = 0.5\alpha_1 I_X,\ I_{Z-} = -\alpha_2 I_X. \tag{5}$$

The proposed grounded inductance simulator is shown in Fig. 5. It uses one MDO-DDCC and three passive elements. To find the input impedance of the circuit, a voltage source $V_{in}$ is connected to the $Y_2$-terminal of the MDO-DDCC of the proposed circuit. Applying KCL at $V_{in}$ terminal of the circuit in Fig. 5, we obtain:

$$I_{in} = \frac{-V_{in} + 2V_{Z+}}{R_2} + \frac{V_{in} - V_{Z+}}{R_1}. \tag{6a}$$

Setting $R_1 = R_2 = R$ in (6a) results in:

$$I_{in} = \frac{V_{Z+}}{R}. \tag{6b}$$

Similarly, writing KCL at terminal $V_{Z+}$ of the proposed circuit gives:

$$\frac{V_{in} - V_{Z+}}{R} = 0.5\left(\frac{V_{in} - 2V_{Z+}}{R}\right) + sCV_{Z+}, \tag{7a}$$

which is simplified to:

$$V_{Z+} = \frac{V_{in}}{2sCR}. \tag{7b}$$

By substituting (7b) into (6b) the following impedance is obtained:

$$Z_{in} = \frac{V_{in}}{I_{in}} = 2sCR^2 = sL_{eq}. \tag{8}$$

Hence,

$$L_{eq} = 2CR^2. \tag{9}$$

## 3. Non-Ideality Effects

Taking into account the non-idealities given in (1), the admittance matrix of (3) for the floating lossy inductance simulator given in Fig. 2 can be re-expressed by the following equations:

$$I_1 = \alpha_2\left(V_1\beta_1 - V_2\beta_2\right)\left(\frac{1}{R_p} + \frac{1}{sL_{eq} + R_s}\right), \tag{10a}$$

$$I_2 = -\frac{\alpha_1}{\alpha_2} I_1. \tag{10b}$$

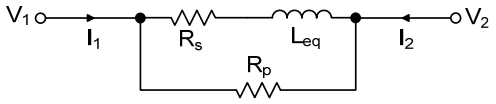


**Fig. 6.** The equivalent non-ideal impedance of the circuit given in Fig. 2.

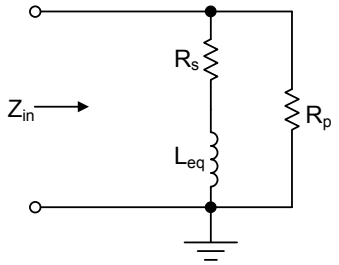


**Fig. 7.** The equivalent non-ideal impedance of the circuit given in Fig. 5.

Therefore, the circuit simulates an inductor ($L_{eq}$) with additional series resistor ($R_s$) all in parallel with the resistor ($R_p$) as shown in Fig. 6 where $L_{eq}$, $R_p$, and $R_s$ are found as:

$$L_{eq} = \frac{CR_1R_2}{1+(\beta_3-1)(1+R_1/R_2)}, \tag{11a}$$

$$R_p = \frac{R_1R_2}{R_1+R_2}, \tag{11b}$$

$$R_s = \frac{R_1(1-\beta_3)}{1+(\beta_3-1)(1+R_1/R_2)}. \tag{11c}$$

Taking into account the non-idealities of MDO-DDCC given in (1b) and (5) the equivalent non-ideal impedance of the grounded lossless inductance simulator shown in Fig. 5 is found to be:

$$Z_{in} = \frac{\left[2-\alpha_1(\beta_1+\beta_3)\right]R+2sCR^2}{2sCR(1-\alpha_2\beta_2)+(\beta_1-\beta_2+\beta_3)(2\alpha_2-\alpha_1)}. \tag{12}$$

Therefore, the circuit simulates an inductor ($L_{eq}$) in series with a resistor ($R_s$) all in parallel with a resistor ($R_p$) as shown in Fig. 7. Here, $L_{eq}$, $R_s$, and $R_p$ are found as:

$$L_{eq} = \frac{CR^2}{(2-\alpha_1\beta_2)\left[\alpha_2(\beta_1+\beta_3)-1\right]}, \tag{13a}$$

$$R_s = \frac{2-\alpha_1(\beta_1+\beta_3)}{(2-\alpha_1\beta_2)\left[\alpha_2(\beta_1+\beta_3)-1\right]}R, \tag{13b}$$

$$R_p = \frac{R}{1-\alpha_2\beta_2}. \tag{13c}$$

In this case, the quality factor $Q$ of the inductor shown in Fig. 5 can be approximately found as [25]:

$$Q_L(\omega) \cong \frac{\omega L_{eq}}{R_s} = \frac{\omega CR}{2-\alpha_1(\beta_1+\beta_3)}. \tag{14}$$

Note that the $\alpha_1$ and/or $\alpha_2$ parameters of the MDO-DDCC can be changed using the technique given in [26].

# 4. Simulation Results

The DO-DDCC and MDO-DDCC are simulated using the schematic implementation in Fig. 8 [19] with DC supply voltages equal to ±1.5 V and bias voltage equal to $V_{BB}$ = –0.9 V. The simulations are performed using SPICE program based on 0.35 μm TSMC CMOS technology parameters given in Tab. 1 [27]. The dimensions of the MOS transistors used in the DO-DDCC and MDO-DDCC implementations are given in Tab. 2. The non-ideal current and voltage gains of the DO-DDCC and MDO-DDCC are found to be as $\alpha_1 = 0.98$, $\alpha_2 = 1.05$, and $\beta_1 = \beta_2 = \beta_3 = 0.938$.

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.MODEL CMOSN NMOS ( LEVEL = 3 TOX = 7.9E-9
+ NSUB = 1E17 GAMMA = 0.5827871 PHI = 0.7 VTO = 0.5445549
+ DELTA = 0 UO = 436.256147 ETA = 0 THETA = 0.1749684
+ KP = 2.055786E-4 VMAX = 8.309444E4 KAPPA=0.2574081
+ RSH = 0.0559398 NFS = 1E12 TPG = 1 XJ = 3E-7
+ LD = 3.162278E-11 WD = 7.046724E-8 CGDO = 2.82E-10
+ CGSO = 2.82E-10 CGBO = 1E-10 CJ = 1E-3 PB = 0.9758533
+ MJ = 0.3448504 CJSW = 3.777852E-10 MJSW = 0.3508721 )
.MODEL CMOSP PMOS ( LEVEL = 3 TOX = 7.9E-9 NSUB = 1E17
+ GAMMA = 0.4083894 PHI = 0.7 VTO = -0.7140674
+ DELTA = 0 UO = 212.2319801 ETA = 9.999762E-4
+ THETA= 0.2020774 KP = 6.733755E-5 VMAX = 1.181551E5
+ KAPPA = 1.5 RSH = 30.0712458 NFS = 1E12 TPG = -1 XJ = 2E-7
+ LD = 5.000001E-13 WD = 1.249872E-7 CGDO = 3.09E-10
+ CGSO = 3.09E-10 CGBO = 1E-10 CJ = 1.419508E-3
+ PB = 0.8152753 MJ = 0.5 CJSW = 4.813504E-10 MJSW = 0.5 )
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**Tab. 1.** 0.35 μm TSMC CMOS transistor parameters [27].

| Transistor | W (μm) | L (μm) |
|---|---|---|
| M1-M4 | 1.4 | 0.7 |
| M5, M6 | 5.6 | 0.7 |
| M7, M8, M13-M15 | 14 | 0.7 |
| M8* | 7 | 0.7 |
| M9, M10 | 20.3 | 0.7 |
| M11, M12, M16-M18 | 58.1 | 0.7 |
| M12* | 29 | 0.7 |

* in case of MDO-DDCC only

**Tab. 2.** Transistor aspect ratios of the DO-DDCC and MDO-DDCC circuit shown in Fig. 8.

The proposed floating lossy inductance simulator circuit shown in Fig. 2 is simulated with the following passive element values: $R_1 = R_2 = 1$ kΩ and $C = 5$ nF, which results in $L_{eq} = 5$ mH in parallel with a resistance with the value of $R_{eq} = 500$ Ω. The ideal and simulated magnitude and phase responses where the second port of the floating simulator is grounded are shown in Fig. 9. For the floating and grounded lossless inductance simulators of Figs. 4 and 5 the following passive element values $R_1 = R_2 = 1$ kΩ and $C = 5$ nF ($C = 2.5$ nF in case of grounded inductance simulator) are selected, which results in $L_{eq} = 5$ mH. In the floating lossless inductance simulator realization, the NIC from the Fig. 3(b) was used. The ideal and simulated magnitude and phase responses are shown in Fig. 10. As it can be seen from Fig. 10, the magnitude of impedances increase with the frequency and the useful frequency ranges are for the floating lossless inductance simulator circuit about 10 kHz to 400 kHz and approximately 5 kHz to 700 kHz for the grounded lossless inductance simulator circuit. Wider operating frequency ranges can be achieved

using parasitic impedance reduction techniques proposed in [12] and [22]. In addition, based on (14) and using the designed values of passive elements listed above, the quality factor $Q$ of the grounded inductance simulator shown in Fig. 5 was also calculated. From Fig. 11 it can be seen that the $Q$ value at 100 kHz is equal to 9.73. It is worth noting here that such type of active inductors that are based on current conveyors and their variants are suitable for low and medium frequencies and they are not suitable for very high frequencies (higher than 1 GHz) [28]. In addition, from (14) it is obvious that high-$Q$ values for low and medium frequencies are hard to achieve. Although for RF and above frequencies spiral inductors are more suitable, an approach to increase the $Q$ value of the CMOS inductor simulators for RF circuits by using the NIC circuit is presented in [29].

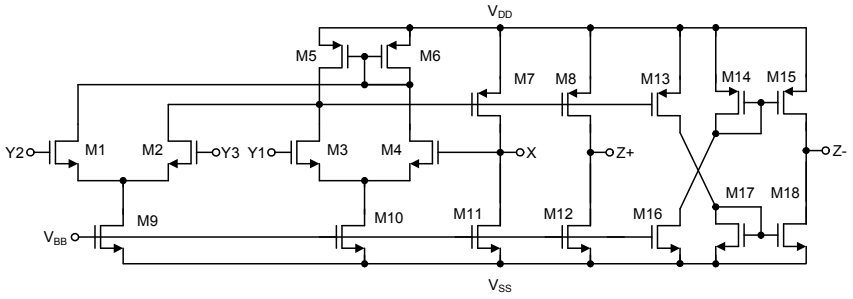


**Fig. 8.** A CMOS implementation for DO-DDCC and MDO-DDCC adopted from [19].

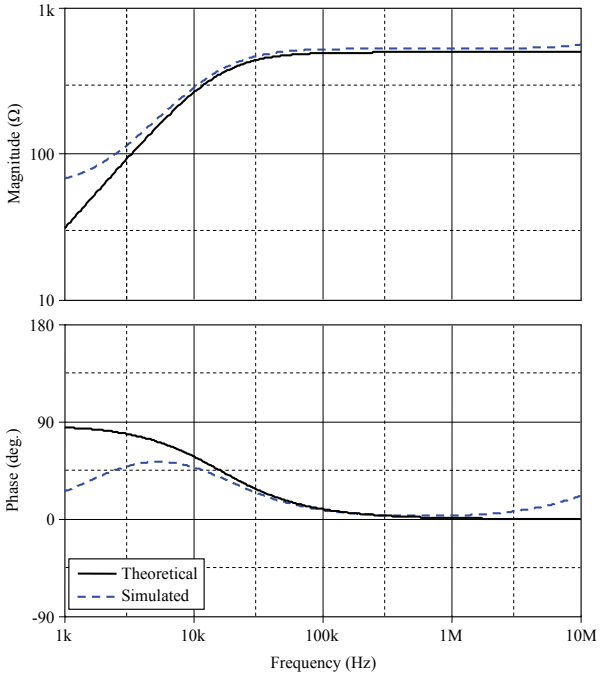


**Fig. 9.** The ideal and simulated magnitude and phase responses of the impedance of the proposed floating lossy inductance simulator in Fig. 2.

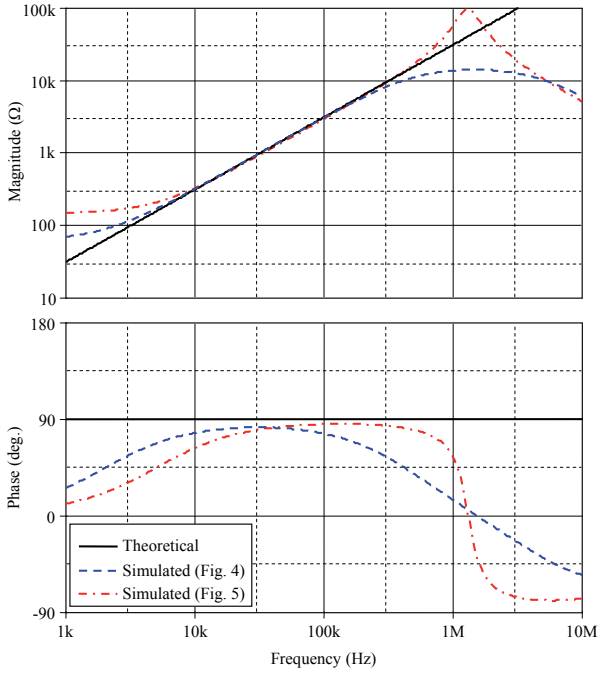


**Fig. 10.** The ideal and simulated magnitude and phase responses of the impedance of the proposed floating and grounded lossless inductance simulators in Figs. 4 and 5, respectively, for $L_{eq}$ = 5 mH.

The simulated waveforms of the voltage and current through the proposed grounded inductance simulator of Fig. 5, when a sinusoidal input current signal with 10 μA peak value at 100 kHz is applied are shown in Fig. 12. From Fig. 12 it can be observed that the phase difference between the current and voltage is 86°, which is close to the ideal value equal to 90°. The deviation is mainly caused by the non-idealities of the active element used and hence in practice a precise design of the MDO-DDCC should be considered to alleviate the non-ideal effects. The input dynamic range of the inductance simulator of Fig. 5 is verified by applying a sinusoidal input current signal at various amplitudes and observing the output voltage of the proposed inductance simulator. The total harmonic distortion (THD) of the output voltage vs. input current signal amplitude is shown in Fig. 13. Using INOISE and ONOISE statements, the noise behavior of the inductance simulator of Fig. 5 with respect to frequency has also been simulated, as it is shown in Fig. 14. The output voltage noise and equivalent input current noise at frequency of 100 kHz are calculated as 0.1038 μV/√Hz and 35.317 pA/√Hz, respectively.

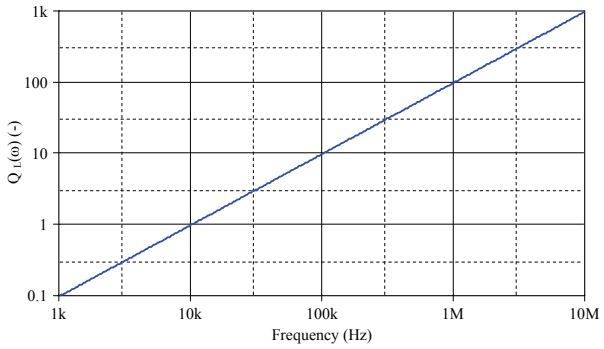


**Fig. 11.** Quality factor vs. frequency for the grounded inductance simulator of Fig. 5 calculated from (14).

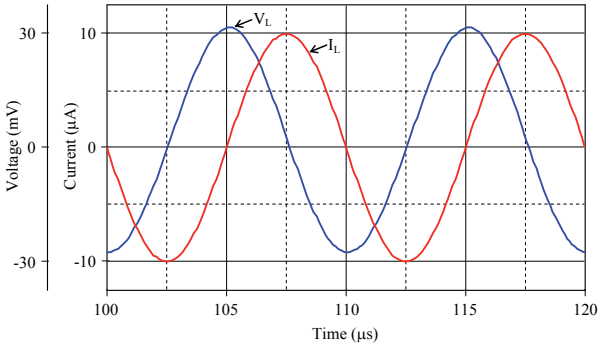


**Fig. 12.** Waveforms of voltage and current for the grounded inductance simulator of Fig. 5.

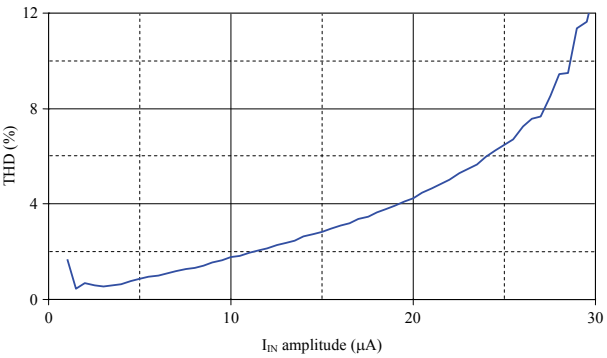


**Fig. 13.** THD of the inductance simulator's output voltage vs. input current signal amplitude.

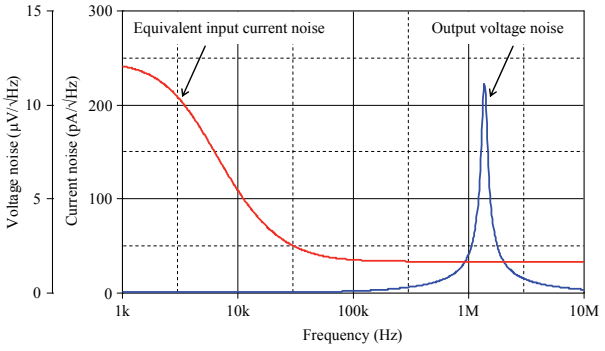


**Fig. 14.** Output and input referred noise responses of the grounded inductance simulator of Fig. 5.

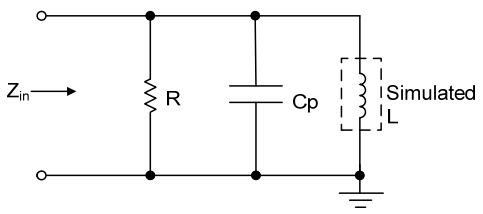


**Fig. 15.** Parallel resonant circuit used for simulation.

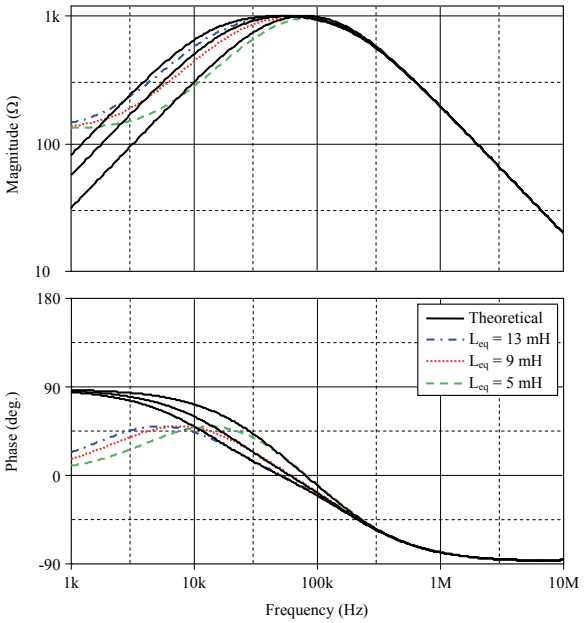


**Fig. 16.** The ideal and simulated magnitude and phase responses of the input impedance of the resonant circuit given in Fig. 15.

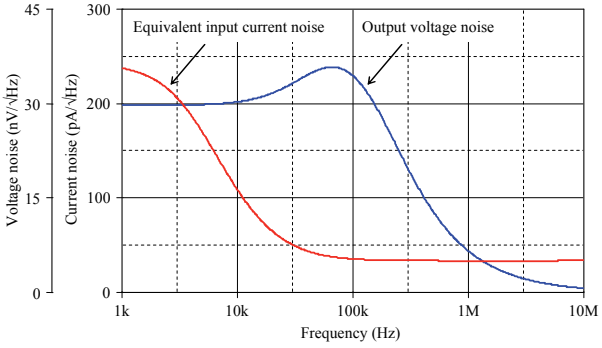


**Fig. 17.** Output and input referred noise responses of the parallel resonant circuit of Fig. 15 for Leq = 5 mH.

To further evaluate the performance of the proposed grounded lossless inductance simulator circuit shown in Fig. 5, we use it in the structure of a parallel resonant circuit shown in Fig. 15. The grounded inductance simulator circuit is simulated with the following passive element values: $R_1 = R_2 = 1$ kΩ and $C = 2.5$, 4.5 and 6.5 nF, which results in $L_{eq} = 5$, 9, and 13 mH, respectively. The remaining element values of passive elements are selected as $R = 1$ kΩ and $C_p = 0.8$ nF for resonance frequencies of 79.5, 59.3, and 49.3 kHz. Ideal and simulated magnitude

and phase responses of the input impedance responses of the parallel resonant circuit are given in Fig. 16. Similarly, the noise behavior of the parallel resonant circuit of Fig. 15 for $L_{eq}$ = 5 mH has also been simulated, as it is shown in Fig. 17. The output voltage noise and equivalent input current noise at frequency of 100 kHz are calculated as 34.401 nV/√Hz and 35.475 pA/√Hz, respectively.

From Figs. 9, 10 and 16, we can see that there are magnitude, resonance frequency, and phase deviations that are due the non-idealities of the simulated inductances as a result of the non-idealities of the DO-DDCC and MDO-DDCC.

## 5. Conclusion

In this paper, one lossy floating inductor, one lossless floating inductor and one lossless grounded inductor simulator topologies have been presented. The proposed topologies employ one DO-DDCC or one MDO-DDCC (lossless floating inductor includes one extra active device, NIC) together with two resistors and one grounded capacitor. The non-ideality effects of the used active element on the proposed inductors have been investigated. To demonstrate the validity of the proposed grounded inductor its behavior is tested in a parallel resonant circuit. The simulation results verify the theoretical analysis.

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