Novel Floating General Element Simulators Using CBTA

Umut Engin AYTEN[1], *Mehmet SAGBAS*[2], *Norbert HERENCSAR*[3], *Jaroslav KOTON*[3]

[1]Dept. of Electronics and Comm. Engineering, Yildiz Technical University, Esenler, 34222 Istanbul, Turkey
[2]Dept. of Electronics Engineering, Maltepe University, Maltepe, 34857 Istanbul, Turkey
[3]Dept. of Telecommunications, Brno University of Technology, Purkynova 118, 612 00 Brno, Czech Republic

ayten@yildiz.edu.tr, sagbas@maltepe.edu.tr, herencsn@feec.vutbr.cz, koton@feec.vutbr.cz

Abstract. *In this study, a novel floating frequency dependent negative resistor (FDNR), floating inductor, floating capacitor and floating resistor simulator circuit employing two CBTAs and three passive components is proposed. The presented circuit can realize floating FDNR, inductor, capacitor or resistor depending on the passive component selection. Since the passive elements are all grounded, this circuit is suitable for fully integrated circuit design. The circuit does not require any component matching conditions, and it has a good sensitivity performance with respect to tracking errors. Moreover, the proposed FDNR, inductance, capacitor and resistor simulator can be tuned electronically by changing the biasing current of the CBTA or can be controlled through the grounded resistor or capacitor. The high-order frequency dependent element simulator circuit is also presented. Depending on the passive component selection, it realizes high-order floating circuit defining as $V(s) = s^n AI(s)$ or $V(s) = s^{-n} BI(s)$. The proposed floating FDNR simulator circuit and floating high-order frequency dependent element simulator circuit are demonstrated by using SPICE simulation for 0.25 μm, level 7, TSMC CMOS technology parameters.*

Keywords

Frequency dependent negative resistor (FDNR), floating inductor, capacitance multiplier, floating element simulator circuit, current backward transconductance amplifier (CBTA), active networks.

1. Introduction

Floating immittance function simulators such as frequency dependent negative resistors (FDNRs), inductors, or capacitance multipliers are useful active building blocks (ABBs) for active filter and oscillator design, or cancellation of parasitic elements. Therefore, during the last few years they became a standard research topic. The first FDNR element was introduced by Bruton in 1969 [1] and it was designed using operational amplifiers. However, due to smaller dynamic range, narrow bandwidth, and higher power consumption of operational amplifiers, the current-mode (CM) active building block (ABB) design received considerable attention [2], [3] during the last decade. Although large number of ABBs listed in [3] emerged as an important class of circuits with exclusive properties that enable them to rival with their voltage-mode (VM) counterparts in wide range of applications, the floating FDNR realizations using these ABBs in [4]–[23] still suffer from the following weaknesses:

(i) they employ three or more ABBs, which enlarge the chip area [5]–[7], [11], [12], [15], [19], [21],

(ii) floating capacitor is used, therefore, the circuit is not suitable for fully integrated circuit design [6]–[13], [15], [16], [18], [20], [22], [23], or

(iii) the circuit cannot be tuned electronically by changing the biasing current [4], [5], [7], [8], [12], [14]–[18].

The most popular ABB in the above listed references is the second-generation current conveyor (CCII). In [5], the general floating impedance simulating circuit employs five plus-type CCIIs and five passive elements from which two are floating. In [6], [12], and [13], four CCII+s are used. Considering current-controlled CCIIs, in [6] and [13] resistorless electronically tunable FDNRs can be obtained, however, in both circuits floating capacitors are used. In other CCII-based versatile active circuits three [15] and two [16] ABBs are used. Unfortunately, the floating capacitors and non-tunable property of circuits are the drawbacks of these works. Compensation advantage of the first-generation CC over the CCII is shown in tunable circuits in [11]. Current feedback operational amplifiers (CFOAs) are also popular ABBs for floating FDNR design in [7] and [17]. In fact, the CFOA is a CCII+ followed by voltage buffer, hence, it does not offer internal tuning feature. Similarly, the differential voltage CC (DVCC) used in [4] and [14] also fits to the same group of ABBs. Although authors in [8] highlight the simplicity of their FDNRs, the disadvantages of operational amplifiers were already mentioned above. Compact tunable FDNR realizations employing floating capacitors and a single dual-X CCII (DXCCII) or low transistor count MOS transcapacitive stages are presented in [9] and [10], respectively. Similarly, a single active device called modified CFOA (MCFOA) and a minimum number of passive elements-based FDNR is shown in [18]. It is worth men-

tioning that in the literature some other versatile circuits exist that can realize a floating inductor, floating capacitor and floating resistor [24]. However, they are not listed above, since they do not allow floating FDNR design.

In recent publication [25], the concept and an implementation of circuit building block called current backward transconductance amplifier (CBTA) is introduced. It has proven to be a useful ABB in many VM and CM analog signal processing applications [25]–[31]. Considering these facts, in this study, a novel floating FDNR, inductor, capacitor, and resistor simulator circuit employing two CBTAs and three passive components is proposed, where all the passive elements are grounded. The circuit does not require any component matching conditions, and it has a good sensitivity performance with respect to tracking errors. Moreover, the proposed FDNR, inductance, capacitor, and resistor simulator can be tuned electronically by changing the biasing current of the CBTA. Furthermore, based on the passive component selection, the proposed circuit can be modified to high-order floating frequency dependent element.

2. Current Backward Transconductance Amplifier

The circuit symbol of CBTA is shown in Fig. 1, where p, n are input terminals, and w, z are the output terminals, respectively. This active element is equivalent to the circuit in Fig. 1(b), which involves dependent current source at p, n, and z terminals and voltage source at w terminal. The input impedances for the ideal CBTA are infinite at p, n, and z terminals and zero at w terminal. The CBTA terminal equations can be defined as follows [25]:

$$\begin{aligned} I_z &= g_m(s)(V_p - V_n), \quad V_w = \mu_w(s)V_z, \\ I_p &= \alpha_p(s)I_w, \quad I_n = -\alpha_n(s)I_w. \end{aligned} \tag{1}$$

In these equations $\alpha_p(s)$, $\alpha_n(s)$, and $\mu(s)$ are respectively the current and voltage gains and they can be expressed as $\alpha_p(s) = \omega_{\alpha p}(1-\varepsilon_{\alpha p})/(s+\omega_{\alpha p})$, $\alpha_n(s) = \omega_{\alpha n}(1-\varepsilon_{\alpha n})/(s+\omega_{\alpha n})$, $g_m(s) = g_o\omega_{gm}(1-\varepsilon_{gp})/(s+\omega_{gm})$, and $\mu_w(s) = \omega_w(1-\varepsilon_w)/(s+\omega_w)$ whereas $|\varepsilon_{\alpha p}| \ll 1$, $|\varepsilon_{\alpha n}| \ll 1$, $|\varepsilon_{gm}| \ll 1$, and $|\varepsilon_{\mu}| \ll 1$. Here, g_o is the DC transconductance gain. Also, $\varepsilon_{\alpha p}$ and $\varepsilon_{\alpha n}$ denote the current tracking errors, ε_{μ} denotes the voltage tracking error, ε_{gm} denotes transconductance error, and $\omega_{\alpha p}$, $\omega_{\alpha n}$, ω_{gm}, ω_{μ} denote corner frequencies. Note that, in the ideal case, the voltage and current gains are unity i.e. $\mu_w(s) = 1$ and $\alpha_p(s) = \alpha_n(s) = 1$ and frequency independent.

The CMOS implementation of the CBTA is given in Fig. 2, which was designed by interconnection of CCII and OTA shown in [32] and [33]. The dimensions of the MOS transistors used in the CBTA implementation are given in Tab. 1. In Fig. 2, the transconductance section is realized by the transistors $M_{21}-M_{34}$, which is formed by MOS coupled pair and current mirrors. We will assume that all MOS devices operate in the saturation region. Let us also assume that M_{21} and M_{22} are perfectly matched and the current mirrors have unity current gain. Then the output current i_o can be given by:

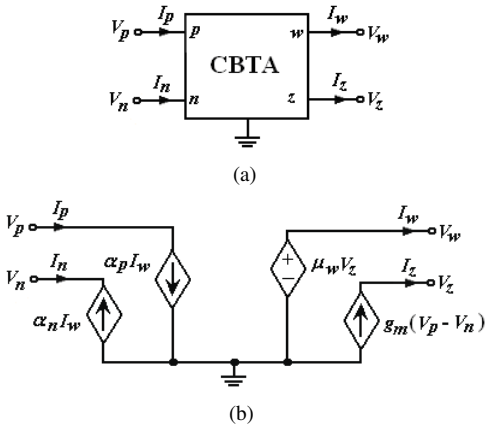

Fig. 1. (a) Block diagram of CBTA, (b) equivalent circuit of the CBTA.

PMOS Transistors	$W(\mu m)/L(\mu m)$
M_3-M_9	20/1
M_{15}	1/0.25
M_{16}, M_{17}, $M_{23}-M_{27}$, M_{29}	2.5/0.25
M_{28}, M_{30}	10/0.25
NMOS Transistors	$W(\mu m)/L(\mu m)$
M_1, M_2, M_{13}, M_{14}	10/1
$M_{10}-M_{12}$	2.5/1
M_{18}, M_{19}	0.5/0.25
M_{20}	2.5/0.25
M_{21}, M_{22}	2/0.25
M_{31}, M_{32}	2.25/0.25
M_{33}, M_{34}	10/0.25

Tab. 1. Dimensions of the CMOS transistors.

$$i_o = g_m v_{in} = \left(\sqrt{2I_B K}\right) v_{in} \tag{2}$$

where v_{in} is the differential input voltage ($v_{in} = v_p - v_n$), I_B is the bias current, $K = \mu C_{ox} W/2L$ is the transconductance parameter, μ is carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length of M_{21} and M_{22} transistors, respectively.

3. Proposed Floating FDNR, Inductor, Capacitor and Resistor Simulator Circuit

Consider floating admittance in Fig. 3(a) and simulator circuit in Fig. 3(b), the short circuit admittance matrices of these circuits can be respectively written as:

$$[y_{ij}] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = Y_f \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{3}$$

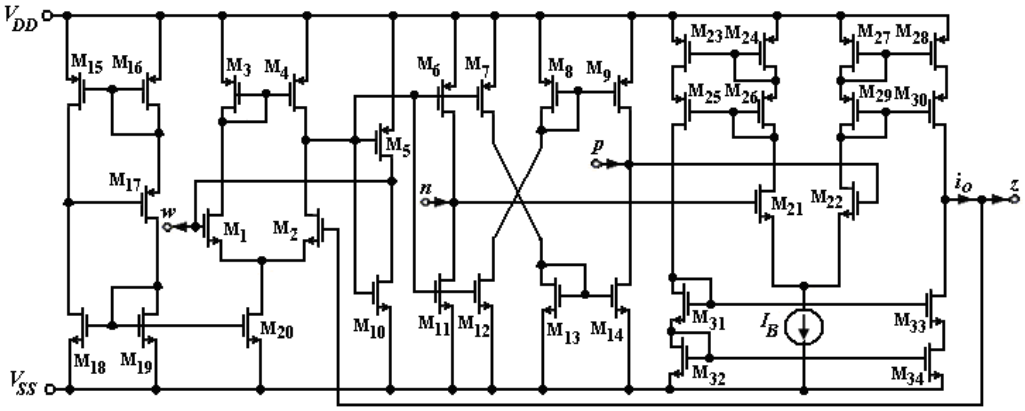

Fig. 2. CMOS implementation of CBTA.

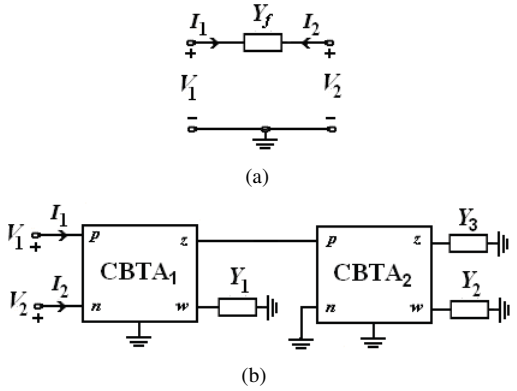

Fig. 3. (a) Floating admittance and (b) floating admittance simulator circuit.

$$[y_{ij}] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \frac{\alpha_1\mu_{w1}}{\alpha_2\mu_{w2}} \frac{g_{m1}Y_1Y_3}{g_{m2}Y_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \quad (4)$$

where $\alpha_p \approx \alpha_n = \alpha$ and $\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{ij} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$.

From (3) and (4) it is seen that depending on the choice of passive component a floating FDNR, inductor, capacitor and resistor simulator can be realized as follows:

(i) If $Y_1 = sC_1$, $Y_2 = G_2$, and $Y_3 = sC_3$ are selected, a floating FDNR is implemented as:

$$[Y_D] = \frac{\alpha_1\mu_{w1}}{\alpha_2\mu_{w2}} \frac{s^2 g_{m1}C_1C_3}{g_{m2}G_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \quad (5)$$

which represents a floating FDNR whose parameter is given by $D_f = \frac{\alpha_1\mu_{w1}}{\alpha_2\mu_{w2}} \frac{g_{m1}C_1C_3}{g_{m2}G_2}$. In ideal conditions, $D_f = \frac{g_{m1}C_1C_3}{g_{m2}G_2}$. Hence, the proposed circuit of Fig. 3(b) behaves as an ideal floating FDNR. By setting either $V_2 = 0$ or $V_1 = 0$, the proposed circuit can also be used as a grounded FDNR. Note that D_f can be tuned through g_{m1}, g_{m2}, G_2, C_1, or C_3.

(ii) If the admittances are chosen as $Y_1 = G_1$, $Y_2 = sC_2$, and $Y_3 = G_3$, the input admittance becomes:

$$[Y_L] = \frac{\alpha_1\mu_{w1}}{\alpha_2\mu_{w2}} \frac{g_{m1}G_1G_3}{sg_{m2}C_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \quad (6)$$

which represents a floating inductor whose inductance is given by $L_f = \frac{\alpha_2\mu_{w2}}{\alpha_1\mu_{w1}} \frac{g_{m2}C_2}{g_{m1}G_1G_3}$. In ideal conditions $L_f = \frac{g_{m2}C_2}{g_{m1}G_1G_3}$. By setting either $V_2 = 0$ or $V_1 = 0$, the proposed circuit can also be used as a grounded inductor.

(iii) If $Y_1 = sC_1$, $Y_2 = G_2$, and $Y_3 = G_3$ are chosen for the circuit depicted in Fig. 3(b), the short circuit admittance matrix of the floating capacitor is found to be:

$$[Y_C] = \frac{\alpha_1\mu_{w1}}{\alpha_2\mu_{w2}} \frac{sg_{m1}C_1G_3}{g_{m2}G_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \quad (7)$$

where $C_f = \frac{\alpha_1\mu_{w1}}{\alpha_2\mu_{w2}} \frac{g_{m1}C_1G_3}{g_{m2}G_2}$. In ideal conditions, $C_f = \frac{g_{m1}C_1G_3}{g_{m2}G_2}$. When the resistors and capacitor in Y_1 and Y_3 admittances are interchanged, we also obtain:

$$[Y_C] = \frac{\alpha_1\mu_{w1}}{\alpha_2\mu_{w2}} \frac{sg_{m1}G_1C_3}{g_{m2}G_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \quad (8)$$

which represents a floating capacitor whose parameter is given by $C_f = \frac{\alpha_1\mu_{w1}}{\alpha_2\mu_{w2}} \frac{g_{m1}G_1C_3}{g_{m2}G_2}$. In ideal conditions, $C_f = \frac{g_{m1}G_1C_3}{g_{m2}G_2}$. The value of grounded capacitor C_3 can be multiplied by a constant which can be tuned electronically by changing transconductance values of the CBTAs or can be controlled through grounded resistors. Hence, the proposed circuit can be used as a floating capacitance multiplier. Moreover, the proposed circuit can be used to convert a grounded capacitor to floating one.

(iv) Finally, choosing $Y_1 = G_1$, $Y_2 = G_2$, and $Y_3 = G_3$ for the circuit depicted in Fig. 3(b) is described by the following short circuit admittance matrix:

$$[Y_R] = \frac{\alpha_1\mu_{w1}}{\alpha_2\mu_{w2}} \frac{g_{m1}G_1G_3}{g_{m2}G_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \quad (9)$$

which represents a floating resistor whose resistance is given by $R_f = \frac{\alpha_2\mu_{w2}}{\alpha_1\mu_{w1}} \frac{g_{m2}G_2}{g_{m1}G_1G_3}$. In ideal conditions, $R_f = \frac{g_{m2}G_2}{g_{m1}G_1G_3}$.

Normalized active and passive sensitivities of D_f, L_f, C_f, and R_f are given by:

$$S^{y_{ij}}_{Y_1,Y_3,\alpha_1,\mu_{w1},g_{m1}} = -S^{y_{ij}}_{Y_2,\alpha_2,\mu_{w2},g_{m2}} = 1, \quad (10)$$

which is not higher than unity in magnitude. Thus, the proposed simulators offer low active and passive sensitivities.

4. Proposed High-Order Floating Frequency Dependent Element Simulator Circuit

In order to realize high-order floating frequency dependent element simulator circuit, the circuit given in Fig. 4, which was presented in [27] is used. Its short circuit admittance matrix can be written as:

$$\left[\ y_{ij}\ \right] = \begin{bmatrix} y_{11} & y_{12} \\ y_{11} & y_{12} \end{bmatrix} = \alpha_1\mu_{w1}\frac{g_{m1}Y_1}{Y_2}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \quad (11)$$

where $\alpha_p \approx \alpha_n = \alpha$ and $\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \left[\ y_{ij}\ \right]\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$.

The circuit in Fig. 3(a) can be used to replace Y_2 in Fig. 4, which will result in a cascade configuration given in Fig. 5, leading to a third-stage frequency dependent element simulator circuit described by the short circuit admittance matrice:

$$\left[\ y_{ij}\ \right] = \begin{bmatrix} y_{11} & y_{12} \\ y_{11} & y_{12} \end{bmatrix} = \frac{\alpha_1\alpha_3\mu_{w1}\mu_{w3}}{\alpha_2\mu_{w2}}\frac{g_{m1}g_{m3}Y_1Y_3}{g_{m2}Y_2Y_4}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}. \quad (12)$$

The general high-order frequency dependent element simulator circuit is given in Fig. 6 and its generalized non-ideal short circuit admittance matrices can be written as follows:

(a) If n is even:

$$\left[\ y_{ij}\ \right] = \frac{(\alpha_1\alpha_3\ldots\alpha_{n+1})(\mu_{w1}\mu_{w3}\ldots\mu_{w(n+1)})}{(\alpha_2\alpha_4\ldots\alpha_n)(\mu_{w2}\ldots\mu_{wn})} \frac{(g_{m1}g_{m3}\ldots g_{m(n+1)})(Y_1Y_3\ldots Y_{n+1})}{(g_{m2}g_{m4}\ldots g_{mn})(Y_2Y_4\ldots Y_n)}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \quad (13)$$

in ideal conditions:

$$\left[\ y_{ij}\ \right] = \frac{(g_{m1}g_{m3}\ldots g_{m(n+1)})(Y_1Y_3\ldots Y_{n+1})}{(g_{m2}g_{m4}\ldots g_{mn})(Y_2Y_4\ldots Y_n)}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}. \quad (14)$$

(b) If n is odd:

$$\left[\ y_{ij}\ \right] = \frac{(\alpha_1\alpha_3\ldots\alpha_n)(\mu_{w1}\mu_{w3}\ldots\mu_{wn})}{(\alpha_2\alpha_4\ldots\alpha_{n-1})(\mu_{w2}\ldots\mu_{w(n-1)})} \frac{(g_{m1}g_{m3}\ldots g_{mn})(Y_1Y_3\ldots Y_n)}{(g_{m2}g_{m4}\ldots g_{m(n-1)})(Y_2Y_4\ldots Y_{n-1})}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \quad (15)$$

in ideal conditions:

$$\left[\ y_{ij}\ \right] = \frac{(g_{m1}g_{m3}\ldots g_{mn})(Y_1Y_3\ldots Y_n)}{(g_{m2}g_{m4}\ldots g_{m(n-1)})(Y_2Y_4\ldots Y_{n-1})}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}. \quad (16)$$

From (13)–(15), high-order frequency dependent element can be obtained by choosing admittances Y. For example; for $n = 5$, if the capacitors are chosen as $Y_1 = sC_1$, $Y_3 = sC_3$, $Y_5 = sC_5$ and the resistors are chosen as $Y_2 = G_2$, $Y_4 = G_4$, $Y_6 = G_6$, the short-circuit admittance matrices can be found as follows:

$$\left[\ y_{ij}\ \right] = \frac{s^3(g_{m1}g_{m3}g_{m5})(C_1C_3C_5)}{(g_{m2}g_{m4})(G_2G_4G_6)}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \quad (17)$$

giving the third-order floating frequency dependent element simulator circuit. If n is chosen as 6, the 4^{th}-order floating frequency dependent element simulator circuit will be obtained. Hence, the circuit given in Fig. 6 realizes high-order floating frequency dependent resistor simulator circuit for n being even and high-order floating frequency dependent capacitor circuit for n being odd defined as $I = s^3EV$, $I = s^4FV, \ldots, I = s^nKV$.

If the resistors are chosen as $Y_1 = G_1, Y_3 = G_3, Y_5 = G_5$, and the capacitors are chosen as $Y_2 = sC_2, Y_4 = sC_4, Y_6 = sC_6$ for previous example $(n = 5)$ and the short circuit admittance matrices can be found as follows:

$$\left[\ y_{ij}\ \right] = \frac{(g_{m1}g_{m3}g_{m5})(G_1G_3G_5)}{s^3(g_{m2}g_{m4})(C_2C_4C_6)}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}. \quad (18)$$

The high-order floating frequency dependent inductor is obtained when n is odd. The high-order floating frequency dependent resistor is obtained when n is even and it is defined as $V = s^3MI, V = s^4NI, \ldots, V = s^nZI$.

The proposed high-order frequency dependent element can be used for active filter synthesis. According to the used active filter synthesis method, proposed n^{th}-order frequency dependent element circuit can be important such as the use of active and passive component count. It is the one of the most important advantages of the proposed nth-order frequency dependent element circuit. On the other hand, n^{th}-order active filter circuit can be realized using less active and passive components with using proposed n^{th}-order frequency dependent element circuit.

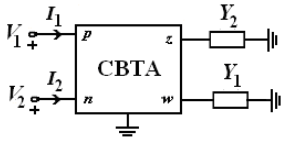

Fig. 4. The proposed circuit given in [27].

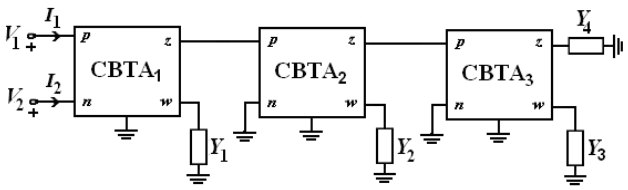

Fig. 5. Third-stage frequency dependent element.

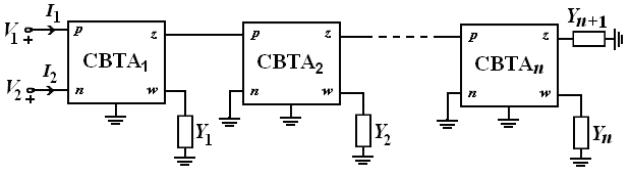

Fig. 6. High-order frequency dependent element.

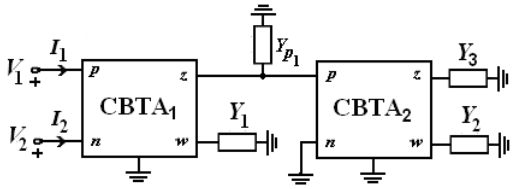

Fig. 7. The effect of the parasitic impedance between z and p terminals for first-order frequency dependent element.

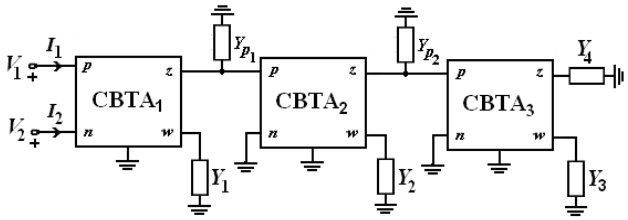

Fig. 8. The effect of the parasitic impedance between z and p terminals for third-stage frequency dependent element.

5. Effects of Parasitic Impedances, AC and DC Transfer Characteristics of CBTA

One of the parasitic impedance effects of the proposed circuit given in Fig. 3(b) is between the connection z terminal of the first CBTA and p terminal of the second CBTA. There has to be voltage in this connection and this voltage value depends on the impedances of the z and p terminals. In order to analyze the effect of this impedance, the circuit shown in Fig. 3(b) is redrawn as in Fig. 7, where Y_{p1} shows the common parasitic impedance between z and p terminals. Routine analysis gives the following short circuit admittance matrix:

$$[y_{ij}] = \frac{g_{m1}Y_1Y_3}{Y_{p1}Y_2 + g_{m2}Y_2} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}. \tag{19}$$

The simulation results, which are given in the next section show that the value of the Y_{p1} is approximately equal to zero. The general high-stage frequency dependent element is also considered for the effect of the parasitic impedance z and p terminals. For these reasons, the circuit shown in Fig. 3 is redrawn as in Fig. 8. Here, Y_{p1} and Y_{p2} represent the common impedances between z and p terminals. Routine analysis gives the following short circuit admittance matrix for the third-stage frequency dependent element:

$$[y_{ij}] = \frac{g_{m1}Y_1Y_{p2}Y_4 + g_{m1}g_{m3}Y_1Y_3}{Y_{p1}Y_{p2}Y_4 + g_{m3}Y_{p1}Y_3 + g_{m2}Y_2Y_4} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}. \tag{20}$$

Since, Y_{p1} and Y_{p2} are approximately equal to zero, which is demonstrated by using SPICE simulations, (20) is almost identical to (12). These results are also valid for the high-order frequency dependent element.

In order to analyze the parasitic resistances and capacitances of the CBTA, the non-ideal equivalent circuit shown in Fig. 9 can be used. The parasitic resistances and capacitances of the CBTA are found using SPICE simulations and listed in Tab. 2. The discrepancies between the theoretical results and SPICE simulations are not originating from the MOS transistor realization of CBTA, due to non-ideal characteristics of CBTAs mentioned in Eq. (1). To give an idea about the differences between the ideal and non-ideal cases, these non-idealities are found by using the SPICE simulations: corner frequencies are $\omega_{\alpha p} = 5300$ Mrad/s, $\omega_{\alpha n} = 6000$ Mrad/s, $\omega_{gm} = 5000$ Mrad/s, and $\omega_{\mu} = 3015$ Mrad/s. Errors of these gains are $\varepsilon_{\alpha p} = -0.014$, $\varepsilon_{\alpha n} = 0.003$, $\varepsilon_{gm} = 0.002$, and $\varepsilon_{\mu} = -0.0035$. For low-frequency application α_p, α_n, g_m, and μ_w can be assumed to be the constants with values $1-\varepsilon_{\alpha p} = 1.014$, $1-\varepsilon_{\alpha n} = 0.997$, $1-\varepsilon_{gm} = 0.998$, and $1-\varepsilon_{\mu} = 1.0035$, respectively. As a result, the maximum operating frequency of the CBTA is $f_{max} = \min\{f_{\alpha p}, f_{\alpha p}, f_{gm}, f_{\mu}\} \approx 480$ MHz. The frequency responses of the current gains $|\alpha_p| = |I_p/I_w|$, $|\alpha_n| = |I_n/I_w|$, the voltage gain $|\mu_w| = |V_w/V_z|$, and the transconductance gain $|g_m| = |I_z/(V_p - V_n)|$ are given in Fig. 10(a)–(c), respectively.

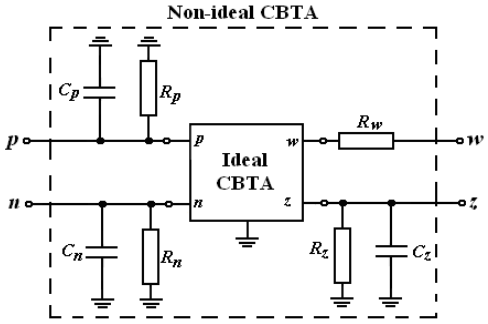

Fig. 9. Parasitic resistance and capacitance of the CBTA.

Parasitic Impedances	Values
R_p	53 kΩ
R_n	67 kΩ
R_z	403 kΩ
R_w	19.6 Ω
C_p	75 fF
C_n	990 fF
C_z	430 fF

Tab. 2. Parasitic impedances of the CBTA.

The DC characteristics such as plots of i_p against i_w, plots of v_w against v_z for the proposed CBTA are obtained. The DC current transfer characteristics of i_p and i_n against i_w, and DC transconductance transfer characteristic of i_z against $v_p - v_n$ when $g_m = 0.5$ mS, and DC voltage transfer characteristic of v_w against v_z are shown in Fig. 11.

6. Examples and Simulation Results

The CBTA is simulated using the schematic implementation shown in Fig. 2 with DC power supply voltages equal to $V_{DD} = V_{SS} = 1.5$ V, and bias current $I_B = 50$ μA, which according to (2) gives $g_m = 0.5$ mS. The simulations are performed using SPICE based on level 7 0.25 μm TSMC CMOS technology parameters. Main technology parameters used in

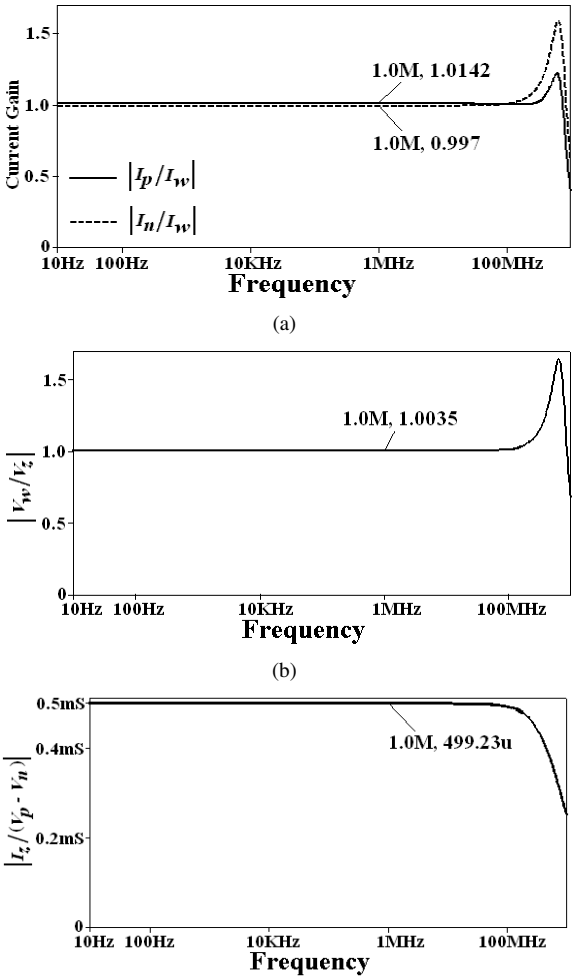

Fig. 10. Variation of the (a) current gains, (b) voltage gain, and (c) transconductance gain of the CBTA versus frequency.

SPICE simulations are given as follows: threshold voltage $V_{TH0} = 0.3894$ V, low field mobility $U_0 = 302.356$ cm^2/Vs, and gate oxide thickness $T_{ox} = 5.714$ nm for the NMOS transistor in addition to $V_{TH0} = 0.567$ V, $U_0 = 107.1614$ cm^2/Vs, and $T_{ox} = 5.714$ nm for the PMOS transistor.

The RLC band-pass filter in Fig. 12(a) was designed and simulated in order to verify the theory. The centre frequency and quality factor of this filter are $f_0 = 159.15$ kHz and $Q = 1$, respectively. Using magnitude scaling constant ($a = 10^9$) and variable impedance scaling method, i.e. dividing the impedance of each element in the Fig. 12(a) by a, the RLC filter is converted into CRD filter shown in Fig. 12(b). Transformed band-pass filter parameters in Fig. 12(b) are calculated using the formulas $C_k = 1/(aR_k)$, $R_k = aL_k$, and $D_k = C_k/a$. Realizing floating FDNR in Fig. 12(b) by the proposed circuit of Fig. 3(b) is obtained by taking $C_{11} = 1$ nF, $R_{12} = 1$ kΩ, $C_{13} = 1$ nF, and $g_{m1} = g_{m2} = 0.5$ mS. The magnitude and the phase characteristics of the filter are shown in Figs. 13(a) and 13(b), respectively. From Figs. 13(a) and 13(b) it appears that the theoretical and simulated results are in good agreement.

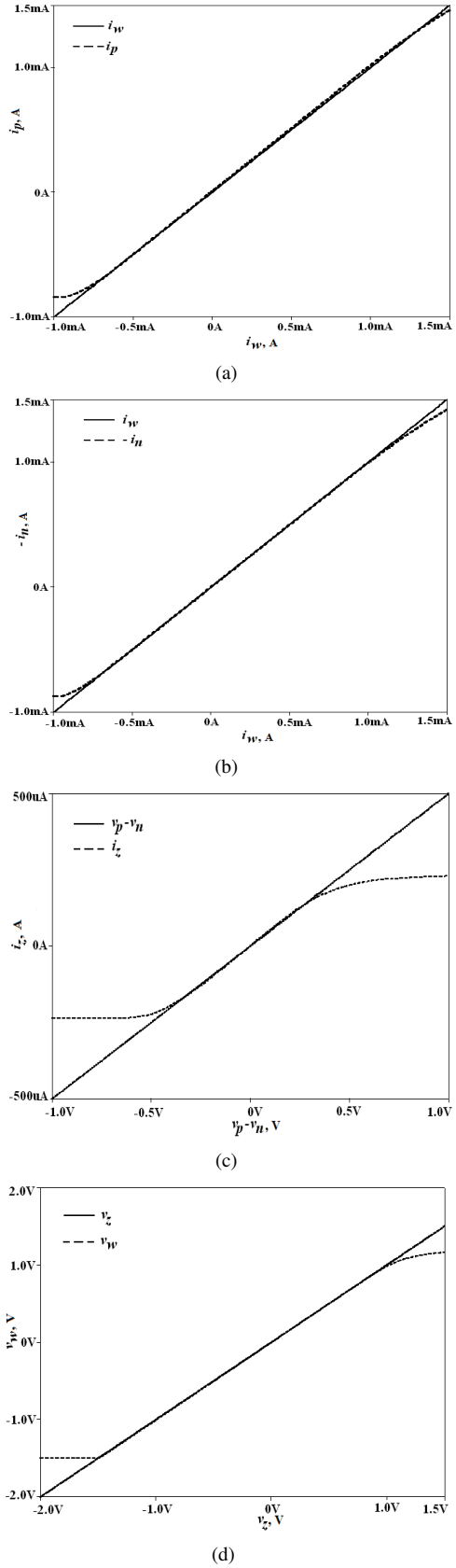

Fig. 11. (a) The current transfer characteristic $i_p = i_w$, (b) the current transfer characteristic $i_n = -i_w$, (c) the transconductance transfer characteristic $i_z = g_m(v_p - v_n)$, (d) the voltage transfer characteristic $v_w = v_z$.

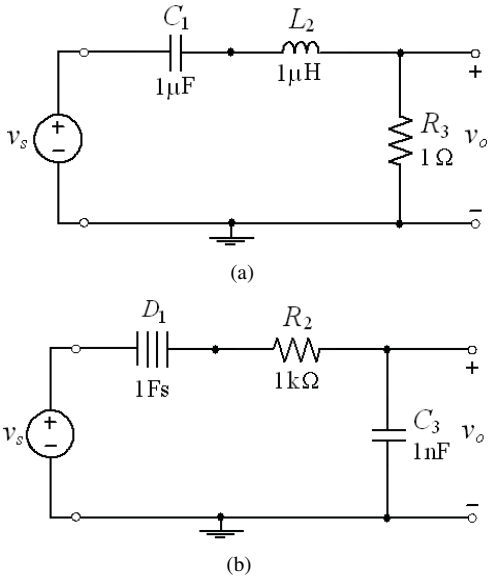

Fig. 12. (a) Band-pass filter with inductor, (b) transformed band-pass filter with FDNR.

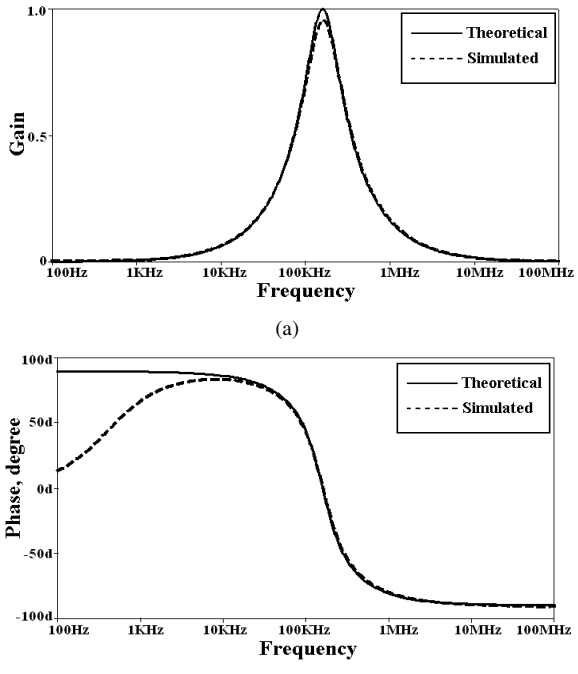

Fig. 13. (a) Gain characteristics, (b) phase characteristics of the theoretical and simulated band-pass filter in Fig. 12.

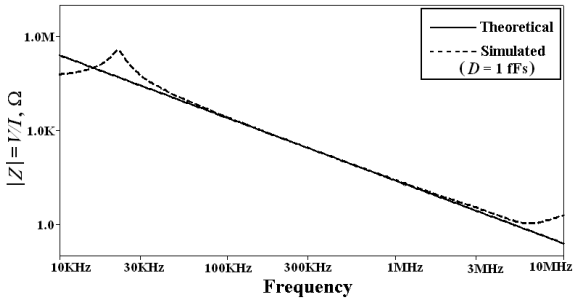

Fig. 14. The impedance values relative to frequency of the theoretical and simulated FDNR.

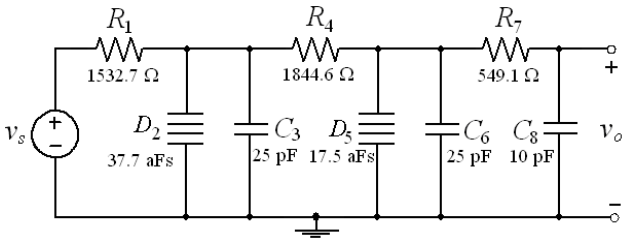

Fig. 15. Fifth-order low-pass filter with FDNR.

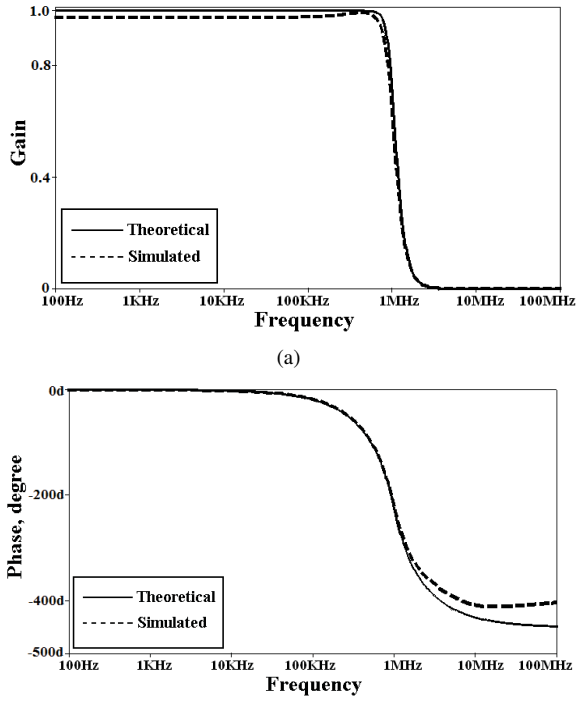

Fig. 16. (a) Gain characteristics, (b) phase characteristics of the theoretical and simulated low-pass filter in Fig. 15.

Fig. 14 shows that the magnitudes of the impedances of the theoretical FDNR and its simulator circuit can be made very close for a set of selected values over many decades; the difference between 40 kHz and 4 MHz is approximately equal to the theoretical data.

As another example a 5$^{\text{th}}$-order low-pass Butterworth filter in Fig. 15 has been designed at cut-off frequency $f_c = 1$ MHz. The passive component values are given on the circuit in Fig. 15. Realizing grounded FDNRs D_2 and D_5 by the proposed circuit of Fig. 3(b) are obtained by taking $C_{21} = 377$ pF, $C_{23} = 100$ pF, $R_{22} = 1$ kΩ, $g_{m1} = g_{m2} = 0.5$ mS for D_2, $C_{51} = 175$ pF, $C_{53} = 100$ pF, $R_{52} = 1$ kΩ for D_5. The magnitude and the phase characteristics of the filter are shown in Figs. 16(a) and 16(b), respectively.

Finally, to further confirm the behavior of the floating high-order element, a third-order high-pass filter shown in Fig. 17 was analyzed. In this circuit, the third-order floating element, defined as $V(s) = s^{-3}E_1 I(s)$, was used based on the

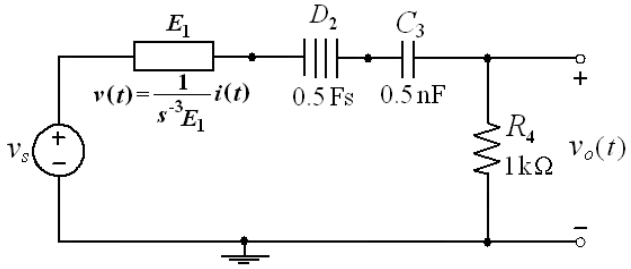

Fig. 17. Design example for high-order floating element.

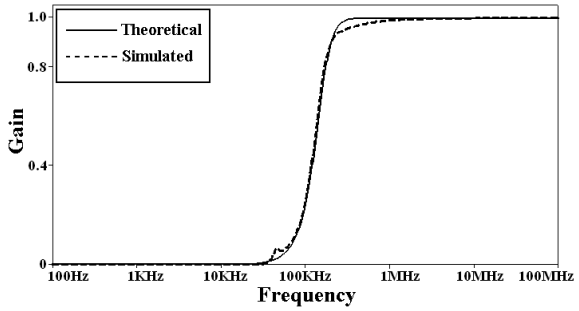

Fig. 18. Gain-frequency characteristics of the theoretical and simulated filter in Fig. 17.

high-order simulator circuit shown in Fig. 6. D_2 was obtained using the FDNR circuit shown in Fig. 3(b). In Fig. 17, E_1 was taken as 10^{-21} Fs^2. Therefore, the transfer function of the design example can be found as follows:

$$\frac{V_o(s)}{V_s(s)} = \frac{s^3}{s^3 + 2\cdot 10^6 s^2 + 2\cdot 10^{12} s + 10^{18}}, \qquad (21)$$

and the gain characteristic of the design example shown in Fig. 17 is given in Fig. 18, respectively.

To conclude, total power dissipation of the band-pass filter with presented FDNR simulator circuit in Fig. 12(b), the low-pass filter in Fig. 15 and the high-pass filter in Fig. 17 is approximately 13.7 mW, 27.3 mW, and 41.3 mW, respectively.

7. Conclusion

The design of floating FDNR, inductor, capacitor, and resistor simulators using two CBTAs is proposed in this paper. The presented floating component simulator does not require any component matching conditions and has low active and passive sensitivities. It uses grounded capacitors and resistors, which is more suitable for IC implementation. The values of FDNR, inductances, capacitances and resistances can be adjusted electronically using transconductance value of the CBTA without changing the values of the passive components. Furthermore, the proposed circuit can be modified to high-order floating frequency dependent element such as floating frequency dependent positive and negative capacitor, inductor and resistor. SPICE simulations prove the validity of the results obtained for the operation of the proposed circuit.

Acknowledgements

The research described in the paper was supported by the Czech Ministry of Education under research program MSM 0021630513 and Czech Science Foundation projects under No. GACR P102/09/1681, GACR 102/10/P561, GACR 102/11/P489, and BUT grant no. FEKT–S–11–15.

Authors also wish to thank the anonymous reviewers for their useful and constructive comments that helped to improve the paper.

A preliminary version of this paper has been presented at the 2011 34th International Conference on Telecommunications and Signal Processing (TSP) [29].

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About Authors...

Umut Engin AYTEN received the M.Sc. and Ph.D. degrees in Electronics and Communication Engineering from the Yildiz Technical University, Istanbul, Turkey, in 2003 and 2009, respectively. He is currently an Asst. Professor at Yildiz Technical University. His research interests are analog integrated circuits, active filters and analog signal processing.

Mehmet SAGBAS was born in Rize, Turkey, in 1977. He received his B.S. degree in Electronics Engineering from the Istanbul Technical University in 2000. He received his M.S. degree in Electronics Engineering from the Fatih University in 2004. He received his Ph.D. degree in Electronics Engineering from the Yildiz Technical University in 2007. He is currently an Asst. Professor at Maltepe University. His research interests are analog integrated circuits and analog signal processing.

Norbert HERENCSAR received the M.Sc. and Ph.D. degrees in Electronics & Communication and Teleinformatics from Brno University of Technology (BUT), Brno, Czech Republic, in 2006 and 2010, respectively. Currently, he is an Assistant Professor at the Dept. of Telecommunications, BUT. From September 2009 through February 2010 he was an Erasmus Exchange Student with the Dept. of Electrical and Electronic Engineering, Bogazici University, Istanbul, Turkey. His research interests include analog filters, current-mode circuits, tunable frequency filter design methods, and oscillators. He is an author or co-author of about 75 research articles published in international journals or conference proceedings. Dr. Herencsar is a member of IEEE, ACEEE, IAENG, and senior member of IACSIT.

Jaroslav KOTON received the M.Sc. an Ph.D. degree in electrical engineering from the Brno University of Technology, Czech Republic, in 2006 and 2009, respectively. He is currently an Assistant Professor at the Department of Telecommunications of the Faculty of Electrical Engineering and Communication of Brno University of Technology, Czech Republic. His current research is focused on linear- and non-linear circuit designing methods with current or voltage conveyors, and current active elements. He is an author or co-author of about 85 research articles published in international journals or conference proceedings. Dr. Koton is a member of IEEE and IACSIT.