

# New Universal Current-mode Biquad Using Only Three ZC-CFTAs

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**Abstract.** *The objective of this paper is to present a new universal current-mode biquad capable of providing all the five basic filter functions, namely, low pass (LP), band pass (BP), high pass (HP), band reject (BR) and all pass (AP) from the same configuration using only three Z - copy current follower transconductance amplifiers (ZC-CFTA) along with the provision of independent electronic tunability of the filter parameters  $\omega_0$  and  $Q_0$  (or bandwidth) through two separate DC bias currents while employing both grounded capacitors as desirable for integrated circuit implementation. The workability of the proposed structure is verified by PSPICE simulations based on CMOS implementation of the ZC-CFTA.*

## Keywords

Analog circuits, current mode circuits, Z-copy current follower transconductance amplifier (ZC-CFTA), universal filters, CMOS circuits.

## 1. Introduction

Recently, a new active element known as current follower transconductance amplifier (CFTA) has been introduced for analog circuit design in [1] and [2] and its various applications, such as those in realizing universal biquads and oscillators, have been presented in [3-6] and [10]. The universal biquad circuits of [3]-[5], although exhibit the important advantages of (i) realisability of all the five generic filter functions without requiring any component-matching conditions, (ii) independent electronic tunability of the filter parameters  $\omega_0$  and  $Q_0$ , and (iii) employment of both grounded capacitors as preferred for IC implementation, but suffer from the drawback of employing four CFTAs (which is more than the minimum number of CFTAs actually necessary i.e. three). On the other hand, the circuit proposed in [6] accomplishes the advantages (i)-(iii) above with only three CFTAs but suffers from the drawbacks of (a) realizing neither a voltage mode nor a current mode but instead a transadmittance mode biquad

(with voltage input and current outputs) and (b) needing an additional resistor also (apart from two grounded capacitors).

The object of this paper is to present a new ZC-CFTA-based universal biquad which offers all the three advantages (i)-(iii) quoted above like the circuits of [3]-[6], but by contrast, offers following advantages: (i) unlike the circuits of [3]-[5], which need four CFTAs, the new circuit needs only three CFTAs; (ii) unlike the circuit of [6] which needs an additional resistor, the new circuit does not require any additional resistor; (iii) unlike the circuit of [6], which is neither a VM nor a CM, the new circuit realizes all the five standard filter responses in proper current mode (CM). The proposed new circuit provides an additional advantage of the tuning of BW without disturbing angular frequency  $\omega_0$  in comparison to the biquad of [7] which although uses only two Z-copy current inverter transconductance amplifiers (ZC-CITAs) (which are almost the same as ZC-CFTAs) but does not offer this advantage. The workability of the proposed structure has been confirmed by PSPICE simulations.

## 2. Z-copy Current Follower Transconductance Amplifier (ZC-CFTA)

The symbolic representation and the equivalent circuit of the ZC-CFTA are shown in Fig. 1.

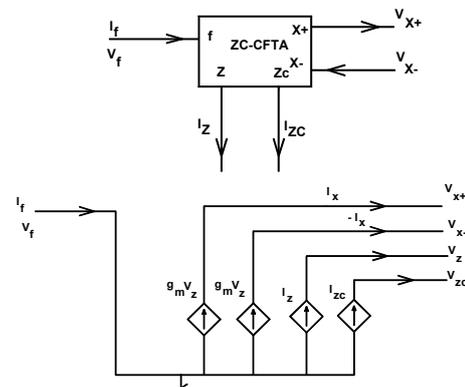


Fig. 1. ZC-CFTA: symbolic representation and equivalent circuit.

The ZC-CFTA is characterized by the following set of equations

$$V_f = 0, \quad i_z = i_{zc} = i_f, \quad i_{x+} = g_m V_z, \quad i_{x-} = -g_m V_z. \quad (1)$$

According to the above equations and equivalent circuit of Fig. 1, the input current  $i_f$  is transferred by the current follower to z terminal and the voltage drop at the terminal z is transformed into currents  $i_{x+}$  and  $i_{x-}$  at the terminals x+ and x- respectively using transconductance  $g_m$ , which is electronically-controllable by an external bias current. The copy of z terminal current is conveyed to zc

terminal. An exemplary CMOS implementation of the ZC-CFTA is shown in Fig. 2, which has been obtained by an appropriate modification of the structure published earlier in [4]. The transconductance  $g_m$  of the ZC-CFTA is given by

$$g_m = \sqrt{I_{set} \mu_0 C_{ox} (W/L)} \quad (2)$$

where  $I_{set}$  controls the transconductance  $g_m$ ,  $\mu_0$  is free electron mobility of channel,  $C_{ox}$  is the gate oxide capacitance per unit area as  $W/L$  is the aspect ratios of the identical MOSFETs  $M_{13}$  and  $M_{14}$  forming the differential pair.

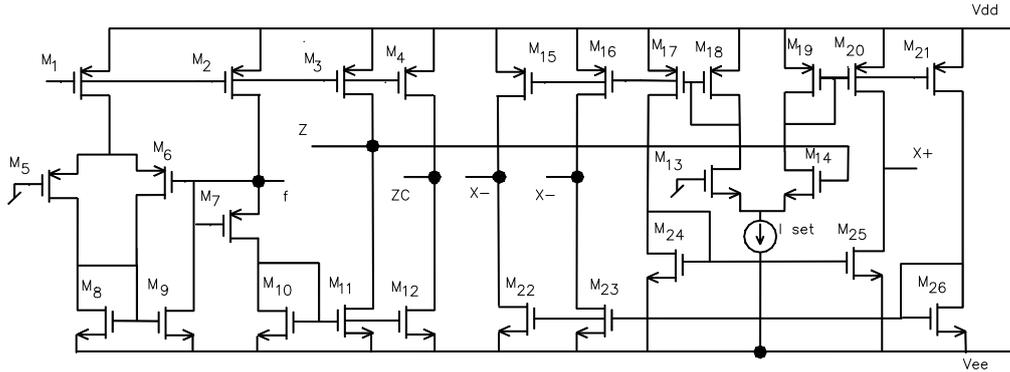


Fig. 2. An exemplary CMOS implementation of the ZC-CFTA.

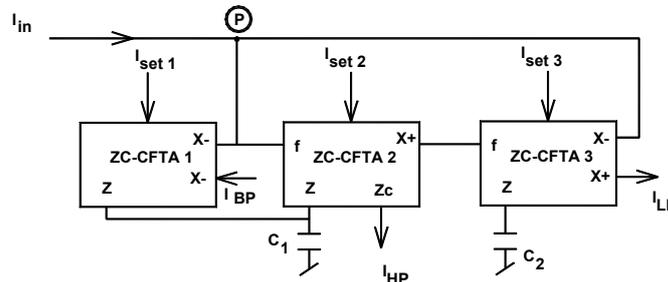


Fig. 3. New current mode universal biquad configuration using ZC-CFTAs.

### 3. Proposed Universal Biquad Employing only Three ZC-CFTAs

The proposed circuit is shown in Fig. 3. An analysis of the proposed circuit of Fig. 3 reveals the following current transfer functions

$$\frac{I_{BP}}{I_{in}} = \frac{-s \left( \frac{g_{m1}}{C_1} \right)}{D}, \quad (3)$$

$$\frac{I_{LP}}{I_{in}} = \frac{\left( \frac{g_{m2} g_{m3}}{C_1 C_2} \right)}{D}, \quad (4)$$

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{D}. \quad (5)$$

Adding the output currents  $I_{LP}$  and  $I_{HP}$ , one obtains  $I_{BR} = I_{LP} + I_{HP}$  which is given by

$$\frac{I_{BR}}{I_{in}} = \frac{s^2 + \left( \frac{g_{m2} g_{m3}}{C_1 C_2} \right)}{D}. \quad (6)$$

Lastly, adding  $I_{LP}$ ,  $I_{BP}$  and  $I_{HP}$  to get  $I_{AP} = I_{LP} + I_{HP} + I_{BP}$ , one obtains

$$\frac{I_{AP}}{I_{in}} = \frac{s^2 - s \left( \frac{g_{m1}}{C_1} \right) + \left( \frac{g_{m2} g_{m3}}{C_1 C_2} \right)}{D} \quad (7)$$

where  $D$  is given by

$$D = s^2 + s \left( \frac{g_{m1}}{C_1} \right) + \frac{g_{m2} g_{m3}}{C_1 C_2}. \quad (8)$$

It is, thus, seen that the proposed circuit is capable of realizing all the five basic functions, without requiring any component-matching or realization conditions.

From (3)-(8), the various filter parameters are given by

$$\omega_0 = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}}, \quad (9)$$

$$BW = \left(\frac{g_{m1}}{C_1}\right), \quad Q_0 = \frac{1}{g_{m1}} \sqrt{\frac{C_1g_{m2}g_{m3}}{C_2}} \quad (10)$$

whereas  $H_0$  is unity in all the cases.

It is clear from (9) and (10) that  $\omega_0$  can be tuned independently of BW in case of band pass and notch filter, former by  $g_{m2}$  and /or  $g_{m3}$  and the later by  $g_{m1}$ , while keeping the gain constant.

In order to attain all the five filter outputs simultaneously, one requires ZC-CFTA1 with two more outputs of X- type, ZC-CFTA2 with two more ZC outputs and ZC-CFTA3 with two more X+ type outputs.

It is, thus, seen that the proposed circuit employs one less active building block (ABB) in comparison to the universal biquads published earlier in [3]-[6] and yet exhibits all the properties of the earlier circuits, in that, it realizes all the five basic filter functions with electronic tunability of two parameters<sup>1</sup> namely,  $\omega_0$  and  $Q_0$  (or bandwidth), offers ideally zero input impedance and explicit current outputs at high impedance nodes in all cases while employing both grounded capacitors as preferred for IC implementation.

### 4. Sensitivity Analysis

The effect of changes in active/passive element values on the various filter parameters is determined by evaluating sensitivity coefficients which are found to be as follows

$$S_{g_{m2}}^{\omega_0} = S_{g_{m3}}^{\omega_0} = -S_{C_2}^{\omega_0} = -S_{C_1}^{\omega_0} = \frac{1}{2}, \quad (11)$$

$$S_{g_{m1}}^{BW} = -S_{C_1}^{BW} = 1, \quad (12)$$

$$S_{g_{m1}}^{Q_0} = -1, \quad (13)$$

<sup>1</sup> The independent control of gain may also be achievable if the circuit is modified as shown in Fig. 4 by adding one more CFTA along with an additional resistor R connected from its Z terminal to ground with input  $I_{in}$  applied at terminal f of this additional CFTA and its output x+ connected at node P of the circuit, with  $I_{set0}$  being the external DC bias current for this CFTA. In this case, the grounded resistor R can be realized by a simple two-MOSFET-resistor [8] to obtain a version suitable for CMOS implementation. With this modification, the gain factor  $H_0$  of all the realized filters can also be independently tuned by this additional bias current  $I_{set0}$ . It is worth pointing out that for voltage mode circuits, an interesting method of achieving gain control has been outlined in [9].

$$S_{g_{m3}}^{Q_0} = S_{g_{m2}}^{Q_0} = -S_{C_2}^{Q_0} = S_{C_1}^{Q_0} = \frac{1}{2}. \quad (14)$$

From (11)-(14) it is clear that all the sensitivities of the various parameters of the filters realized from the proposed configuration are very low.

### 5. Effect of Main Parasitic Impedances and Non-idealities

For more accurate analysis, the effects of main parasitic impedances and non idealities are to be taken into account. The model for ZC-CFTA including various parasitics is shown in Fig. 5. In case of non-ideal ZC-CFTA, relationships of current and voltages given in equation (1) can be rewritten as

$$V_f = 0, \quad i_z = i_{zc} = \alpha i_f, \quad i_{x+} = \beta g_m V_z, \quad i_{x-} = -\beta g_m V_z. \quad (15)$$

where  $\alpha = 1 - \epsilon_i$  and  $\epsilon_i$  ( $|\epsilon_i| \ll 1$ ) is the current tracking error from f to Z and ZC terminals. The transconductance inaccuracy factor from Z to X+/- terminal is denoted by  $\beta$ .

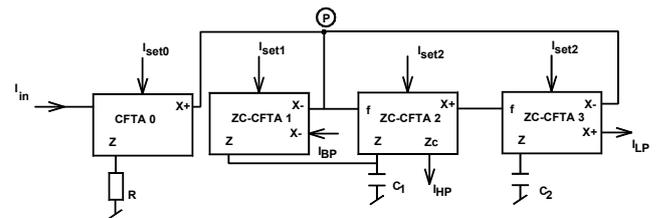


Fig. 4. Modified structure to obtain independent control of gain also.

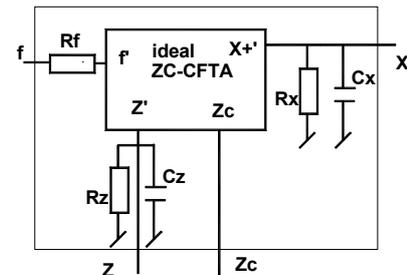


Fig. 5. Model of ZC-CFTA including parasitic elements.

From Fig. 5 it is clear that the parasitic resistance  $R_x$  and the parasitic capacitance  $C_x$  appear between the high impedance X+/- terminal and ground. To eliminate the effect of these parasitic impedances in the proposed circuit of Fig. 3, ZC-CFTA2 and ZC-CFTA3 should be designed to have a very low input parasitic resistance  $R_f$ . Ideally, the value of  $R_f$  is zero and terminal f is virtually grounded. Since these parasitic impedances are connected between true ground and virtual ground, these are, therefore almost ineffective.

The parasitic impedances  $R_z$  and  $C_z$  appear between high impedance Z terminal and ground as shown in Fig. 5.

The effect of above mentioned parasitic impedances consists in adding the  $R_z$  parasitic resistance at terminal Z and increasing the working capacitances  $C_1$  and  $C_2$  to  $C_1'$  and  $C_2'$  respectively by absorbing the parasitics as addition to

these external capacitances. Non ideality of current gain parameter  $\alpha$ , transconductance inaccuracy factor  $\beta$ , parasitic resistances and capacitances at terminal Z, modify the current transfer function in equation (3) to

$$\frac{I_{BP}}{I_{in}} = \frac{-S \left( \frac{\alpha_2 \beta_1 g_{m1}}{C_1'} \right) - \frac{\alpha_2 \beta_1 g_{m1}}{C_1' C_2' R_{Z3}}}{S^2 + S \left( \frac{1}{C_2' R_{Z3}} + \frac{1}{C_1' R_{Z2}} + \frac{\alpha_2 \beta_1 g_{m1}}{C_1'} \right) + \frac{g_{m3} g_{m2}}{C_1' C_2'} \left( \frac{1}{R_{Z2}' R_{Z3} g_{m3} g_{m2}} + \frac{\alpha_2 \beta_1 g_{m1}}{g_{m3} g_{m2} R_{Z3}} + \beta_2 \beta_3 \alpha_3 \alpha_2 \right)} \quad (16)$$

where  $C_1' = C_1 + C_{z1} + C_{z2}$  , (17)

$$C_2' = C_2 + C_{z3} , \quad (18)$$

$$R_{z2}' = R_{z2} \parallel R_{z1} \quad (19)$$

and  $R_z$  and  $C_z$  are the parasitic resistance and capacitance appearing at terminal Z of respective number of ZC-CFTA. Natural frequency, bandwidth and gain for the circuit shown in Fig.3 are now modified to

$$\omega_0' = \sqrt{\frac{g_{m2} g_{m3}}{C_1' C_2'} \left( \beta_2 \beta_3 \alpha_3 \alpha_2 + \frac{1}{g_{m2} g_{m3} R_{z2}' R_{z3}} + \frac{\alpha_2 \beta_1 g_{m1}}{g_{m3} g_{m2} R_{z3}} \right)} \quad (20)$$

$$BW' = \frac{g_{m1}}{C_1'} \left( \alpha_2 \beta_1 + \frac{C_1'}{C_2' R_{z3} g_{m1}} + \frac{1}{R_{z2}' g_{m1}} \right) \quad (21)$$

$$H_0' = \frac{1}{1 + \frac{1}{\alpha_2 \beta_2 g_{m1}} \left( \frac{C_1'}{C_2' R_{Z2}'} + \frac{1}{R_{Z3}} \right)} \quad (22)$$

Since gain  $H_0$  (ideally unity) gets modified as  $H_0'$  and turns out to be dependent on  $g_{m1}$ , from the expression for  $H_0'$ , it is found that nonideally, the gain  $H_0'$  increases from -1.52 dB to -1.02 dB and then to 0.82 dB when  $I_{set1}$  is varied from 20  $\mu$ A to 60  $\mu$ A and then to 180  $\mu$ A. This explains the different values of the gain as observable in Fig. 7. The appearance of parasitic resistance  $R_{z3}$  changes the type of impedance at Z terminal of ZC-CFTA for the circuit of Fig. 3, which should be purely capacitive in character. The possible solution to this problem is to make the operating frequency  $\omega_0 > 1/(R_{z3} C_2)$ .

## 6. SPICE Simulation Results

The proposed biquad has been simulated in PSPICE using CMOS ZC-CFTA of Fig. 2 with component values:  $C_1 = C_2 = 16$  pF and DC power supply voltages taken as  $V_{cc} = 1.5$  V,  $V_{ee} = -1.5$  V and  $V_1 = 0.5$  V. The dimensions of the MOSFETs were taken as shown in Tab. 1. The simulation was carried out using TSMC 0.35 $\mu$ m CMOS technology parameters shown in Tab.2.

The tunability of  $f_0$  for band pass filter has been verified by the circuit of Fig. 3 designed for values of  $f_0$  as 1.157 MHz, 1.735 MHz, 2.268 MHz, by varying  $g_{m1}$ ,  $g_{m2}$

and  $g_{m3}$  simultaneously with the values of bias currents  $I_0$  (i.e  $I_0 = I_{set1} = I_{set2} = I_{set3}$ ) taken as 20  $\mu$ A, 60  $\mu$ A and 180  $\mu$ A respectively, at constant  $Q = 1$  (Fig. 6). The bandwidth values 1.348 MHz, 1.915 MHz, 2.45 MHz, were obtained by varying  $g_{m1}$  through the bias currents  $I_{set1}$  taken as 20  $\mu$ A, 60  $\mu$ A, and 180  $\mu$ A respectively and  $I_{set2} = I_{set3} = 180$   $\mu$ A for maintaining a constant center frequency of 2.286 MHz (see Fig. 7). The circuit is designed to obtain LP, BR, BP, HP and AP responses with  $f_0 = 1.1$  MHz and  $Q = 1$  (simulation results for the same are shown in Fig. 8 and Fig. 9).

Transistor type	Transistor name	W( $\mu$ m)	L( $\mu$ m)
PMOS	M <sub>5</sub> , M <sub>6</sub>	1.4	0.35
PMOS	M <sub>1</sub> - M <sub>4</sub>	2.8	0.35
PMOS	M <sub>7</sub>	2.71	0.35
PMOS	M <sub>15</sub> - M <sub>21</sub>	4	1
NMOS	M <sub>8</sub> - M <sub>12</sub>	0.7	0.35
NMOS	M <sub>13</sub> , M <sub>14</sub> , M <sub>22</sub> -M <sub>26</sub>	4	1

Tab. 1. Dimensions of CMOS transistors.

NMOS: Level= 3 T <sub>ox</sub> = 7.9E-9 NSUB = 1E17 GAMMA = 0.5827871 PHI = 0.7 VTO = 0.5445549 DELTA = 0, U0 = 436.256147 ETA = 0 THETA = 0.1749684 KP = 2.055786E-4 VMAX = 8.309444E4 KAPPA = 0.2574081 RSH = 0.0559398 NFS = 1E12 TPG = 1 XJ = 3E-7 LD = 3.162278E-11 WD = 7.046724E-8 CGDO = 2.82E-10 CGSO = 2.82E-10 CGBO = 1E-10 CJ = 1E-3 PB = 0.9758533 MJ = 0.3448504 CJSW = 3.777852E-10 MJSW = 0.3508721
PMOS: Level = 3 T <sub>ox</sub> =7.9E-9 NSUB = 1E17 GAMMA = 0.4083894 PHI = 0.7 VTO = -0.7140674 DELTA = 0 U0= 212.2319801 ETA = 9.999762E-4 THETA = 0.2020774 KP= 6.733755E-5 VMAX = 1.181551E5 KAPPA = 1.5 RSH = 30.0712458 NFS = 1E12 TPG = -1 XJ = 2E-7 LD = 5.000001E-13 WD = 1.249872E-7 CGDO = 3.09E-10 CGSO = 3.09E-10 CGBO = 1E-10 CJ = 1.419508E-3 PB = 0.8152753 MJ = 0.5 CJSW = 4.813504E-10 MJSW = 0.5

Tab. 2. CMOS process parameters.

In addition to the above, transient response of the band pass filter is shown in Fig. 10, with a 1.157 MHz sinusoidal input current signal having 15  $\mu$ A peak value applied at the input of the filter. Total harmonic distortion (THD) analysis has been carried out on BP filter at  $f_0 = 1.157$  MHz at various sinusoidal peak input currents and results for the same are shown in Fig. 13.

Simulated DC transfer characteristics are shown in Fig. 14 where it is shown that linear range of ZC-CFTA is from -25  $\mu$ A to 22.5  $\mu$ A. The dynamic range is 1 nA to 35  $\mu$ A and THD percentage would be low till input current

does not exceed  $\pm 22.5 \mu\text{A}$  (at  $f_0 = 1.1 \text{ MHz}$ ). The simulation results of the proposed circuit shown in Fig.6 –

14, thus, are seen to confirm the validity of the theoretical results.

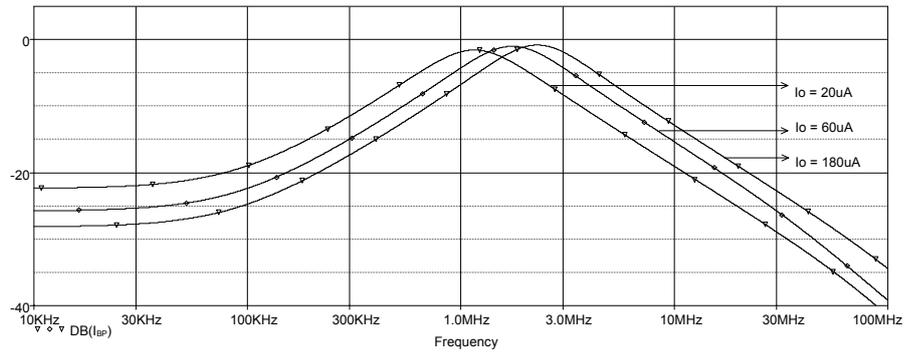


Fig. 6. Simulated result of BP filter with different  $f_0$  (keeping  $Q = 1$ ).

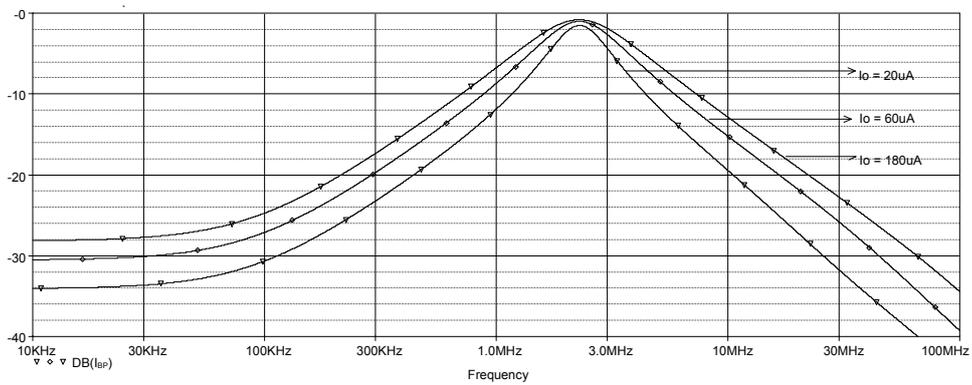


Fig. 7. Simulated result of BP filter showing variation in BW with change in  $g_{m1}$ .

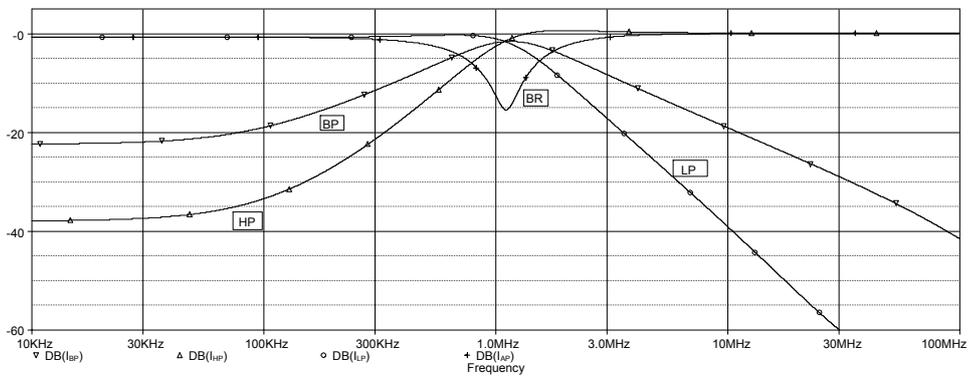


Fig. 8. Simulated frequency response of BP, LP, HP and BR filter.

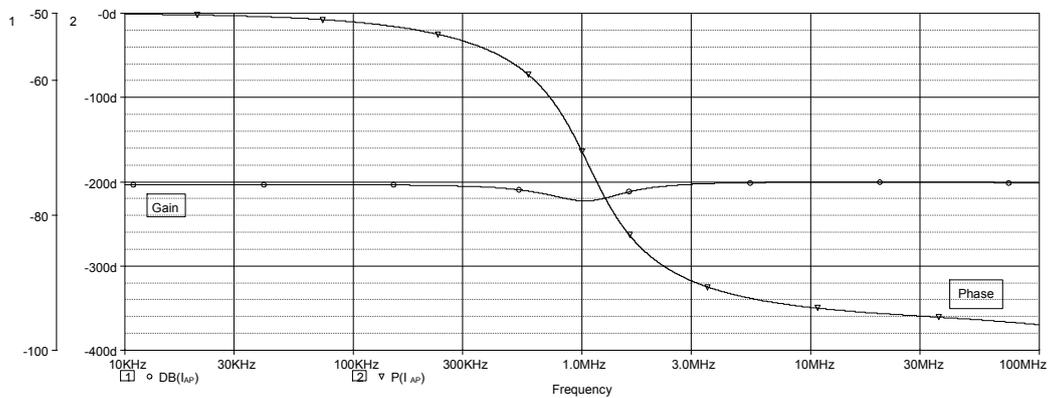


Fig. 9. Simulated gain and phase response of AP filter.

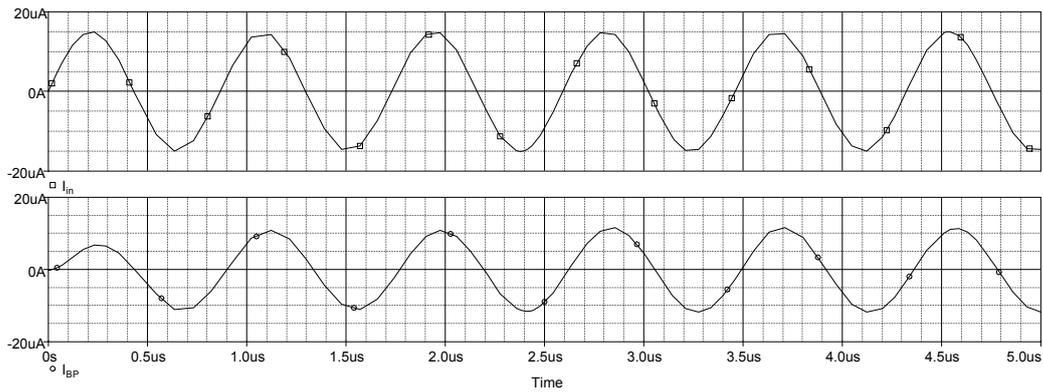


Fig. 10. Transient response of BP filter at  $f_0 = 1.157$  MHz.

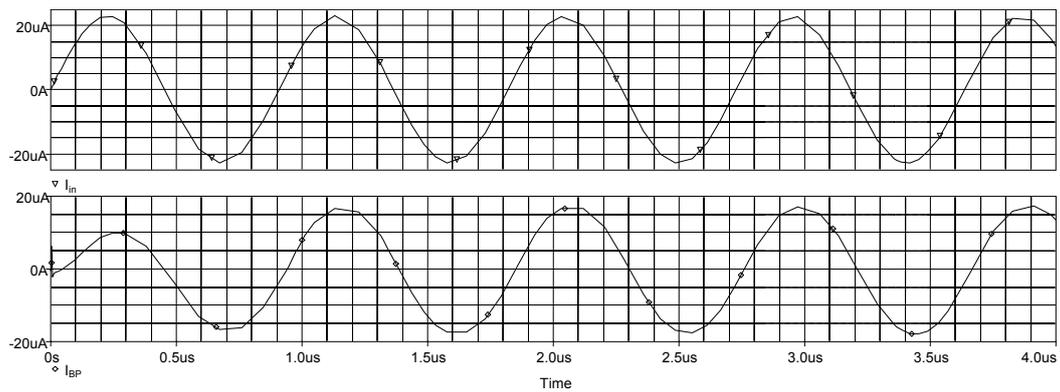


Fig.11. Large signal behavior of the bandpass filter (at  $f_0 = 1.1$  MHz with peak input of  $23 \mu A$ ).

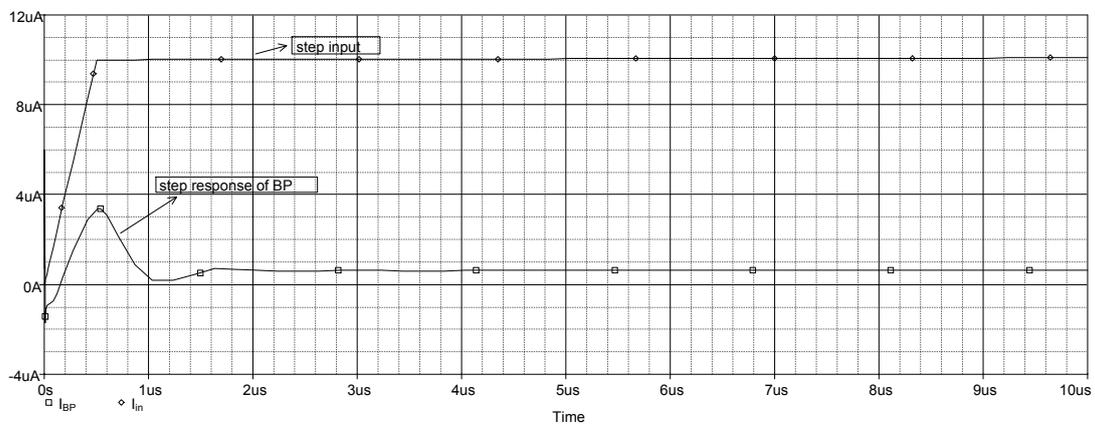


Fig.12. Step response of the BP filter.

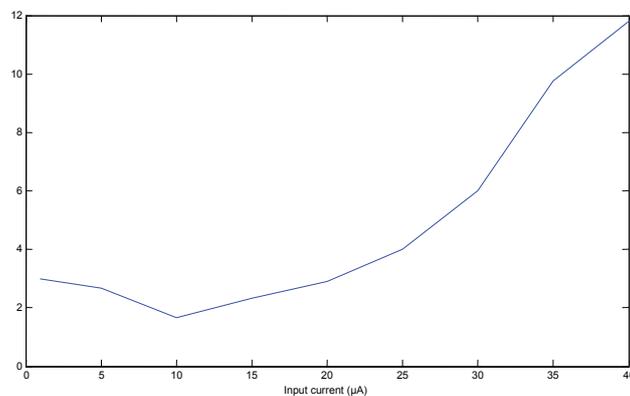


Fig.13. THD variations of the output waveform of the BP filter.

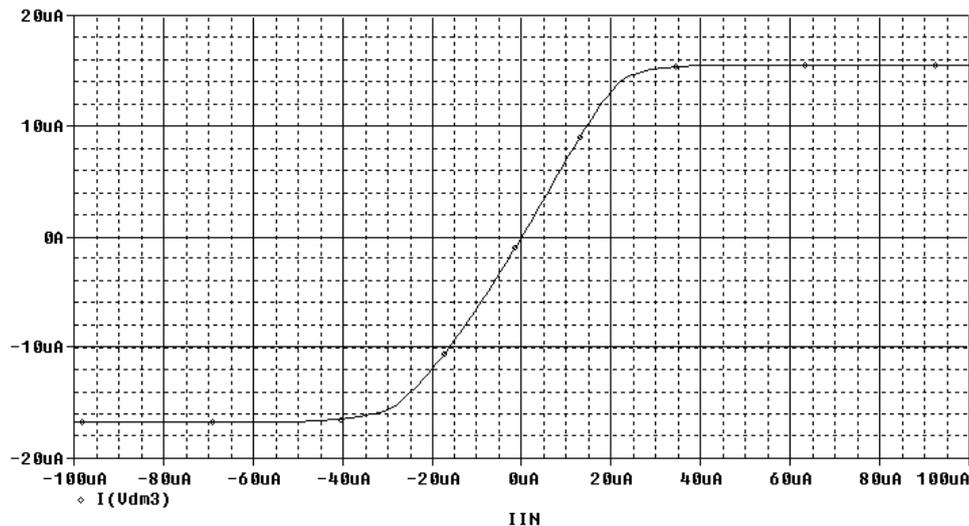


Fig.14. Simulated DC transfer Characteristics of ZC-CFTA.

## 7. Concluding Remarks

A new CFTA-based universal biquad has been presented which offers all the advantages of its predecessors of [3]-[6] namely, (i) realisability of all the five generic filter functions without requiring any component-matching conditions; (ii) independent electronic tunability of the filter parameters  $\omega_0$  and BW; and (iii) employment of both grounded capacitors as preferred for IC implementation. When compared with the four-CFTA circuits of [3]-[5], the new circuit has the advantage of requiring only three CFTAs. On the other hand, when compared to three-CFTA biquad of [6], the new circuit has the advantage of (i) not requiring any additional resistor as in [6], and (ii) providing a true CM operation unlike the transadmittance operation as in the circuit of [6]. The workability of the proposed structure has been confirmed by PSPICE simulation results.

The paper has, thus added a new universal biquad, having advantageous features as shown above, to the existing repertoire [3]-[6] of CFTA-based analog circuits.

Lastly, it may be mentioned that for realizing electronically controllable functions use of OTAs is well established, the use of CCCIs is rigorously being investigated recently but by contrast, CDTAs as well as CFTAs are relatively newer building blocks from a wide variety of possible new building blocks, see [1]. Consequently, very few publications have appeared on CFTAs and its full potential is still to be exploited. In view of this, we believe that newer applications of CFTAs deserve to be investigated further.

## Acknowledgements

This work was performed at Analog Signal Processing Research Lab, NSIT, New Delhi. The authors thank the

anonymous reviewers for their constructive suggestions and comments.

## References

- [1] BIOLEK, D., SENANI, R., BIOLKOVA, V., KOLKA, Z. Active elements for analog signal processing: Classification, review, and new proposals. *Radioengineering*, 2008, vol.17, no.4, p. 15-32.
- [2] HERENC SAR, N., KOTON, J., VRBA, K. Realisation of current mode KHN equivalent biquad using current follower amplifiers (CFTAs). *IEICE Transactions Fundamentals*, 2010, E93-A (10), p. 1816-1819.
- [3] TANGSRITAT, W. Single-input three output electronically tunable universal current mode filter using current follower transconductance amplifiers. *International Journal of Electronics and Communication (AEU)*, doi: 10.1016/j.aeu.2011.01.002.
- [4] SATANSUP, J., PUKKALANUM, T., TANGSRITAT, W. Current mode KHN biquad filter using modified CFTAs and grounded capacitors. *Proceedings of IMECS*, 2011, vol.2.
- [5] SATANSUP, J., TANGSRITAT, W. Single-input five-output electronically tunable current-mode biquad consisting of only ZC-CFTAs and grounded capacitors. *Radioengineering*, 2011, vol. 20, no. 3, p. 650 – 655.
- [6] HERENC SAR, N., KOTON, J., VRBA, K., LAHIRI, A. Novel mixed-mode KHN-equivalent filter using Z-copy CFTAs and grounded capacitors. *Latest Trends on Circuits, System and Signal, North Atlantic University Union (NAUN) WSEAS*, 2010, p. 87-90.
- [7] BIOLEK, D., BIOLKOVA, V., KOLKA, Z., BAJER, J., Single-input multi-output resistorless current-mode biquad. In *Proc. of ECCTD '09, European Conference on Circuit Theory and Design*. Antalya (Turkey), August 23-27, 2009, p. 225-228.
- [8] WANG, Z. 2-Mosfet transresistor with extremely low distortion for output reaching supply voltages. *Electronics Letters*, 1990, vol. 26, no. 13, p. 951- 952.
- [9] KOTON, J., HERENC SAR, N., VRBA, K. KHN-equivalent voltage-mode filters using universal voltage conveyors. *International Journal of Electronics and Communications (AEU)*, 2011, vol. 65, no. 2, p. 154-160.

- [10] HERENC SAR, N., KOTON, J., VRBA, K., LAHIRI, A. Realizations of single-resistance controlled quadrature oscillators using a generalized current follower transconductance amplifier and a unity-gain voltage follower. *International Journal of Electronics*, 2010, vol. 97, no.8.

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