Biquadratic Filter Applications Using a Fully-Differential Active-Only Integrator

Hacer Atar YILDIZ, Ali TOKER, Serdar ÖZOĞUZ

Faculty of Electrical&Electronics Eng., Istanbul Technical University, 34469, Maslak, Istanbul, Turkey

haceryildiz@itu.edu.tr, tokeral@itu.edu.tr, ozoguz@itu.edu.tr

Abstract. *A new class of active filters, real active-only filters, is described and possible implementation issues of these filters are discussed. To remedy these issues, a fully-differential active-only integrator block built around current controlled current conveyors is presented. The integration frequency of the proposed circuit is adjustable over a wide frequency range. As an application, a real active-only filter based on the classical two-integrator loop topology is presented and designed. The feasibility of this filter in a 0.35 μm CMOS process is verified through SPECTRE simulation program in the CADENCE design tool.*

Keywords

Active-only filters, current controlled current conveyors, analog filter design.

1. Introduction

Although there is a considerable amount of design experience available in the field of traditional active-R filter design [1], [2], the lack of electronic tuning possibility of these filters, which is an important drawback in their IC realizations, stimulated the researchers to focus on a new family of filters known as active-only filters [3]-[8]. These circuits are conventionally built using two active elements, opamp and OTA, the former being used to generate filter poles/zeros as in the case of conventional active-R filters, while the latter is used to ensure the tuning of the filter parameters. This added feature makes active-only circuits attractive compared to conventional active-R filters when these circuits are to be integrated on chip.

However, in active-only filters, other restrictions due to use of opamps, such as slew-rate limitations remain unsolved [9]. Furthermore, to realize filter coefficients, the active-only filters incorporate voltage scaling blocks composed of OTAs, which insert additional high impedance nodes to the circuit topology. Due to the parasitic capacitances at these high-impedance nodes, additional poles occur in the filter feedback and feed-forward paths, which degrade filter function characteristics. Moreover, the poles/zeros of the active-only filters [1]-[8] are realized using the compensation capacitor of the opamp, which is actually an external capacitor, thus the chip area occupied by these filter is large. In brief, this class of active-only circuits should not be considered as "real" active-only filters, but rather they are "pseudo" active-only filters that suffer from the same limitations as the classical opamp-RC filters, i.e. poor slew-rate performance, limited high-frequency range and large occupied chip area.

In this paper, in order to tackle these problems, a "real" active-only integrator and a "real" active-only filter based on this integrator are presented. The integrator pole comes from the intrinsic capacitances and resistances of a current controlled current conveyor (CCCII) [10], although the active element could be replaced with any transconductance amplifiers offering electronically tunable parameter.

This type of filters offers two obvious advantages over the conventional active-R filters: i) The filter is free from slew-rate limitation, hence offers better high-frequency performance compared to the conventional active-only filters which employ opamps. ii) The removal of external capacitors significantly reduces the chip area occupied by the filter.

However, this approach also entails some practical implementation issues: i) the time constants turn out to be very large, making the filter design challenging at relatively lower frequencies, ii) some of the intrinsic capacitances due to involved active devices suffer from large tolerances, iii) some of the intrinsic capacitances are nonlinear.

In order to address these issues, we considered and discussed possible circuit design techniques, which, in turn, have lead us to a new active-only integrator capable of operating at high-frequencies and providing electronically adjustable time constant with wide tuning range.

The integration frequency of the proposed integrator is determined by the intrinsic x-terminal resistance and z-terminal capacitor of a current controlled current conveyor (CCCII), the multiplication factor of a capacitance multiplier and the loss factor of a voltage divider. To illustrate the usefulness of the proposed integrator, a second-order filter based on the well-known two-integrator loop filter topology is considered and simulation results using SPECTRE in the CADENCE design tool verifying the proper operation of the circuit are provided.

The authors of this paper have recently proposed another real active-only integrator in [11]. However, the

integrator presented herein is superior since it utilizes an embedded capacitance multiplier subcircuit [12] which allows a very wide tuning range. Moreover, it operates in fully-differential mode; hence it enjoys all the advantages of differential mode of operation unlike the previous circuit in [11].

2. Design Considerations of the Real Active-only Integrator

In Fig. 1, a typical lossless integrator, widely used as the main building block of many filters is shown. In this circuit, the active device is a CCCII which is connected as a basic voltage to current converter [10].

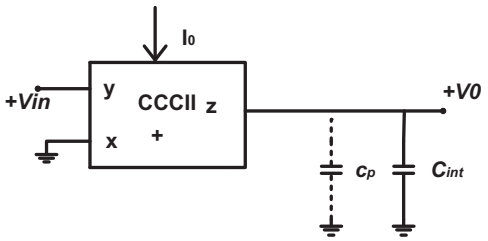


Fig. 1. A typical lossless integrator.

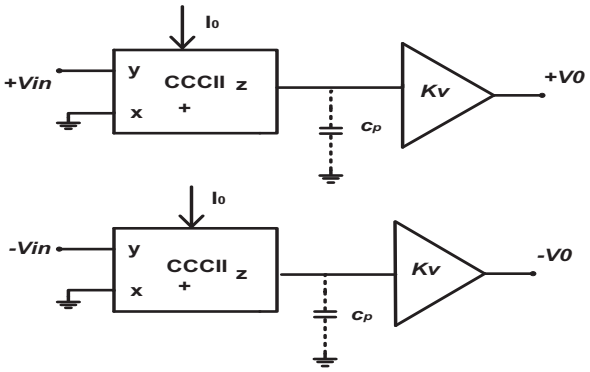


Fig. 2. Fully differential active-only integrator block.

Considering the following constitutive equation of CCCII [10],

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & r_x & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}, \tag{1}$$

it can be easily deduced that CCCII used in the lossless integrator operates as a basic transconductance amplifier. The integrator's time constant of this sample circuit is determined by the ratio of the equivalent capacitor seen into the z-terminal of the CCCII, i.e. (C_{int} +c_p) and the voltage to current conversion of the active device, which is the inverse of the CCCII's *x*-terminal parasitic resistance, r_x. For the standard CMOS CCCII realization in [13], r_x is an electronically controllable parameter through a biasing current I_0.

It may first seem straightforward to derive a real active-only integrator, i.e. an integrator without any external capacitor, from this circuit, by simply removing the external capacitor C_{int}, in which case the integration frequency, is given by $\omega_{int} = 1/r_x c_p$. This circuit, in differential-mode, is given in Fig. 2. Note that the equivalent capacitors c_p's consist of the parallel combination of the *z*-terminal intrinsic capacitors of the CCCIIs and the input capacitance of the voltage buffers at the circuit outputs. However, the real active-only integrator thus obtained turns out to offer limited high-frequency performance when ω_{int} assumes very large values, i.e. when its value is comparable with the undesired high-frequency poles of the CCCIIs and the voltage buffers. This is unfortunately the case for practical component values, due to very small value of the parasitic capacitor, c_p. It is, therefore, inevitable to lower the value of ω_{int}, in order to reduce the effects of these undesired high-frequency poles.

The high-frequency limitation mentioned above could be alleviated to some extend by deliberately increasing the value of c_p, by using very large transistors at the input stage of the following voltage buffer. However, the design of the circuit in this direction increases the chip area occupied by the circuit.

It should be also noted that any attempt to decrease the value of ω_{int} with the intent to increase the value of r_x is impractical, since this fact usually requires decreasing the biasing currents of the CCCII, which, in turn, causes the undesired high-frequency poles decreased as well.

On the other hand, the low frequency performance of the integrator is limited due to the finite output impedance of the CCCII. In the low-frequency operating region, the circuit operates as a lossy integrator, characterized by the following transfer function:

$$\frac{V_{out}}{V_{in}} = \frac{1}{r_x(sc_p + g_0)} \tag{2}$$

where g_0 is the nonzero output conductance of the CCCII. Note that due to the nonideal output conductance, a low-frequency pole at $1/r_0 c_p$ appears. For the proper operation of the integrator, the integration frequency should be sufficiently larger than this low-frequency pole.

From the above discussion, it can be concluded that for the proper operation of the integrator in Fig. 2, the undesired high-frequency and low-frequency poles should be sufficiently apart from the integration frequency of the circuit.

Considering all these remarks, we propose two circuit design techniques for a proper design of the active-only integrator:

(i) The output voltage buffer with unity gain is replaced with a buffered voltage divider providing a scaling factor smaller than unity. In this case, the transfer function of the integrator is given by

$$\frac{V_{out}}{V_{in}} = \frac{K_v}{r_x(sc_p + g_0)} \tag{3}$$

where K_v<1 is the nonnegative scaling factor of the voltage divider which can also be made electronically adjustable by using a proper design. Note that in this case, the integration frequency becomes $K_v/r_x c_p$ and its value is decreased, while the undesired low-frequency pole due to nonzero output conductance of CCCII remains the same. This may reduce the low-frequency performance of the integrator.

(ii) If a properly designed capacitance multiplier is embedded to the integrator, the value of c_p can be further increased, in which case the integrator's transfer function is given by:

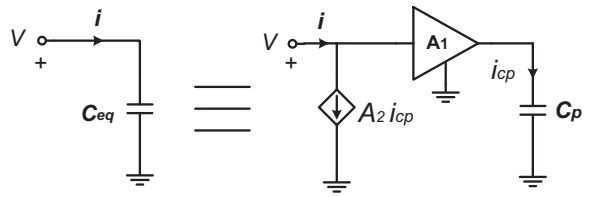
$$\frac{V_{out}}{V_{in}} = \frac{1}{r_x(sc_pK_c + g_0)} \tag{4}$$

where K_c is the capacitance multiplication parameter, the value of which is greater than unity.

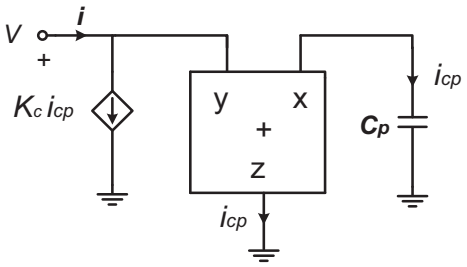
The conceptual circuit of capacitance multiplier [12] which consists of one voltage amplifier and one current amplifier is shown in Fig. 3a. Routine analysis of this circuit yields the following driving-point impedance function:

$$\frac{V}{I} = \frac{1}{sC_{eq}} = \frac{1}{sc_p.A_1.A_2} \tag{5}$$

which shows that when the product $A_1.A_2$ is kept larger than unity, the circuit operates as a capacitance multiplier.



(a)



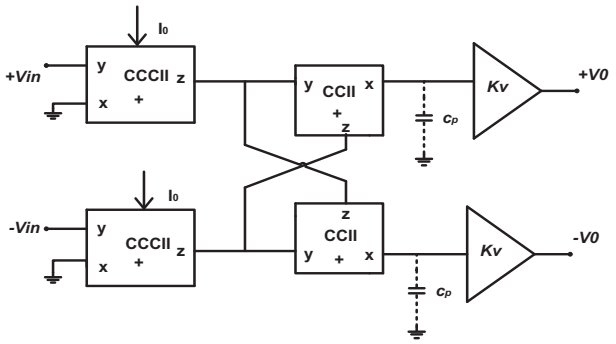
(b)

Fig. 3. a) Conceptual circuit for the capacitance multiplier [12]. b) Possible implementation using CCIIs.

This conceptual circuit can readily be implemented using the second-generation current conveyor (CCII)-based circuit in Fig. 3b. In this realization, we have $A_1 = 1$, $A_2 = K_c$, thus the equivalent capacitance becomes $C_{eq} = c_p.K_c$. Note that the dependent current source shown in this figure can be easily realized using a slightly modified CCII which provides a current gain of K_c, rather than unity.

It should be noted that this design technique is more appealing in the sense that both the integration frequency, ω_{int} and the low-frequency pole decrease of the same amount. Thus, the low-frequency performance of the integrator is not degraded unlike the previous technique.

(iii) Finally, for the proper design of the integrator, it is highly desirable that the integration frequency is adjustable within a large range, in order to compensate the deviation due to process variations.



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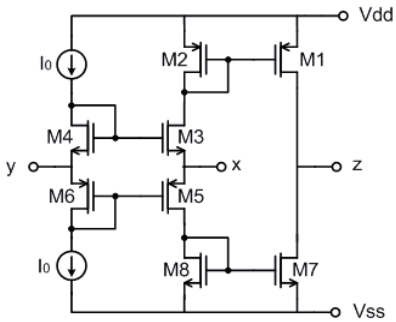

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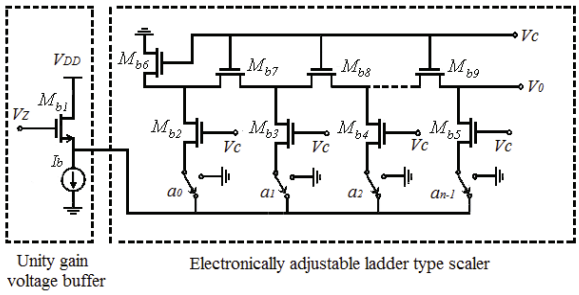


(c)

Fig. 4. a) The proposed fully-differential real active-only integrator. b) The CMOS circuit of the CCCIIs/CCIIs. c) Realization of the buffered voltage divider.

3. The Real Active-only Integrator

The real active-only integrator derived from the circuit in Fig. 2 according to the suggested modifications is shown in Fig. 4a. In this circuit, the additional cross-coupled current conveyors operate as capacitance multipliers. The detailed circuit of the involved CCIIs/CCCIIs and the buffered voltage divider are given in Figs. 4b and 4c, respectively.

Transistor labels	Transistor dimensions		
	CCCII	CCII	voltage divider
M_1	42/0.4	depends on K_C	
M_2	42/0.4	12/0.4	
M_3-M_4	15/0.4	40/0.4	
M_5-M_6	35/0.4	100/0.4	
M_7	15/0.4	depends on K_C	
M_8	15/0.4	15/0.4	
M_{b1}			140/1.2
M_{b2}-M_{b6}			10/1
M_{b7}-M_{b9}			20/1

Tab. 1. Dimensions of the MOS devices in Figs. 4b and 4c (M_{b1}-M_{b9} are NMOS transistors).

Note that CCIIs are realized from the same MOS circuitry as the CCCIIs, where the value of r_x is deliberately kept very low by choosing its biasing current sufficiently large compared to those of other CCCIIs in the circuit. Moreover, CCIIs used in the capacitive multiplication subcircuit are slightly modified current conveyors, where the current transfers between their *x*- to *z*-terminal currents are greater than unity, say equal to K_c, unlike conventional current conveyors where the current gain is unity. This current gain can be easily realized in the CMOS circuit in Fig. 4b by simply keeping the ratio of the transistors' dimensions at the output current mirrors (that is M_1, M_2 and M_7, M_8) equal to K_c. The CCIIs designed in this way sense the currents of the intrinsic capacitors at the input terminals of the buffers and feedback to the output terminal of CCCIIs after multiplying the capacitive multiplication parameter, K_c. In this case, it is easy to verify that the circuit fulfills the same function of the capacitance multiplier in Fig. 3 and the impedance appearing at the z-terminal of the CCCIIs becomes $K_c.c_p$.

Assuming that active devices are ideal, routine analysis of the circuit leads to the following transfer function:

$$\frac{V_0(s)}{V_i(s)} = \frac{K_v}{K_c s c_p r_x} \tag{6}$$

where K_v is the scaling factor of the voltage divider, K_c is the capacitance multiplication parameter and r_x is the *x*-terminal intrinsic resistance of the CMOS CCCII. For the CMOS circuit in Fig. 4b, r_x is given by:

$$r_x \approx \frac{1}{g_{m3} + g_{m5}} = \frac{\left(2\beta_n I_0\right)^{-0.5}}{1 + \sqrt{\beta_p / \beta_n}} \tag{7}$$

where I_0 is the biasing current of CCCII and $\beta_{n(p)}$ is the transconductance parameter and is defined as $\beta_{n(p)} = \mu_{n(p)} C_{ox} (W/L)_{n(p)}$.

Therefore, r_x is an electronically adjustable parameter via the biasing current, I_0. On the other hand, the circuit in Fig. 4c used to realize the voltage divider provides a scaling factor always less than unity. The value of this factor can be adjusted by changing the values of the digital word composed of the logical inputs, $\{a_0\ a_1\ a_2\ a_3\ \ldots\}$, which in turn control the positions of the switches. The circuit in Fig. 4c is depicted such that all the control inputs, a_i's are set to one. Routine analysis of this circuit shows that the value of the conversion factor, K_v is determined according to the following expression:

$$K_v = \sum_{i=0}^{n-1} a_i 2^{-(n-i)} \tag{8}$$

where *n* is the number of stage of the voltage divider.

Therefore, in our design, the third design technique mentioned in Section 2 is met, since K_v and r_x are both electronically adjustable parameters and the ratio K_v/r_x, and hence the integration frequency can be adjusted within a sufficiently large range.

The real-active only integrator also offers the following vital features for its proper operation:

(i) CCCII is designed to provide a very good high-frequency performance. For this purpose, the sizes of the MOS transistors CCCII are chosen as small as possible, at the cost of having decreased accuracy.

(ii) Buffered voltage divider in Fig. 4c is designed such that the equivalent capacitances, c_p's are as large as possible. To this end, the size of the transistor M_{b1} at the input stage of the buffer is chosen very large. On the other hand, it is seen from Fig. 4c that the input capacitance is dominated by the gate-source capacitance of the MOSFET transistors which can be considered linear as long as the transistor remains in saturation region. In this way, the input capacitance of the buffered voltage divider which is highly linear, becomes much more dominant than the *z*-terminal parasitic capacitances of the CCCIIs.

Finally, since the integration frequency of the proposed integrator depends on the value of a parasitic capacitor, c_p, it may be claimed that the circuit may be largely susceptible to random deviations in the process variations. However, after performing Monte-Carlo simulations of the proposed real active-only integrator designed in AMS 0.35 μm CMOS process, the standard deviation of its integration frequency is found to be almost the same as the standard deviation of a conventional two-stage opamp's unity-gain bandwidth. Note that active-only filters in [3]-[8] rely upon the unity-gain bandwidths of the

involved opamps created using an externally connected compensation capacitor. Therefore, the proposed integrator is not more susceptible to process variations due to the use of a parasitic capacitor rather than the use of an external capacitor. The details of these simulation results are given in a recent paper [11].

3.1 Characteristics of the Main Building Blocks

In this subsection, we have derived the main characteristics of the basic building blocks used in the real active-only integrator. The CCCII and CCII are implemented using the classical translinear topology in Fig. 4b and designed in AMS 0.35μm CMOS process. The circuits are powered with a single 3.3V DC, the aspect ratio of the MOSFETs are chosen as given in Tab. 1. The biasing current, I_0 is set to $I_0 = 5\mu A$, which corresponds to $r_x \approx 2\ k\Omega$, for the CCCII and $I_0 = 100\ \mu A$ for the CCII. Note that the capacitance multiplication parameter K_c is set to the desired value, by appropriately choosing the aspect ratios of the transistors, M_1 and M_8. The voltage divider is designed as a four-stage block ($n = 4$) with a scaling factor of $K_v = 0.5$ by setting $a_3 = 1$, $a_2 = 0$, $a_1 = 0$, and $a_0 = 0$.

First, in order to determine the dynamic range limitations of the CCCII, we have derived large signal voltage transfer characteristic from *y*- to *x*-terminals of this element. The simulation results obtained for three different biasing currents ($I_0 = 5\ \mu A$, $I_0 = 10\ \mu A$ and $I_0 = 20\ \mu A$), and are given in Fig. 5. From these characteristics, it can be deduced that the voltage transfer between *y*- to *x*- terminals remains close to the ideal case for an input signal range of 0.5 V, regardless of the value of the biasing current, I_0. Owing to the differential-mode operation of the integrator circuit, this range corresponds to a large-signal operation range of 1 V.

We have also derived the frequency dependency of the nonideal voltage gain between *y*- and *x*-terminals voltages. Simulations were performed for a biasing current of $I_0 = 5\ \mu A$ and the results are shown in Fig. 6. It follows from this characteristic, that in the frequency range of interest, the nonideal voltage gain can be modeled by a single pole model of the following form:

$$\alpha(s) = \frac{A}{1 + s/p_i}$$

similar to the common approach in the literature [14]. In this model, $A = 1 - \varepsilon_i$ is the DC gain error, p_i is the high-frequency pole. From the magnitude characteristic in Fig. 6, the parasitic high-frequency pole is determined as 900 MHz, while A is 0.99. It should be also noted that the characteristics in Fig. 6 remains the same regardless of the value of the biasing currrent, I_0.

We have also derived high-frequency limitations of nonideal current gain between *x*- and *z*-terminal currents of the CCCII. The resulting frequency characteristic shown in

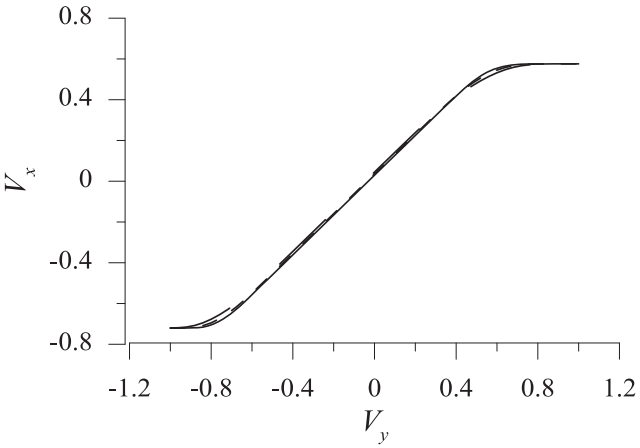


Fig. 5. Large signal characteristic of the *y*-to *x*-terminal voltage transfer of the CCCII for $i_x = 0$.

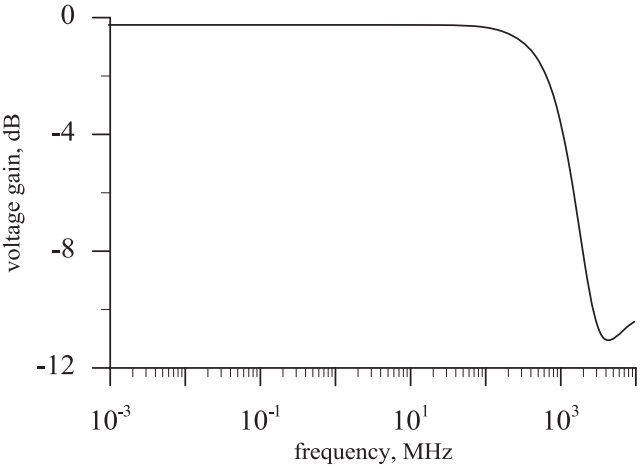


Fig. 6. Frequency dependency of the nonideal voltage gain between *y*- to *x*-terminal voltages.

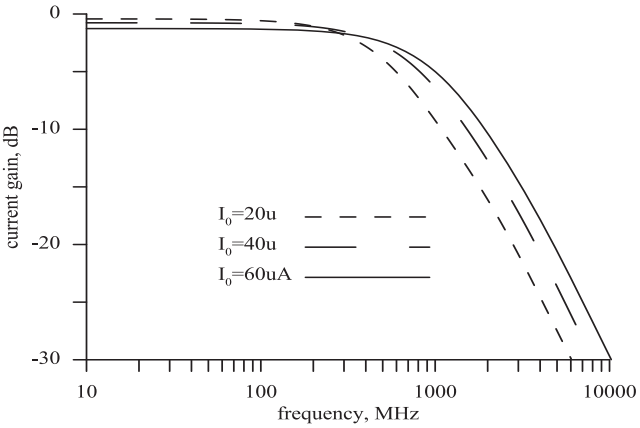


Fig. 7. Frequency dependency of CCCII current transfer between *x*- to *z*-terminal currents.

Fig. 7 conforms well to the single-pole model within the frequency range of interest. From these results, it is seen that the nonideal current gain suffers from a high frequency pole, which is at approximately 610 MHz for $I_0 = 40\ \mu A$. Note that this pole is significantly smaller than the pole of

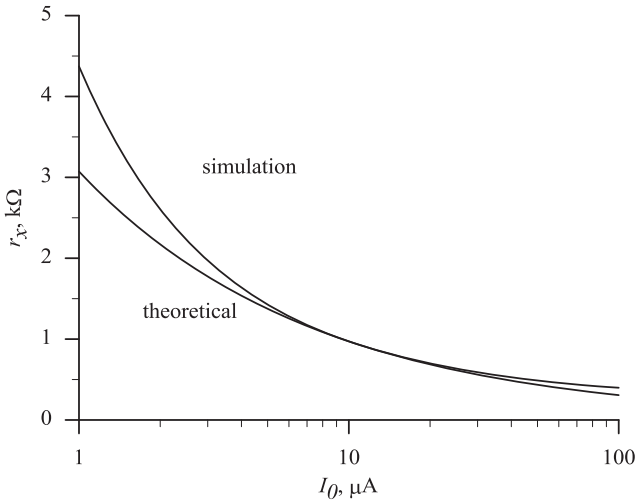


Fig. 8. The variation of the CCCII intrinsic resistance r_x with respect to biasing current I_0.

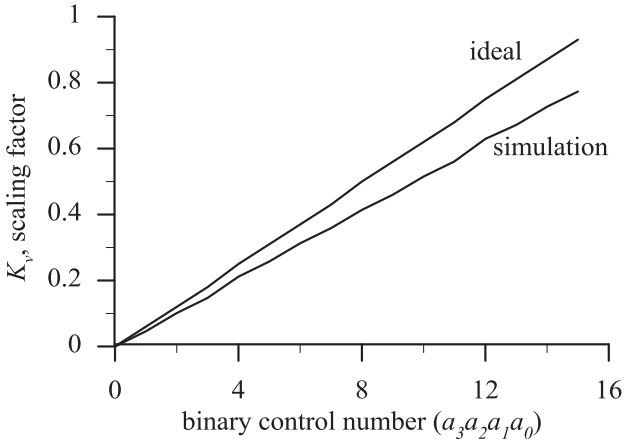


Fig. 9. The dependency of the gain of the voltage divider to the control word $\{a_3\ a_2\ a_1\ a_0\}$.

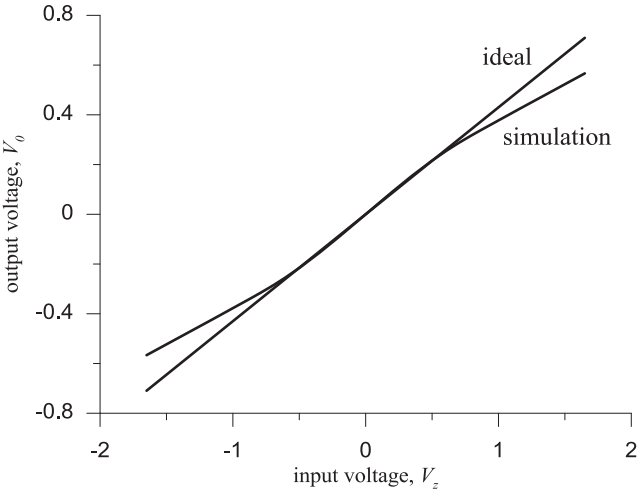


Fig. 10. The large signal voltage transfer of the buffered voltage divider.

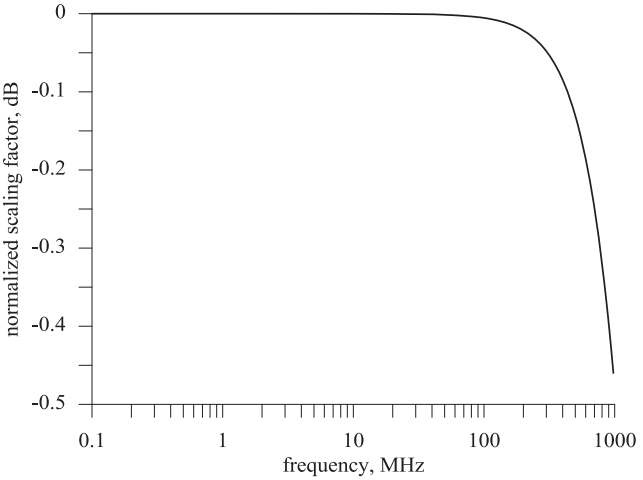


Fig. 11. Frequency dependency of the scaling factor of the buffered voltage divider.

the nonideal voltage gain of the CCCII+. As seen from these simulation results, the high frequency pole tends to increase for larger values of the biasing current, I_0.

As the final step for characterizing CCCII, we derived the dependency of the intrinsic resistance r_x to the biasing current I_0. Although we have the closed-form expression in (7) modeling this dependency, we have also provided the characteristic in Fig. 8 which illustrate this dependency. From these results, the wide-range controllability of the intrinsic resistance r_x with the biasing current I_0 over a wide range is verified. Note that the model in (7) is valid for mid-biasing current levels, while at low current levels, the square-root dependency of the conductance, r_x^{-1} in (7) tends to a linear dependency.

After specifying all the main characteristics of the CCCII, we have also studied the characteristics of the buffered voltage divider in Fig. 4c. For this purpose, we have derived the dependency of the scaling factor, K_v to the digital word $\{a_3\ a_2\ a_1\ a_0\}$ for $n = 4$. Aspect ratios of the transistors used in the circuit are as given in Tab. 1. The results of the simulation are shown in Fig. 9. Note that the discrepancies between the ideal and simulated curves stem mainly from the gain of the source follower built around transistor M_{b1} in Fig. 4c, which is lower than unity.

We have also studied large signal behavior of the buffered voltage divider. The circuit is designed with a scaling factor of $K_v = 0.5$ by setting the binary control number as $a_3 = 1$, $a_2 = 0$, $a_1 = 0$, and $a_0 = 0$, and its large signal input-output transfer characteristic is derived. From this characteristic given in Fig. 10, it is seen that voltage divider operates well with an input signal range of 0.7 V.

As the final step of the voltage divider characterization, we have derived its frequency characteristic when the scaling factor was $K_v = 0.5$. The scaling factor is plotted in Fig. 11. It follows from these results that, although the circuit suffer from high-frequency parasitic poles, these poles appear at much higher frequencies compared to the undesired pole of the CCCII+ nonideal current gain.

Finally, we tried to identify the effects of several underlying nonlinear mechanisms that cause distortion at the circuit output.

In analog circuit design, it is a common practice to use differential circuit design technique to improve the THD performance of circuits [15]. This advantage becomes more apparent if even order harmonics are dominant in the circuit. For this purpose we first consider a simple CCCII-based transconductance stage, similar to the subcircuit that drives the capacitors in Fig. 1. Note that the main nonlinearity that affects the performance of this simple voltage-to-current converter is the intrinsic r_x resistance, which, in turn, is a nonlinear element. Since r_x is basically the resistance seen into the source terminal of a MOS transistor and the characteristic of a MOS transistor obeys square-law model, this intrinsic resistance creates even-order harmonics. Therefore, in this voltage-to-current converter, even order harmonics are dominant. Both the single-ended and differential versions of this circuit are simulated for different biasing current values and variations of the THD at the output currents with respect to input signal amplitude are shown in Fig 12. Indeed, we have verified trough simulations that in single-ended mode, the second harmonic of the output signal is much larger (34 times larger, to be precise) than the third harmonic. These results justify the usefulness of the differential-mode operation to obtain acceptable THD performance at the output.

We have also studied the effect of the buffered voltage divider to the output signal distortion. For this purpose, the circuit in Fig. 4c is driven by a sinusoidal signal and THD at the output signal is measured. From the simulation results given in Fig. 13, it is seen that buffered voltage divider is a highly linear circuit.

3.2 The Main Non-idealities and Simulation Results of the Proposed Integrator

After considering the main frequency dependent non-idealities of the current conveyors and the voltage divider of the circuits in Fig. 4c, a more accurate model for the transfer function of the proposed integrator is given by:

$$\frac{V_0(s)}{V_i(s)} = \alpha(s)\beta(s)\gamma(s)\frac{1}{r_x}\frac{K_v}{g_0 + sK_c c_p \alpha(s)\beta(s)} \qquad (9)$$

where g_0 is the parasitic z-terminal conductance of the CCCII, r_x and K_v are electronically adjustable parameters defined in (7) and (8), $\alpha(s)$ and $\beta(s)$ are respectively the frequency dependent current and voltage gains of the current conveyors which are assumed to be equal for both CCCII and CCII. Finally, $\gamma(s)$ is the frequency dependent gain of the buffered voltage divider circuit in Fig. 4c. As discussed in Section 3.1, all the active non-idealities of current conveyors can be modeled by a single pole model and the bandwidth of the non-ideal current transfer function, $\alpha(s)$ is smaller than those of $\beta(s)$ and $\gamma(s)$.

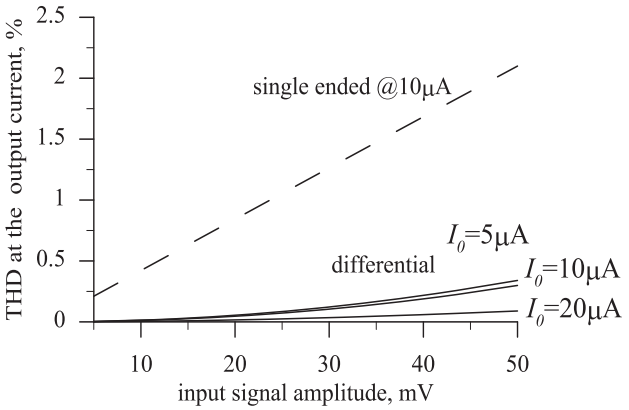


Fig. 12. Output THD of a CCCII-based transconductance block (input signal frequency were 25 MHz).

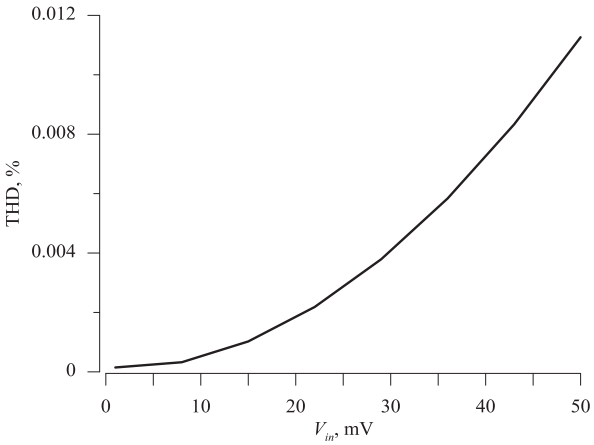


Fig. 13. Output THD of the buffered voltage divider (input signal frequency were 25 MHz).

Therefore, the transfer function in (9) can be simplified further by assuming that $\beta(s)$ and $\gamma(s)$ are constant and $\alpha(s)$ behaves according to the following single pole model in the frequency range of interest:

$$\alpha(s) = \frac{A}{1 + s/p_i}$$

where $A = 1\text{-}\varepsilon_i$ for the CCCII, $A = K_c(1\text{-}\varepsilon_i)$ for the CCII. Substitution of this model into (9) yields the following non-ideal transfer function:

$$\frac{V_0(s)}{V_i(s)} = \frac{1}{r_x}\frac{K_v(1-\varepsilon_i)}{\left[g_0 + s(K_c c_p(1-\varepsilon_i) + g_0/p_i)\right]}. \qquad (10)$$

From this expression, it is seen that due to the frequency dependent non-idealities of CCCIIs, the value of the equivalent capacitor, therefore the integration frequency is slightly changed. Note that this effect is not crucial, owing to the electronically controllability feature of the integration frequency.

In order to verify the feasibility of the above presented real active-only integrator, we have simulated the circuit and studied its performance. The basic blocks are designed and simulated as explained in Section 3.1.

In Fig. 14, simulation results obtained for two different values of K_c are given. It is seen that by changing the capacitor multiplication parameter, from $K_c = 1$ to $K_c = 20$, the value of the integration frequency changes from 37 MHz to 1.8 MHz. These results show that using the proposed integrator, the integration can be made adjustable over a very wide frequency range, i.e. well over one decade in this example.

The wide adjustability feature of the integration frequency can be illustrated alternatively using the simulation results shown in Fig. 15a and 15b, where the variations of the integration frequency via biasing current and capacitance multiplication factor are shown.

Finally, we have measured the power dissipation of the integrator as 3.1 mW.

4. Design of a Real Active Only Filter

In this section, in order to illustrate the usefulness of the proposed active-only integrator, the full-differential active-only filter in Fig. 16 is considered (only one half of the circuit is shown for the sake of simplicity). The circuit is of the classical two-integrator loop configuration and employs two of the proposed active-only integrators presented in Section 3 and two CCCIIs connected as simple voltage-to-current converters which form the filter feedback loops.

It is easy to verify by routine analysis that the circuit realizes the following transfer functions:

$$\frac{V_{LP}}{V_{in}} = -\frac{H_1\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}, \qquad \frac{V_{BP}}{V_{in}} = -\frac{H_2 s\frac{\omega_0}{Q}}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{11}$$

where

$$\omega_0 = \sqrt{\frac{K_{v1}K_{v2}}{r_{x2}r_{x3}K_{c1}K_{c2}C_{p1}C_{p2}}},$$

$$Q = \sqrt{\frac{K_{c1}K_{v2}C_{p1}}{K_{c2}K_{v1}C_{p2}}}\,\frac{r_{x4}}{\sqrt{r_{x2}r_{x3}}},$$

$$H_1 = \frac{r_{x3}}{r_{x5}} \quad \text{and} \quad H_2 = \frac{r_{x4}}{r_{x5}}.$$

Therefore, the circuit is capable of generating second-order lowpass and bandpass responses simultaneously. It is important to note that both the filter pole-frequency and pole-quality factor can be controlled electronically via the parameters K_{v1}, K_{v2}, r_{x2}, r_{x3}, r_{x4}, and the quality factor can be electronically adjusted independently from the pole frequency by varying r_{x4}.

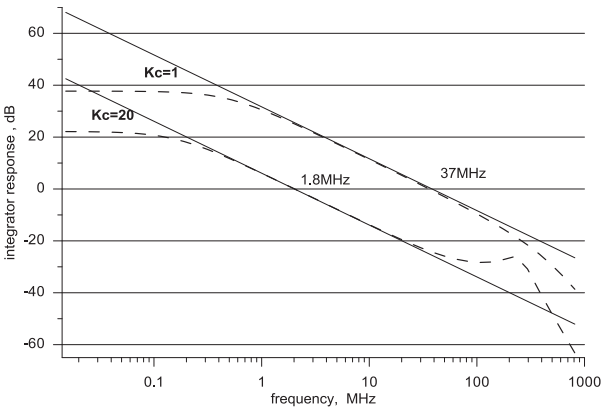


Fig. 14. Simulation results of the proposed active-only integrator for two capacitive multiplication parameter, $K_c = 1$ and $K_c = 20$ (—— ideal, - - - simulated).

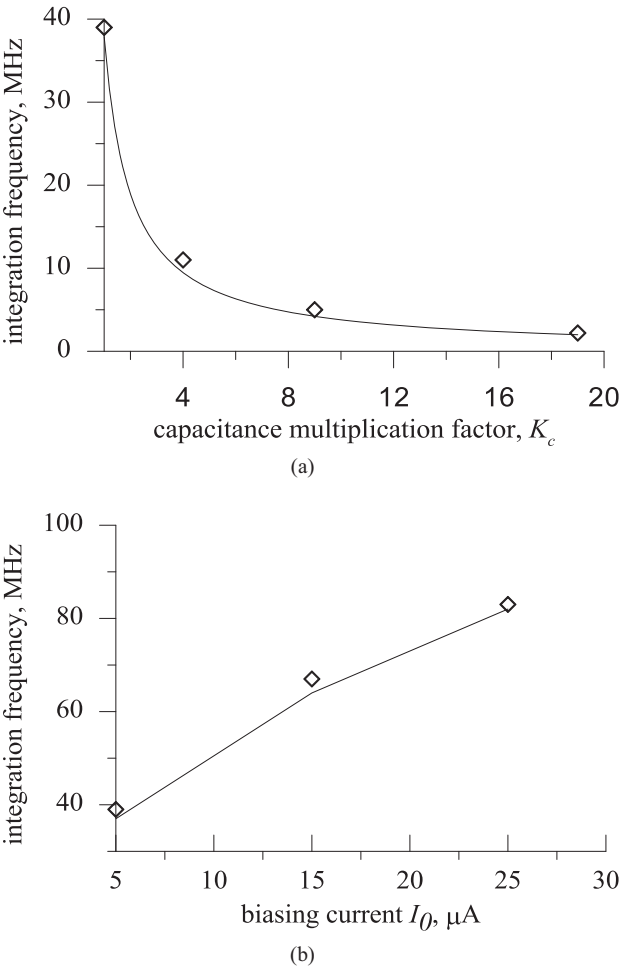


Fig. 15. Simulation results of the proposed active-only integrator for different values of a) the capacitance multiplication factor, K_c , b) biasing current, I_0.

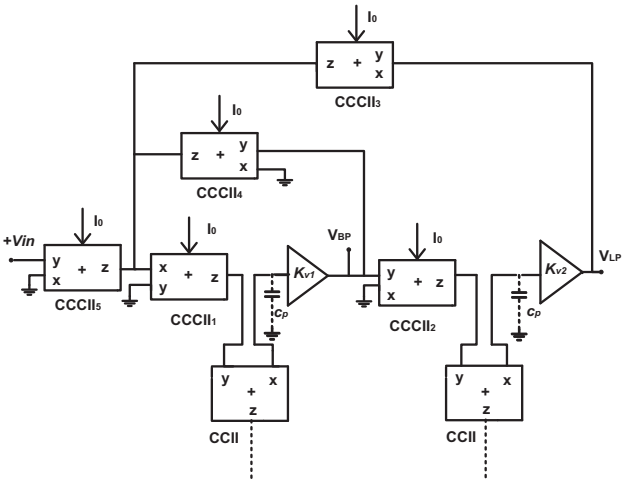


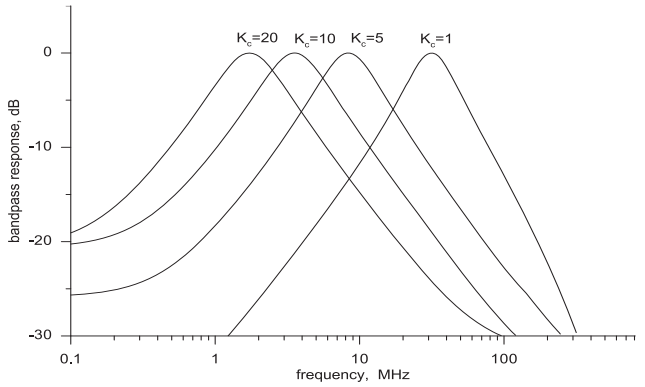
Fig. 16. The real active- only two-integrator loop filter (for the sake of simplicity, the negative half of the fully-differential circuit is not shown).

Using the same settings as those used for the real active-only integrator in Ssection 3.1, the overall filter is simulated in AMS 0.35 μm CMOS process. With this design and setting $K_c = 1$, the filter pole frequency becomes 37 MHz, with Q = 1.

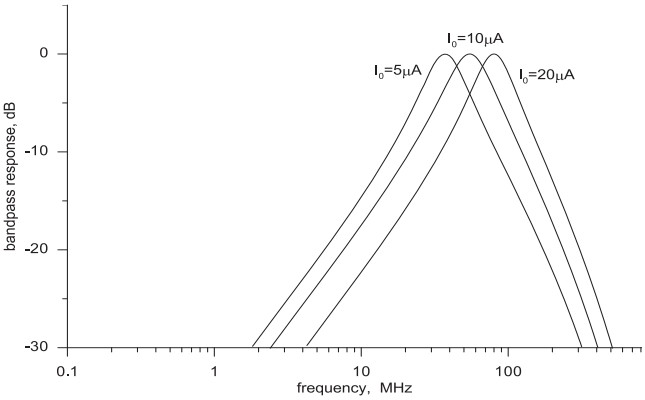
In order to verify the tunability of the filter over a wide frequency range, the circuit is simulated by changing the capacitor multiplication factor, K_c, from 1 to 20. As seen from the corresponding normalized magnitude characteristics in Fig. 17a, the circuit operates properly even if the center frequency is as low as 1.8 MHz, when K_c is 20. Note that for the classical integrator in Fig. 1 and with the same biasing conditions, an integration frequency value of 1.8 MHz requires a capacitor of 40 pF, which is an impractical value in today's IC technology.

We have also simulated the filter for different values of the biasing currents of CCCIIs, I_0 but keeping the value of K_c constant. The simulation results are shown in Fig. 17b where it can be seen that the center frequency of the bandpass filter can be electronically controllable from 37 MHz to 80 MHz. These results show that the bandpass filter has an electronic tuning range of approximately half a decade.

For the sake of completeness, we have provided phase responses for the bandpass filter in Fig. 18. The results are obtained for constant biasing current values, but with two different capacitance multiplication values, $K_c = 5$ and $K_c = 10$. Note that both the limited attenuation for the magnitude responses in Fig. 17a and the discrepancies for the phase responses in Fig. 18 appearing at low frequencies are attributed to the finite z-terminal resistance of the CCCIIs. Due to this, for large values of K_c , that is for low values of the center frequency, the operation frequency range of the filter is limited. However, this issue can be coped with by replacing output current mirrors of the CCCIIs (see Fig.4b) with those exhibiting larger output impedances, such as cascode current mirrors [15].



(a)



(b)

Fig. 17. Bandpass filter output of the real active only filter, a) for different capacitor multiplication factor, K_c ($@I_0$=5 μA). b) for different values of the biasing current, I_0($@K_c$=1).

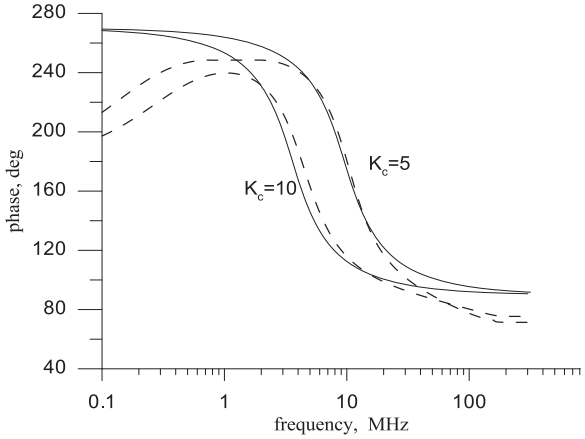


Fig. 18. Phase response of bandpass filter outputs for different capacitor multiplication factor, K_c ($@I_0$ = 5 μA). (—— ideal, - - - simulation).

Since the integration frequency and the center frequency of the proposed filter depend on the value of a parasitic capacitor, we have studied random deviations of the integration frequency of the active-only integrator due to the process variations. For this purpose, we have applied

Monte-Carlo simulations of the circuit with the same filter parameters that resulted in the AC characteristic in Fig. 16 for $I_0 = 10$ μA. The simulations were repeated 100 times and the variation of the center frequency is measured at each simulation. The histogram of the center frequency, whose nominal value is 40 MHz is given in Fig. 19. These simulations revealed a standard deviation of 6 % in the center frequency.

Finally, in order to show the proper operation of the filter, we have given some sample transient signals at the bandpass output as well as at the filter input in Fig. 20. The filter parameters were those that resulted in the AC characteristic in Fig. 16 for $I_0 = 10$ μA. The input signal frequency was 32.5 MHz, where AC gain at this frequency in Fig. 16 was -2.5 dB.

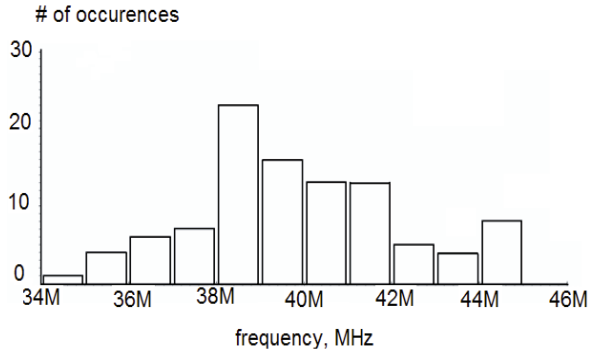


Fig. 19. Monte-Carlo simulation results showing the deviation in the standard deviations of the bandpass filter center frequencies (The filter parameters are the same as those used to derive Fig. 16).

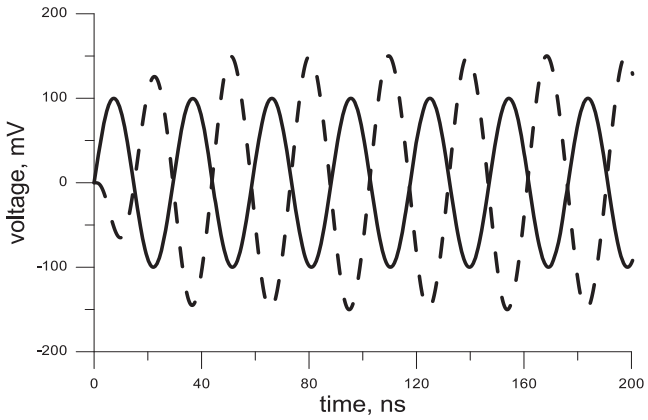


Fig. 20. Transient responses of the bandpass filter. The filter parameters are the same as those used to derive Fig. 16 (- - - input signal, ____ bandpass output).

5. Conclusion

A real active-only integrator composed of current conveyors and a buffered voltage divider is proposed. Owing to the use of an embedded capacitance multiplier, the circuit offers very wide tuning range. It is seen that the use of the proposed integrator to implement a filter without any external capacitor allows the realization of a pole-frequency value as low as 1.8 MHz. It is also concluded from filter simulation results that the tuning range of the considered filter is well over one decade.

Recently, some active only filters and/or filter basic building blocks, integrators, differentiators are presented [16]-[19]. While some of these circuits realize the required poles/zeros using the compensation capacitor of an opamp which is actually an external capacitor, to the authors' best knowledge, none of these filters employs a capacitive multiplication technique, which helps keeping the chip area significantly small.

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About Authors...

Hacer Atar YILDIZ was born in Trabzon, Turkey. She received the B.Sc. and M.Sc. degrees in electronics engineering from the Faculty of Electrical and Electronics Eng., Karadeniz Technical University, Turkey in 1997 and 2000, respectively. She is now pursuing her Ph. D. thesis at Istanbul Technical University in the area of analog integrated circuits and active-only filters.

Ali TOKER was born in Istanbul, Turkey. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Faculty of Electrical and Electronics Eng., Istanbul Technical University, Turkey in 1973 and 1975, respectively. He received the Ph. D. degree in 1986 from the Institute of Science and Technology of the same university. He is currently a full professor in electronics, teaching graduate and undergraduate courses. He is also the author or co-author more than 110 papers published in scientific reviews or conference proceedings. His main research interests are design of current-mode circuits and analog signal processing applications.

Serdar OZOGUZ was born in Istanbul, Turkey. He received his B.Sc. and M.Sc. in Electronics Engineering from Istanbul Technical University in 1991, 1993 and 2000 respectively. Since 2009, he is working as a full professor in Istanbul Technical University. He is currently a full professor in electronics, teaching graduate and undergraduate courses. He is also the co-author of 100 papers published in scientific reviews or conference proceedings. His research interests include analog circuit design, chaotic circuits and chaos applications.