A 0.5V 3rd-order Tunable g_m-C Filter

Richa ARYA, George SOULIOTIS, Spyros VLASSIS, Costas PSYCHALINOS

Electronics Laboratory, Dept. of Physics, University of Patras, Patras, Greece

aarya@upatras.gr, gsoul@upatras.gr, svlassis@physics.upatras.gr, cpsychal@physics.upatras.gr

Abstract. *This paper proposes a 3rd-order g_m-C filter that operates with the extremely low voltage supply of 0.5 V. The employed transconductor is capable for operating in an extremely low voltage power supply environment. A benefit offered by the employed transconductor is that the filter's cut-off frequency can be tuned, through a dc control current, for relatively large ranges. The filter structure was designed using normal threshold transistors of a triple-well 0.13μm CMOS process and is operated under a 0.5V supply voltage; its behavior has been evaluated through simulation results by utilizing the Analog Design Environment of the Cadence software.*

Keywords

G_m-C filters, analog filters, low voltage circuits.

1. Introduction

The operational transconductance amplifiers or g_m stages are used in the constructions of a number of continuous time circuits for analog signal processing such as filters and oscillators [1], [2]. The most often implementations of continuous-time filters are based on the g_m-C approach. A transconductor stage normally does not need frequency compensation as the operational amplifier does in order to ensure its stability and therefore it does not include low frequency poles. The advantage of g_m-C based continuous-time filters compared with active-RC filters is the higher frequency performance. Even if the transistors of the basic blocks operate in weak inversion and they cannot achieve the high frequency of the strong inversion operating transistors, they still keep advantage comparing with other topologies in terms of power consumption per pole. In addition, the resulted topologies are resistorless due to the employment of the small-signal transconductance parameters of the g_m stages, giving the potential for performing electronic adjustment of their frequency characteristics. On the other hand, the linear performance is worsened due to the restriction for operation in small-signal conditions.

The conventional transconductor stage uses a simple differential MOS transistor pair where its transconductance is easily controlled by modifying the tail current. A very interesting g_m stage topology is based on CMOS inverter and is called Nauta's transconductor. This transconductor is a very robust building block for implementing high frequency g_m-C filters [3], [4] because it does not include internal nodes and therefore low frequency poles. The Nauta's transconductor is based on six CMOS inverters in differential mode configuration. Due to the topology simplicity this block can operate in lower voltage supply comparing with conventional transconductors. However, based on this concept several CMOS inverter-based transconductors have been published [5-8] proposing transconductance control methodologies in order to use them as basic devices in tunable filters. To achieve tunable transconductance, the supply nodes of the internal inverters must be independent from the main chip supply [2], [3]. Therefore, tunable voltage regulators are used which are stacked on the CMOS inverters excluding this transconductor from low-voltage applications. Some alternative tuning concepts have been reported, using the input common-mode (CM) voltage [5] or floating-gate MOS (FGMOS) transistors [6].

In this paper we used a modified Nauta's current-controlled g_m stage, by means of transconductance tuning, in the construction of extremely low voltage continuous time g_m-C filters. Despite of operating the MOS devices in the weak inversion, the g_m stage is able to support filter applications in the range of few MHz due to the absence of internal nodes. The bulk voltages of the devices which are included in the g_m stage are appropriately modified through a control circuit achieving a linearly current-controlled transconductance [9]. The cut-off frequency of the filter can be easily adjusted through a control current using 0.5V voltage supply and offering also high g_m/I_{DD} ratio and circuit simplicity. All circuitries were designed using a triple-well 0.13μm CMOS process.

The paper is organized as follows: in Section 2 the filter topology is described. In Section 3, the simulation results verify the circuit operation and the performance comparing with other low-voltage topologies is given.

2. Filter Description

The topology of the LC ladder passive prototype filter is shown in Fig. 1(a), where its element values for realizing the normalized 3rd-order Butterworth filter function in (1)

$$H(s) = \frac{1}{s^3 + 2s^2 + 2s + 1} \tag{1}$$

are C_{1p}= C_{3p}= 1 F, L_{2p}= 2 H, and R_S= R_L= 1 Ω.

Following the leapfrog technique, the derived active g_m-C filter topology is depicted in Fig. 1(b).

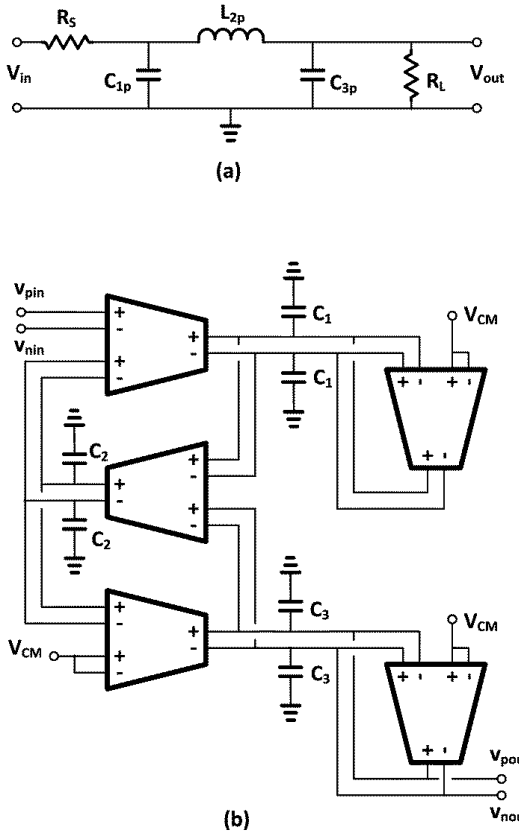

Fig. 1. Filter topology: a) passive prototype/circuit and b) active implementation.

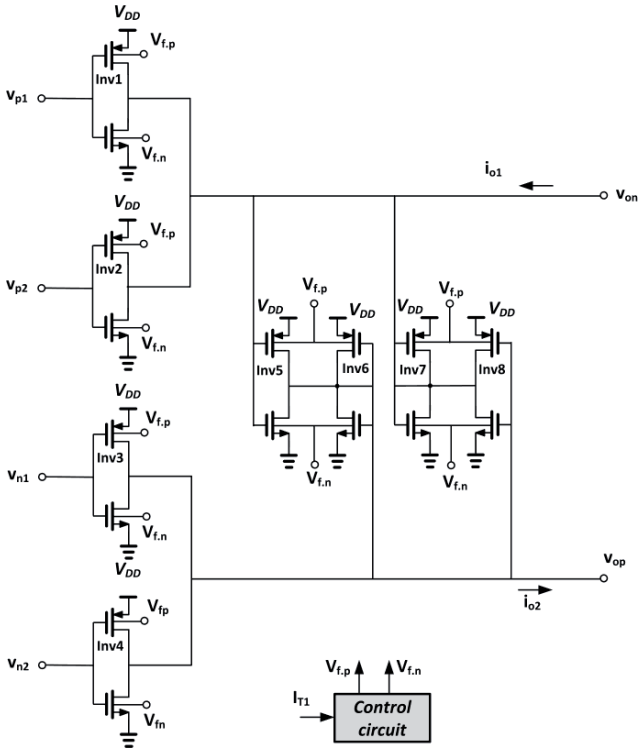

Fig. 2. The double input differential gm stage.

The core of the filter is the differential double input g_m stage with two very important features: the capability for operation with an extremely low-voltage power supply and the linearly current-controlled transconductance. The circuit of the g_m stage, which is based on the g_m stage proposed in [9], is shown in Fig. 2. In this paper, the transconductor has been modified in order to create multiple inputs suitable to be employed in the filter of Fig. 1.

In order to achieve both, low-voltage operation and transconductance tuning, the bulk terminals of the transistors are not connected to constant voltages as in conventional circuit topologies, but they are used to adjust their bias. Inverters Inv1 to Inv4 form the double input differential transconductor, inverters Inv5, Inv8 form the differential output load and inverters Inv6, Inv7 form the common mode (CM) output load. All inverters are controlled through the bulk voltages V_{fp} and V_{fn} which are generated by the Control circuit and the control current I_{TI}.

The transconductance controlled methodology is based on the master-slave technique using the control circuit which is shown in Fig. 3a. The CMOS inverter which is formed by $M_{p.s}$ and $M_{n.s}$, is the slave or active transconductor element and the input voltage V_{in} is applied at its input assuming also that input CM equal to middle supply (V_{DD}/2). The bulk terminals of both transistors are adjusted by the control circuit generating the voltages V_{fp} and V_{fn} which appropriately adjusted, bias the inverter with the desired quiescent current. Transistors $M_{p.m}$-$M_{n.m}$ and $M_{p.s}$-$M_{n.s}$ are the master the slave devices, respectively. The aspect ratios of the master devices are scaled down m times compared with the corresponding slave devices to minimize the area and current consumption. Therefore, the quiescent current of the slave devices are m times larger ($m \cdot I_T$) than those of the master devices (I_T).

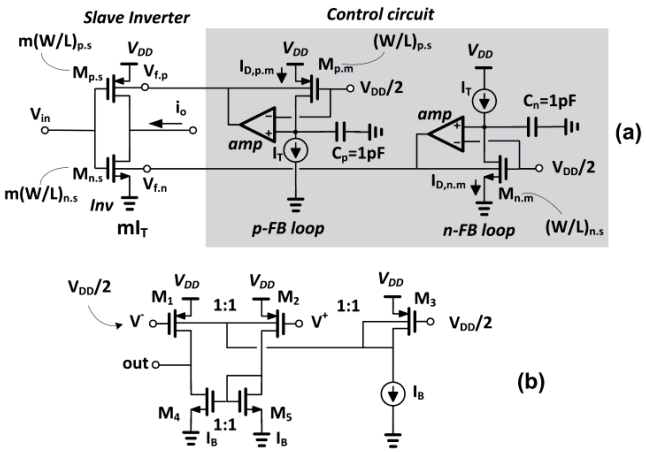

Fig. 3. (a) Schematic diagram of the proposed technique and (b) the circuit of the differential amplifier (amp).

The feedback voltages $V_{f.p}$ and $V_{f.n}$ are applied to the bulk terminal of the $M_{p.s}$ and $M_{n.s}$, respectively, of the slave inverter. Therefore, the quiescent current of the slave inverter will be $m \cdot I_T$ and the output CM voltage will be $V_{DD}/2$. Eventually, using this approach the transconductances $g_{m.p.s}$ and $g_{m.n.s}$ of $M_{p.s}$ and $M_{n.s}$, respectively, can be

adjusted by means of the controlling current I_T. The feedback loops ensure also, that the output CM voltage is kept constant, equal to $V_{DD}/2$ and independent from the value of I_T.

According to the above considerations and assuming that all transistors operate in weak-inversion [8] the transconductance of the slave inverter will be equal to,

$$g_{m.s} = g_{m.p.s} + g_{m.n.s} = (I_{D,p.s}+I_{D,n.s})/nV_t = 2mI_T/nV_t \quad (2)$$

where $g_{m.p.s}$, $g_{m.n.s}$ are the transconductance and $I_{D,p.s}$, $I_{D,n.s}$ are the drain current of the $M_{p.s}$ and $M_{n.s}$ transistors, respectively, shown in Fig. 3a. Also, n is the slope factor and $V_t = kT/q$ is the thermal voltage.

The output current of the transconductor in Fig. 2 is,

$$i_{dif} = i_{o1} - i_{o2} = v_{in.dif}\ g_{m.d} = (v_{p1} - v_{n1} + v_{p2} - v_{n2})g_{m.s} \quad (3)$$

The circuit of the differential amplifier which is employed in FB loops is shown in Fig. 3b. The input differential pair is formed by the pMOS devices M_1, M_2. Transistor M_3 is biased by the constant current I_B. Based on Figs. 3a and 3b, the constant voltage of $V_{DD}/2$ is applied to the gate voltage of M_1 and the feedback loops ensure that the gate voltage of M_2 will be locked at $V_{DD}/2$. Therefore, transistors M_1, M_2 and M_3 act, actually, as current mirror for CM signals and the quiescent drain currents of M_1, M_2 will be equal to I_B.

3. Simulation and Comparison Results

To verify the operation of the proposed filter, the circuit was designed and simulated using a triple well 0.13μm CMOS process with $V_{DD} = 0.5$ V. The transistors used in the simulations have a normal threshold voltage. The 3rd order Butterworth filter of Fig. 1b has a nominal cutoff frequency equal to 1 MHz for I_{TI} 10 μA. The capacitors of the filter have values $C_1 = C_3 = 74.31$ pF and $C_2 = 148.63$ pF.

The transistors' s aspect ratios of the transconductor in Fig. 3 were $(W/L)_{p.s1,2} = 100$ μm/0.5 μm, $(W/L)_{n.s.1,2} = 50$ μm/0.5 μm for $I_{nv1,2}$, $(W/L)_{p.s.3\text{-}6} = 25$ μm/0.5 μm, $(W/L)_{n.s.3\text{-}6} = 12.5$ μm/0.5 μm for Inv3-6 and $(W/L)_{1\text{-}3} = 10$ μm/0.5 μm, $(W/L)_{4,5} = 30$ μm/0.5 μm for the amplifier.

The scale factor was $m = 4$ and the bias current of $I_B = 1$ μA. The transconductance g_m and the gain-bandwidth product GBW of the transconductor are illustrated as functions of the tuning current I_{TI} in Fig. 4 [9]. THD is -40 dB for an input signal with amplitude 50 mV. Also, it is important that the common mode output is almost constant from process and temperature variations due to the internal feedback loop.

The cutoff frequency as function of the tuning current I_{T1} is plotted in Fig. 5. The lowest and highest cutoff frequency is 0.94 MHz and 5.1 MHz, for I_{T1} current 10 μA and 80 μA, respectively. In Fig. 6 the frequency responses are depicted for I_{T1} ranging between 10 μA and 80 μA. From Fig. 5 and Fig. 6 it becomes obvious that the relation between cutoff frequency and control current I_{T1} is not completely linear as expected from (2). This can be explained by the fact that the tuning range has been realized using a relatively high drain current variation. Increasing the drain current of a MOS transistor the drain-source conductance is decreased affecting the accuracy of (3).

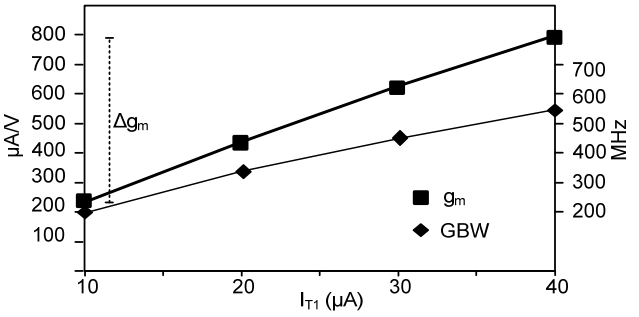

Fig. 4. Input transconductance g_m as function of I_{TI}.

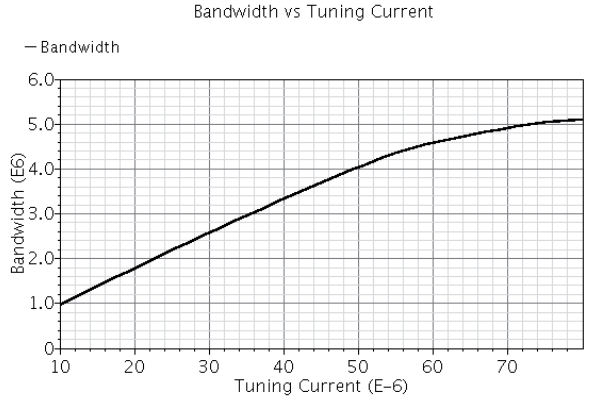

Fig. 5. Cutoff frequency as function of I_{TI}.

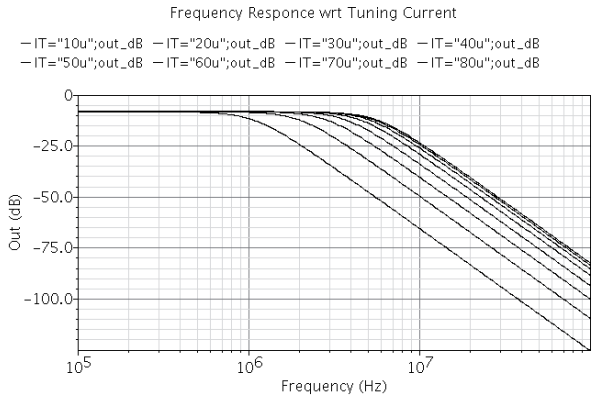

Fig. 6. Frequency responses for a range of I_{T1} from 10 μA to 80 μA.

Monte Carlo simulations have been performed in order to inspect the influence of the process and mismatch variations on the cutoff frequency of the filter. The results are shown in Fig. 7. The mean value is at 0.97 MHz with a standard deviation $\sigma = 17.4$ kHz, corresponding to 1.7% deviation from the nominal value. Also, corner analysis simulation results are summarized in Tab. 1. For the results the current I_{TI} is 10 μA, V_{DD} is 0.5 V and input amplitude

51.75 mV. As expected, while most of the parameters are unaffected, however there is a significant influence in the cutoff frequency, mostly due to the capacitor variations. It is known that the fully integrated filters may deviate from the nominal frequency with the corner variations, and therefore an automatic tuning topology is required when the accuracy is of high importance. The proposed filter is suitable to be combined with automatic frequency tuning technique, due to its inherent ability for electronic tuning.

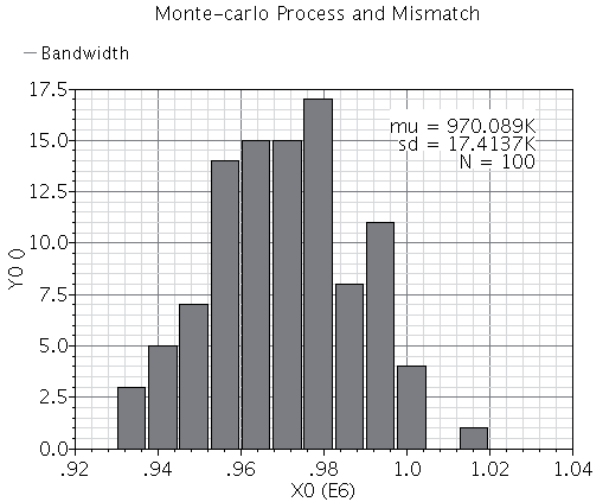

Fig. 7. Monte Carlo simulation results for the filter cutoff frequency.

In Tab. 2 the performance of the filter and some of its parameters are compared with other implementations of g_m-C filters [9]-[13]. This filter has the lowest supply voltage and also shows the best power consumption. Also, the values of other parameters of the filter, including dynamic range, noise, operating frequency and tuning range are comparable with the values of the other filters. The final conclusion is that this filter can achieve almost similar performance with other topologies but with significant reduction in supply voltage and in power consumption which is extremely important in mobile and biomedical applications. Some parameters of this filter may be worse, such as the tuning range. However, this is the price paid for operating in ultra low supply voltage using transistors of typical threshold.

	Unit	Typical	Fast-best	Slow-worst
Temperature	°C	27	-25	80
Cutoff frequency	MHz	0.970	1.165	0.819
Power Consumption @I_{T1} = 10 µA	µW	-339.2	-328.5	-338.7
Consumption Current	µA	-678.4	-657.0	-677.5
DC differential gain	dB	-8.1	-8.6	-7.4
CMRR	dB	-31.3	-31.0	-31.5
Dynamic Range		63.13	65.44	60.49
Integrated Noise (1 kHz-1 MHz)	µVrms	9.4	7.0	12.8
Input Referred Noise (1 kHz – 1 MHz)	µVrms	25.5	19.5	34.6
Input Referred Noise (Spot Noise@1 kHz)	nV/√Hz	217.51	193.12	242.85
Input Referred Noise (Spot Noise@1 MHz)	nV/√Hz	27.56	16.75	46.44
DC Output Voltage	mV	249.9	249.7	251.4
Input Offset	mV	-0.06	-0.331	1.359

Tab. 1. Parameter values of the filter vs corner variations.

4. Conclusion

A low-voltage filter operating at 0.5 V is proposed in this paper. The filter is constructed from transconductors based on simple inverters, where their tranconductance is controlled by the bulk voltage. The tuning range of the filter is controllable by a single control current. The filter has been simulated using transistor models with normal threshold voltage of a 0.13µm CMOS technology. The topology shows low power consumption and good performance in terms of noise, linearity, tunability and dynamic range.

	Unit	This Filter	[11]	[12]	[13]	[14]	[15]
Process		0.13µm CMOS	0.35µm CMOS	0.35µm CMOS	0.18µm CMOS	0.18µm CMOS	0.35µm CMOS
Supply/VDD	V	0.5	1.1	1.2	1.8	1	2.7
Filter Order		3	2	2	4	3	4
Bandwidth	MHz	0.9705	2.66	3			2.5
Frequency /Tuning range	MHz	0.97 – 5.1	0.05 – 2.6		0.5 - 12	0.135 - 2.2	0.2 – 2.5
Linearity/ THD		THD -40 dB @ 51.75 mVpp	THD -38 dB (0.4 Vp-p@ 2.6 MHz)	THD -40 dB @ 1.8 Vp-p		IM3 < 68.5 dB @ 2 MHz	Linearity 1 dB Comp 620 mVp-p diff
Power Consumption	µW	332	720	382	1100-4700	2000	1674
Spot noise	nV/√Hz @1MHz	27.56				65	41
Integrated noise	µVrms	9.44#		210 *			
Dynamic Range	dB	63.13		69.6			
Bulk/Gate Driven		Bulk Driven	Gate Driven	Bulk Driven	Gate Driven	Gate Driven	Gate Driven
Applications		Bluetooth	GSM, UMTS, WCDMA	2nd order FD OTA-C low pass filter	IEEE802.1 W-LANs, W-CDM, Bluetooth	GSM, Bluetooth, cdma2000, wide-band CDMA	GSM, IS-95, UMTS

*Integrated input referred Noise (100 Hz – 4 MHz)
#Total Summarized Noise (Output Noise 1 kHz-1 MHz)

Tab. 2. Comparison with other filter topologies.

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About Authors

Richa ARYA was born in Muzffarnagar, Uttar Pradesh, India. She received her B.Sc. degree in 2003 and M. Sc. degree in 2005, both in Physics, from M.J.P. Rohilkhand University, Bareilly, India. She is currently a PhD candidate in the Electronics Laboratory of University of Patras.

George SOULIOTIS received his B.Sc. in Physics from the University of Ioannina, Greece, in 1992, his M.Sc. in Electronics from the University of Patras, Greece in 1998 and his Ph.D. from the University of Patras, Greece in 2003. He is currently a member of the technical staff of the Department of Physics, University of Patras, Greece. Also, from 2004 he has been as a Post-Doctoral Researcher with the Electronics Laboratory, Department of Physics, University of Patras, Greece. Dr Souliotis serves as a reviewer for many international journals and he is member in national and international professional organizations. His research interests include integrated analog circuits and filters, current mode circuits and low voltage circuits.

Spyros VLASSIS received the B.Sc. in Physics in 1994, the M.Sc. degree in Electronic Physics in 1996 and the Ph.D. degree in 2000, from Aristotle University of Thessaloniki, Greece. He was working as a senior engineer for VC funded startup companies in the development and commercialization of high-performance RFICs for wireless communications and RF MEMS for consumer applications. He has published over 50 papers in journals and conferences and holds one U.S. patent. He is currently Assistant professor with Electronics Laboratory, Dept. of Physics. University of Patras, Greece. His research interests are in analog and RF integrated circuits and signal processing.

Costas PSYCHALINOS received the B.Sc. degree in Physics and the Ph.D. degree in Electronics from the University of Patras, Greece, in 1986 and 1991, respectively. From 1993 to 1995, he worked as Post-Doctoral Researcher with the VLSI Design Laboratory at the University of Patras. From 1996 to 2000, he was an Adjunct Lecturer with the Dept. of Computer Engineering and Informatics, University of Patras. From 2000-2004 he was an Assistant Professor with the Electronics Laboratory, Dept. of Physics, Aristotle University of Thessaloniki, Greece. From 2004-2009 he was an Assistant Professor and currently he is an Associate Professor with the Electronics Laboratory, Dept. of Physics, University of Patras, Greece. His research area is in the continuous and discrete-time analog filtering, including companding filters, sampled-data filters, current amplifier filters, CCII and CFOA filters, and in the development of low-voltage active blocks for analog signal processing. He also serves as a member of the Editorial Board of the Analog Integrated Circuits and Signal Processing Journal and as an Associate Editor of the Circuits, Systems, and Signal Processing Journal.