A Novel Second-Order All-Pass Filter Using Square-Root Domain Blocks

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Abstract. *In this study, a new second order all-pass filter is synthesized in the square-root domain by using the state-space method. The proposed second order all-pass filter is constituted by current mirrors, current sources, current-mode square-root circuits and capacitors. The pole frequency of the filter can be tuned electronically by varying the values of the current sources of this circuit. The filter is simulated in PSpice using 0.35μm CMOS technology parameters. Quality factor of the circuit is selected as 5 and supply voltage is set to 2.7 V. The simulation results show that the proposed circuit has the merits of electronic tunability. We also performed noise, THD and Monte-Carlo analyses. Various simulation results are presented to show the effectiveness of the proposed circuit.*

Keywords

Square-root domain filter, second order all-pass filter, translinear circuits.

1. Introduction

Nowadays, many researchers are interested in translinear filter circuits. Translinear circuits have some advantages, i.e. low voltage, low power and large dynamic range [1], [2]. Additionally, these filters are highly linear, i.e. produce low distortion, and can be electronically tunable [1], [3], [4].

Square-root domain (SRD) filters are a subclass of translinear circuits. These filters use the idea of the companding signal processing method [5], [6]. This feature uses the nonlinear current-to-voltage characteristics of MOS or bipolar transistors in order to achieve reduced voltage swings at internal nodes, thus allowing large dynamic ranges at low supply voltages.

SRD filters use MOS transistor devices in the strong inversion region of operation. These filters are based on the quadratic relationship between gate-to-source voltage and drain current of MOS transistors [6]. SRD circuits have been designed by using different synthesis methods. One of them is the state-space synthesis method. The state-space synthesis method for designing SRD filter was proposed in 1996 [7]. Then other systematic synthesis methods, e.g. block diagram method, for designing SRD filters have been introduced in the literature [8], [9]. Although many different types of SRD filters were designed so far, unfortunately, the proposed circuits cannot satisfy a high quality factor and electronic tunable all-pass characteristics together in second order [2], [6], [9], [10].

All-pass filter is a very popular processing block in analog signal operations in order to obtain time delays for the input signal while keeping the amplitude of the input signal constant for all frequencies [11]. Designed many all-pass filters employ active devices such as current-controlled conveyors [12], operational transresistance amplifiers (OTRA) [11], log domain integrators [13] and SRD block structures [10].

Many all-pass filters have been proposed in the literature; that use voltage mode synthesis methods and current mode synthesis methods [14], [11], [12]. Second order voltage mode all-pass filter with high input impedance property is proposed by Yuce et al. in 2008 [14]; however, the circuit has four passive elements including resistors and capacitors, has a low quality factor and it requires matching. First order voltage mode all-pass filter was proposed by Salawu [15]; this circuit has three resistors and a grounded capacitor, but it has not high input impedance. Another voltage mode cascadable first order all-pass filter with high input impedance was proposed in 2009 [16]. The filter is using single current conveyor and three passive elements; besides it has not capability of electronically tunable. First order voltage mode all-pass filter was proposed in 2008 [17]. The filter designed resistorless was electronically tunable. In 2010 voltage-mode all-pass filter was proposed by Biolek et al. [18]. The filter is using one active element, voltage differencing-differential input buffered amplifier (VD-DIBA), and one grounded capacitor. The filter operation is not determined by any matching constraint.

First order current mode all-pass filter was designed in 2003 [12].That filter has an electronically adjustable pole frequency but it requires a floating capacitor; which is not favorable for integrated circuit implementation [19]. Electronic tunable high frequency second order all-pass filter is presented in 2009 [13]. This filter, however, has not canonical number of capacitors. In Tab. 1 the proposed filter is compared with previously published first order and second order all-pass filters.

	Current Mode				Voltage Mode						
Properties	[12]	[13]	[20]		[11]	[14]	[16]	[17]	[18]	[21]	Proposed
Filter order	First	Second	First		Second	Second	First	First	First	First	Second
High quality factor	No*	Yes	No*		Yes	No	No*	No*	No*	No*	Yes
Electronically tunable	Yes	Yes	Yes		No	No	No	Yes	Yes	Yes	Yes
High input impedance	_	_	_		No	Yes	Yes	Yes	Yes	No	Yes
Grounded capacitors	No	Yes	Yes		No	Yes	Yes	Yes	Yes	No	Yes
Resistorless design	Yes	Yes	Yes		No	No	No	Yes	Yes	Yes	Yes
Number of canonical capacitors	Yes	No	Yes		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Supply voltage (V)	±2.5	3	±2.5		±2.5	±3	±2.5	±2.5	±5	±2.5	2.7
Power dissipation (mW)	NA**	25.3	NA**		NA**	99.5	NA**	NA**	NA**	15.6	9.67

Tab. 1. Comparison of the proposed filter with other first and second order all-pass filters.

*If cascaded to obtain second order all-pass filter
**Not available

In this paper, second order all-pass SRD filter circuit is designed by using the state-space synthesis method. The proposed circuit has high quality factor, high input impedance, only two grounded capacitors and electronic tunable pole frequency. The proposed filter does not require critical passive element matching. The paper is organized as follows: In section 2, the design method and architecture of the proposed second order all-pass SRD filter circuit is explained. Performance of the designed filter circuit is presented in section 3 by using PSpice simulation program. Obtained time domain and frequency domain responses as well as THD, Monte-Carlo and noise analysis results are given in this section. Finally, some conclusions are given in the last section.

2. Circuit Design

In this paper, second order SRD all-pass filter is designed by using the state-space synthesis method. The state-space synthesis method is more generally powerful and efficient approach. It defines not only input and output variables but also internal state variables. This allows us to observe and control all internal variables. Therefore, we can obtain the status of internal variables simply by using dynamic state-space equations.

A general second order all-pass filter's transfer function is given in (1), where ω_0 is the pole frequency and Q is the quality factor of the filter.

$$\mathrm{H(s)}=\frac{V_{out}}{V_{in}}=\frac{y}{u}=\frac{s^2-\omega_0/Qs+\omega_0^2}{s^2+\omega_0/Qs+\omega_0^2}. \tag{1}$$

According to the state-space synthesis method, state-space equations can be obtained from the transfer function by using several methods [22], [23], [24]. In this study, we use the modified companion method [24], [25] for state-space representation of (1). State-space representation of the proposed all-pass filter obtained by using this technique is expressed as (2).

$$\begin{gathered}\ddot{y}=-\frac{\omega_0}{Q}\dot{y}-\omega_0^2 y+\ddot{u}-\frac{\omega_0}{Q}\dot{u}+\omega_0^2 u,\\ x_1=y+r_1 u,\\ \omega_0 x_2=\dot{x}_1+r_2 u\end{gathered} \tag{2}$$

where u is input, y is output, x_1 and x_2 are the state variables, r_1 and r_2 are coefficients depending on the pole frequency and quality factor and these coefficients are given in (3).

$$r_1=-1\,;\quad r_2=\frac{2\omega_0}{Q}. \tag{3}$$

Then some adjustments are applied to (2) and the state-space representation of the system is obtained as (4).

$$\begin{gathered}\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix}=\begin{bmatrix}0 & \omega_0\\ -\omega_0 & -\frac{\omega_0}{Q}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}-\frac{2\omega_0}{Q}\\ \frac{2\omega_0}{Q^2}\end{bmatrix}u\\ y=\begin{bmatrix}1 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}1\\ 0\end{bmatrix}u\end{gathered} \tag{4}$$

In this work, second order SRD all-pass filter is designed by using only current mode square-root blocks, current mirrors and two grounded capacitors. Therefore, the circuit equations must be formed only square-rooting terms. In order to design this filter in SRD, DC input u_2 is added to the system. For this purpose state-space equations are organized as follows (5).

$$\begin{gathered}\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix}=\begin{bmatrix}0 & \omega_0\\ -\omega_0 & -\frac{\omega_0}{Q}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}-\frac{2\omega_0}{Q}\\ \frac{2\omega_0}{Q^2}\end{bmatrix}u+\begin{bmatrix}k_1\omega_0\\ k_2\omega_0\end{bmatrix}u_2\\ y=\begin{bmatrix}1 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}1\\ 0\end{bmatrix}u\end{gathered} \tag{5}$$

where u_2 is DC input, k_1 and k_2 are coefficients depending on the quality factor. The coefficients are given in (6).

$$k_1 = \frac{2-Q}{Q} \;;\; k_2 = \frac{Q^2+Q-2}{Q^2}. \tag{6}$$

The state-space design procedure is based on non-linear transformation of input and state variables while maintaining linear relationship through input to output. In this study, MOS transistors are utilized. Nonlinear square-root transformation is shown in (7) for MOS transistor characteristics.

$$\begin{aligned} x_1 = v_1 = \sqrt{\frac{I_1}{\beta}} + V_{th} \;;\; x_2 = v_2 = \sqrt{\frac{I_2}{\beta}} + V_{th} \\ u = \sqrt{\frac{I_u}{\beta}} + V_{th} \;;\; u_2 = \sqrt{\frac{I_{u_2}}{\beta}} + V_{th} \end{aligned} \tag{7}$$

where $\beta = \frac{\mu_0 C_{ox} W}{2L}$.

Nonlinear mapping shown in (7) is applied to the state-space equations of (5). Obtained circuit equations are given in (8).

$$\begin{aligned} \dot{v}_1 &= \omega_0 \sqrt{\frac{I_2}{\beta}} - \frac{2}{Q}\omega_0 \sqrt{\frac{I_u}{\beta}} + k_1 \omega_0 \sqrt{\frac{I_{u_2}}{\beta}} \\ \dot{v}_2 &= -\omega_0 \sqrt{\frac{I_1}{\beta}} - \frac{1}{Q}\omega_0 \sqrt{\frac{I_2}{\beta}} + \frac{2}{Q^2}\omega_0 \sqrt{\frac{I_u}{\beta}} + k_2 \omega_0 \sqrt{\frac{I_{u_2}}{\beta}} \\ y &= v_1 + u \end{aligned} \tag{8}$$

Equation (9) is derived from (8) by multiplying each side by $C(= C_1 = C_2)$ coefficient. Then $\frac{\omega_0^2 C^2}{\beta}$ is assumed to be equal to DC current source I_f values.

$$\begin{aligned} C_1 \dot{v}_1 &= \sqrt{I_f I_2} - \frac{2}{Q}\sqrt{I_f I_u} + k_1 \sqrt{I_f I_{u_2}} \\ C_2 \dot{v}_2 &= -\sqrt{I_f I_1} - \frac{1}{Q}\sqrt{I_f I_2} + \frac{2}{Q^2}\sqrt{I_f I_u} + k_2 \sqrt{I_f I_{u_2}} \\ y &= v_1 + u \end{aligned} \tag{9}$$

In (9), $C_1\dot{v}_1$ and $C_2\dot{v}_2$ are regarded as the time varying current through two capacitors C_1 and C_2 connected between v_1 and ground and between v_2 and ground, respectively. In these equations; v_1, v_2, u and u_2 are gate-source voltages of MOS transistors operating in the saturation region and their drain currents are defined as I_1, I_2, I_u and I_{u2} respectively.

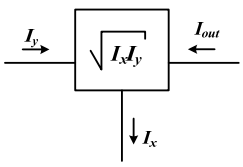

Fig. 1. Current mode square-root circuit block diagram.

Second order SRD all-pass filter can be realized using (9). According to (9) the proposed all-pass filter is designed by using square-root blocks, current mirrors, current sources and grounded capacitors. In these equations, each square-root term can be designed using a square-root block diagram with two input currents shown as in Fig. 1.

Block diagram in Fig. 1 is realized by using MOS transistors as shown in Fig. 2 [26]. That circuit operates as a square-root circuit since its output is the square-root of two input currents I_x and I_y. This expression is formulated as shown in (10).

$$I_{out} = \sqrt{I_x I_y}\,. \tag{10}$$

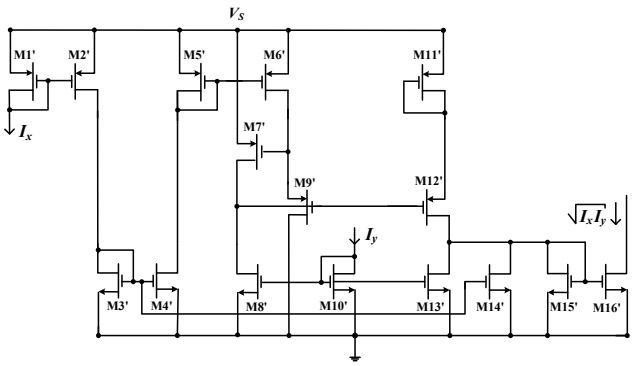

Fig. 2. Current mode square-root circuit derived from [26].

In this paper the proposed second order SRD all-pass filter circuit is designed as seen in Fig. 3.

3. Simulation Results

The second order all-pass filter consists of four square-root circuit blocks, current mirrors, current sources and two grounded capacitors. The designed circuit has been simulated using TSMC 0.35μm CMOS model parameters in PSpice program. The circuit supply voltage is selected to be 2.7 V. The values of two capacitances of the circuit are chosen to be 15 pF. The bias current of circuit I_f is set to be 50 μA. Input voltage of the proposed circuit u is set to 0.75 V DC and 50 mV AC values. Added DC voltage u_2 is set to 1 V. The gain of the filter is chosen as 1 and quality factor Q is chosen as 5. Dimensions of transistors in the proposed filter circuit are given in Tab. 2.

Transistor	W (μm)	L (μm)	Transistor	W (μm)	L (μm)
M1, M4, M8, M9, M13, M14, M15, M20, M22	6	0.7	M2, M5, M6, M7,M10, M11, M21	20	0.7
M12	1.2	0.7	M3	22.4	0.7
M18	2.8	0.7	M16, M17	36	0.7
M19	2.4	0.7	M23	3.6	0.7
M3', M4', M8', M10', M15', M16'	6	0.7	M1', M2', M5', M6', M7', M9'	20	0.7
M13', M14'	3	0.7	M11', M12'	40	0.7

Tab. 2. Dimensions of the MOS transistors for square-root circuit in Fig. 2 and 3.

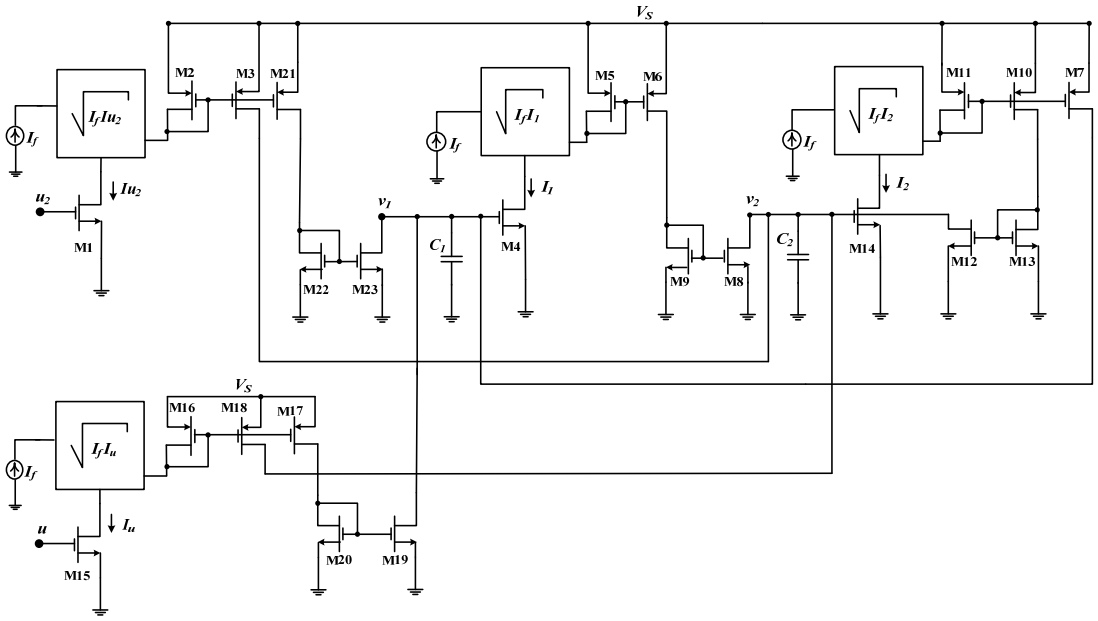

Fig. 3. Proposed second order SRD all-pass filter circuit diagram.

The designed all-pass filter circuit's pole frequency is obtained about 1.69 MHz. The filter is analyzed in PSpice for frequency response. Obtained gain and phase responses of the filter are shown in Fig. 4.

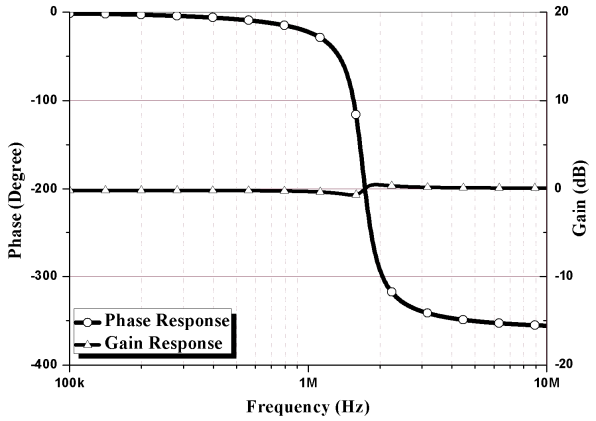

Fig. 4. Second order all-pass filter gain and phase response.

Fig. 5 shows the transient analysis response of the proposed all-pass filter in Fig. 3 while applying a 50mV sinusoidal wave with frequency of 1.69 MHz at the input. Input and output voltages of the proposed filter are given as in Fig. 5.

Next simulation is performed for frequency response of the circuit by tuning the pole frequency electronically. The quality factor of filter is set to $Q = 5$. The simulations are performed to tune the pole frequency by varying the values of the current sources. Varying the values of the current sources, from 15 µA to 150 µA, the pole frequency of the filter is tuned. The resulting frequency response for all-pass filters is plotted in Fig. 6.

Total harmonic distortion values are calculated through PSpice simulation program for input voltage amplitude values from 10 mV to 100 mV. The obtained results are plotted in Fig. 7. THD analysis results show that; when input voltage amplitude is below 10 mV, THD is less than 0.4 %; THD is below than 4 % for input voltage amplitude is below 100 mV.

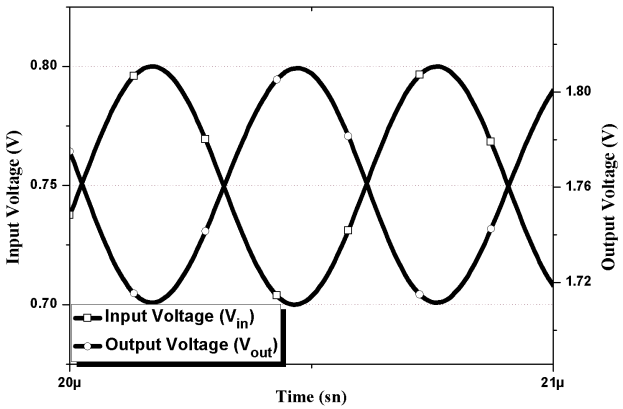

Fig. 5. Second order all-pass filter time domain response.

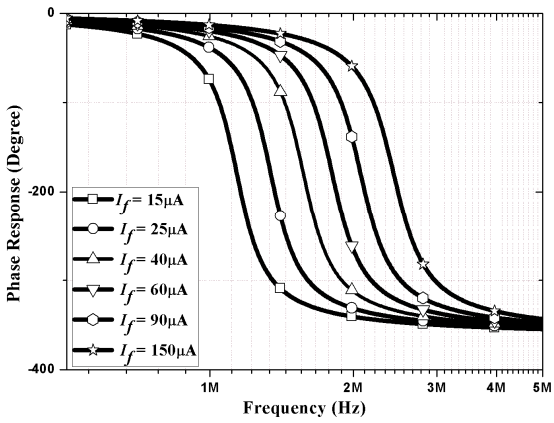

Fig. 6. Electronically tunable second order all-pass filter phase response.

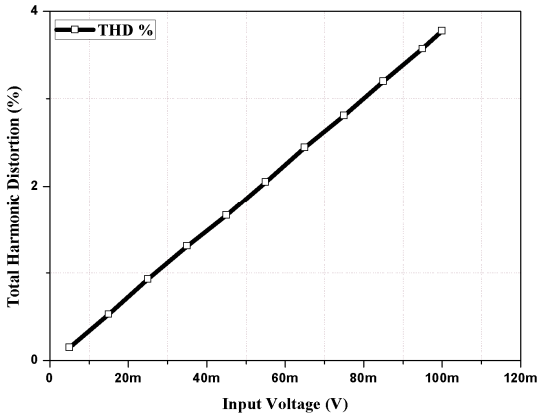

Fig. 7. Total harmonic distortion for various input voltages.

Statistical analysis of the proposed circuit was also performed by using PSpice program. Simulation results of Monte-Carlo analysis for 5% Gaussian change in the C_1 and C_2 capacitor values and 10% Gaussian change in the I_f current sources value are given in Fig. 8 and 9 respectively.

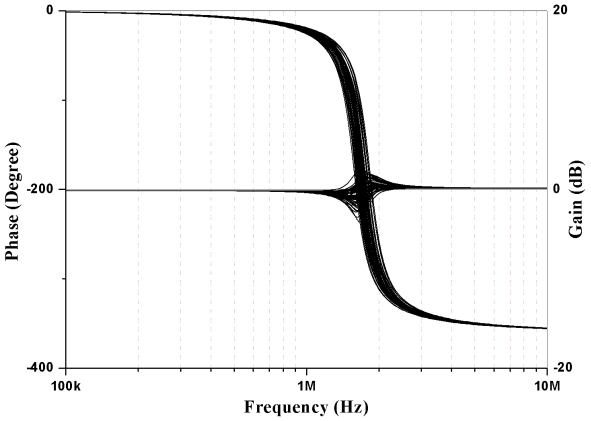

Fig. 8. Monte-Carlo analysis for the phase and gain responses for 5% Gaussian change in the C_1 and C_2 capacitor values.

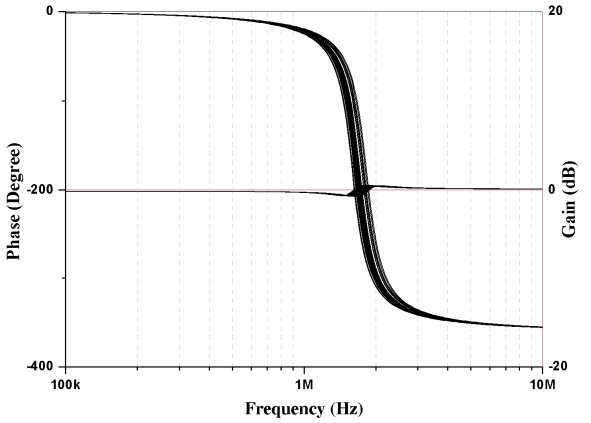

Fig. 9. Monte-Carlo analysis for the phase and gain responses for 10% Gaussian change in the I_f's current source values.

Monte-Carlo analysis is also applied to MOS transistor process parameters. According to this simulation 0.5% Gaussian change in the zero-bias threshold voltage (VTO) and transconductance coefficient (KP) are applied to all NMOS and PMOS transistors in the circuit at the same time. Obtained phase and gain responses of the filter are given in Fig. 10.

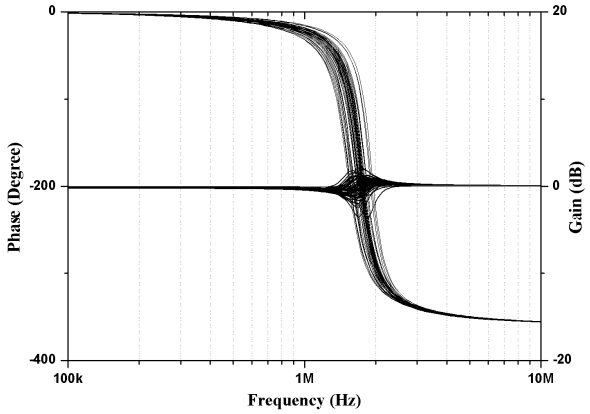

Fig. 10. Monte-Carlo analysis for the phase and gain responses for 0.5% Gaussian change in the process parameters of all transistors.

In the proposed circuit, MOS transistors' variation is also studied by using PSpice program. According to analysis results, dimensions (W) of all NMOS transistors are changed 1% in the circuit and the obtained phase and gain responses are given in Fig. 11.

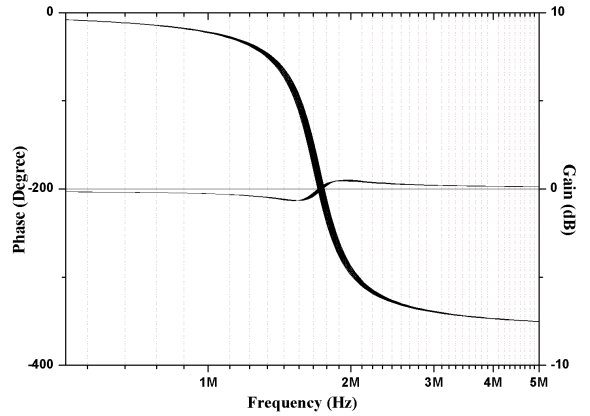

Fig. 11. Gain and Phase responses when all NMOS transistor dimensions (W) are changed 1%.

Noise analysis of the proposed circuit is performed for $Q = 5$. Obtained output noise performance is given in Fig. 12. Also the proposed filter's total power dissipation is calculated as 9.67 mW.

The proposed second order all-pass filter is operated for different quality factor, by changing dimensions of transistors M3, M12, M13, M16, M17, M18, M19 and M23. Dimensions of those are given in Tab. 3 for different quality factors between 3 and 10. The filter is analyzed in PSpice for pole frequency of 3.9 MHz. Obtained phase responses are given in Fig. 13.

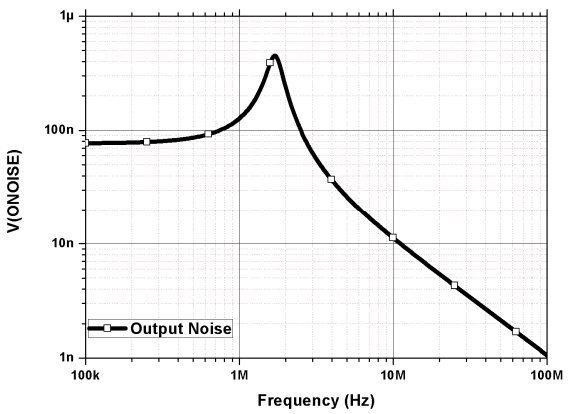

Fig. 12. Output noise of second order all-pass filter.

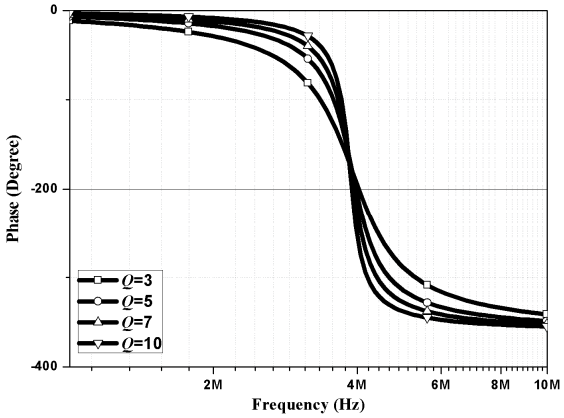

Fig. 13. Phase response of Fig. 3 for different quality factors.

Transistor	Quality Factor							
	Q= 3		Q = 5		Q = 7		Q = 10	
	W(µm)	L(µm)	W(µm)	L(µm)	W(µm)	L(µm)	W(µm)	L(µm)
M3	22.2	0.7	22.4	0.7	22	0.7	21.6	0.7
M12	2	0.7	1.2	0.7	1.7	0.7	1.2	0.7
M13	6	0.7	6	0.7	12	0.7	12	0.7
M16	36	0.7	36	0.7	36	0.7	70	0.7
M17	36	0.7	36	0.7	36	0.7	70	0.7
M18	8	0.7	2.9	0.7	1.5	0.7	1.4	0.7
M19	4	0.7	2.4	0.7	1.7	0.7	1.2	0.7
M23	2	0.7	3.6	0.7	4.3	0.7	4.8	0.7

Tab. 3. Dimensions of the MOS transistors in Fig. 3 for different quality factors.

4. Conclusions

In this paper, a second order SRD all-pass filter circuit is designed. The proposed filter is synthesized by using the state-space method and by adopting translinear circuits. The proposed SRD circuit has following advantages: (a) Pole frequency of the filter can be changed electronically by adjusting the values of DC current sources only. (b) The circuit has canonical number of capacitors which are grounded. (c) The filter does not suffer from disadvantages of use of resistors in IC process. (d) The filter has high quality factor. Only analysis results for Q = 5 are given. It can be operated for different high quality factors by changing dimension of any transistors. (e) The filter has high input impedance. The filter is simulated in PSpice for transient, AC, Monte-Carlo, noise and THD analysis. Obtained results show that the measured total harmonic distortions are less than 4% and total power dissipation is 9.67 mW. Obtained results are sufficient for analog integrated circuit design.

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