Low-Voltage MOS Current Mode Logic Multiplexer

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Abstract: *In this paper, a new low-voltage MOS current mode logic (MCML) multiplexer based on the triple-tail cell concept is proposed. An analytical model for static parameters is formulated and is applied to develop a design approach for the proposed low-voltage MCML multiplexer. The delay of the proposed low-voltage MCML multiplexer is expressed in terms of the bias current and the voltage swing so that it can be traded off with the power consumption. The proposed low-voltage MCML multiplexer is analyzed for the three design cases namely high-speed, power-efficient, and low-power. Finally, a comparison in performance of the proposed low-voltage MCML multiplexer with the traditional MCML multiplexer is carried out for all the cases.*

Keywords

MOS current mode logic, low-voltage, triple-tail cell.

1. Introduction

The rapid advances in the VLSI technology have led to the development of high-resolution mixed-signal applications [1]-[2]. These applications demand high performance digital circuits to be integrated with analog circuitry on the same chip. The traditional CMOS logic style is not suitable as it generates a large amount of switching noise [3]-[4]. Many alternative logic styles have been suggested in literature [5]-[12]. Among them, MOS current mode logic (MCML) style is the most preferred option for high-resolution mixed-signal integrated circuits due to the reduced switching noise [12]-[13]. Also, MCML style exhibits better power-delay than CMOS at high frequencies [14]-[15]. Hence, MCML is suitable for designing high-speed communication systems [15]-[21] wherein a multiplexer is a key element for serialization of parallel data during transmission.

The implementation of traditional MCML multiplexer is based on the series-gating approach (i.e. stacked source-coupled transistor pairs) [22]. This approach requires that all the stacked transistor pairs should operate in saturation region thereby limiting the power supply requirement. The power supply may however be lowered by reducing the number of stacked transistor pair levels with triple-tail cell concept [23]-[27]. In this paper, a new low-voltage MCML multiplexer based on the triple-tail cell concept is proposed. An analytical model for static parameters is formulated and is used to size transistors of the proposed low-voltage multiplexer. From the knowledge of the transistor sizes, the delay is expressed in terms of the bias current and the voltage swing so that it can be traded off with the power consumption. Then, the proposed low-voltage multiplexer for high-speed, power-efficient and low-power design cases is illustrated and finally its performance is compared with the traditional MCML multiplexer for each case.

In this paper, the operation of the traditional MCML multiplexer is briefly reviewed in Section 2. Then, the new low-voltage MCML multiplexer is proposed and its analytical formulations for different static parameters and delay are presented in Section 3. The analysis of the proposed multiplexer for the three design cases, namely high-speed, power-efficient, and low-power, and its performance comparison with the traditional MCML multiplexer is discussed in Section 4. Finally, the paper is concluded in Section 5.

2. Traditional MCML Multiplexer

A traditional 2:1 multiplexer with differential inputs, namely SEL A and B is shown in Fig. 1 [28]. It consists of two levels of source-coupled transistor pairs to implement the logic function and a constant current source M_{TR1} to generate bias current I_{SS}. The differential SEL input drives the lower level transistor pair M_{TR2}-M_{TR3} that alternatively activates the upper level transistor pairs M_{TR4}-M_{TR5} and M_{TR6}-M_{TR7}. When differential input SEL is high, M_{TR3} is off, the bias current I_{SS} flows through M_{TR2} and is steered either to M_{TR4} or M_{TR5} according to the differential input A. Conversely, when differential input SEL is low, the bias current I_{SS} flows through M_{TR3} and is steered to one of the two transistors, i.e. either M_{TR6} or M_{TR7} depending on the differential input B. The bias current I_{SS} is converted to the differential output voltage ($V_Q - \overline{V_Q}$) through the transistors M_{TR8} and M_{TR9} [28]. The load capacitance C_L includes the effect of fanout, and the interconnect capacitances.

The minimum supply voltage, $V_{DD\_MIN\_TR}$ for the traditional multiplexer is defined as the lowest voltage at which all the transistors in the two levels and the current source operate in the saturation region [29] and has been computed as

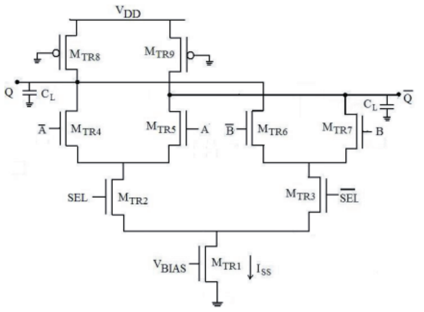

Fig. 1. Traditional MCML 2:1 multiplexer.

$$V_{DD\_MIN\_TR} = 3V_{BIAS} - 3V_{T\_TR1} + V_{T\_TR} \tag{1}$$

where V_{T_TR} is the threshold voltage of the transistors $M_{TR4,5,6,7}$, V_{T_TR1} is the threshold voltage of M_{TR1}, V_{BIAS} is the biasing voltage of M_{TR1}.

3. Proposed Low-voltage MCML Multiplexer

The proposed low-voltage 2:1 multiplexer with differential inputs, namely SEL A and B, is shown in Fig. 2. It consists of two triple-tail cells (M_{LV3}, M_{LV4}, M_{LV7}) and (M_{LV5}, M_{LV6}, M_{LV8}) biased by separate current sources of $I_{SS}/2$ value. The transistors M_{LV7} and M_{LV8} are driven by the differential SEL input and are connected between the supply terminal and the common source terminal of transistor pairs M_{LV3}-M_{LV4} and M_{LV5}-M_{LV6} respectively. A high differential SEL voltage turns on the transistor M_{LV8}, and deactivates the transistor pair M_{LV5}-M_{LV6}. At the same time, the transistor M_{LV7} turns off so that the transistor pair M_{LV3}-M_{LV4} generates the output according to the differential input A. Similarly, the transistor pair M_{LV5}-M_{LV6} gets activated for low differential SEL voltage and produces the output corresponding to the differential input B.

The minimum supply voltage, $V_{DD\_MIN\_LV}$ for the proposed multiplexer has been computed by the method outlined in [29] as

$$V_{DD\_MIN\_LV} = 2V_{BIAS} - 2V_{T\_LV1} + V_{T\_LV} \tag{2}$$

where V_{T_LV} is the threshold voltage of transistor $M_{LV3,4,5,6}$, V_{T_LV1} is the threshold voltage of M_{LV1}, V_{BIAS} is the biasing voltage of M_{LV1}.

3.1 Static Model

The static model has been derived by modeling the load transistors M_{LV9}, M_{LV10} by an equivalent linear resistance, R_p [30]. Using the standard BSIM3v3 model, the linear resistance R_p has been computed as

$$Rp = \frac{R\text{int}}{1 - \dfrac{\left(R_{DSW} \cdot 1 \cdot 10^{-6}\right)/W_P}{R_{int}}} \tag{3}$$

where R_{DSW} is the empirical model parameter, W_P is the channel width of the load transistor and the parameter R_{int} is the intrinsic resistance of the PMOS transistor in the linear region and is given as

$$R_{int} = \left[\mu_{eff,p} C_{ox} \frac{W_P}{L_P}\left(V_{DD} - \left|V_{T,p}\right|\right)\right]^{-1} \tag{4}$$

where C_{ox} is the oxide capacitance per unit area. The parameters $\mu_{eff,p}$, $V_{T,p}$ and L_P are the effective hole mobility, the threshold voltage and the effective channel length of the load transistor, respectively.

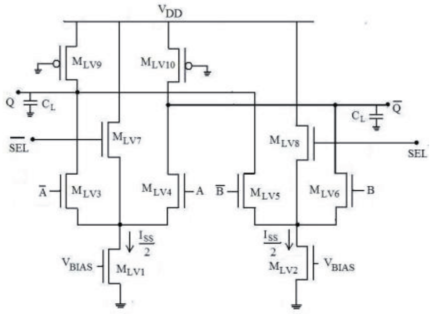

Fig. 2. Proposed low-voltage 2:1 multiplexer.

It may be noted that if equal aspect ratio of all transistors in the triple tail cells is considered, then the transistors M_{LV7} and M_{LV8} will not be able to completely switch off the transistor pair M_{LV3}-M_{LV4} and M_{LV5}-M_{LV6}. Hence, for proper operation, the aspect ratio of transistors M_{LV7}, M_{LV8} is made greater than other transistors' aspect ratio by a factor N. As an example if the value of differential inputs A and B is chosen such that the transistors M_{LV3}, M_{LV5} are on while the transistors M_{LV4}, M_{LV6} are off. Then, a high differential SEL voltage turns on the transistor M_{LV8} and deactivates the transistor pair M_{LV5}-M_{LV6}. But since the transistors M_{LV8} and M_{LV5} have the same gate-source voltages, the currents flowing through M_{LV5} ($i_{D,5}$) and M_{LV8} ($i_{D,8}$) can be written as

$$i_{D,5} = \frac{I_{SS}}{2}\frac{1}{1+N}, \tag{5a}$$

$$i_{D,8} = \frac{I_{SS}}{2}\frac{N}{1+N}. \tag{5b}$$

The current through M_{LV5} can be minimized by increasing factor N. This input condition produces minimum output voltage V_{OL} as

$$\begin{aligned} V_{OL} &= V_Q - \overline{V}_Q = R_p\left[\left(i_{D,4} + i_{D,6}\right) - \left(i_{D,3} + i_{D,5}\right)\right] \\ &= -\frac{R_p I_{SS}}{2}\left(1 + \frac{1}{1+N}\right) \end{aligned} \tag{6}$$

where $i_{D,3}$, $i_{D,4}$, $i_{D,5}$, $i_{D,6}$ are the currents through transistors M_{LV3}, M_{LV4}, M_{LV5}, M_{LV6} respectively. The differential output voltages for various input combinations are enlisted in Tab. 1. It can be observed from Tab. 1 that there are two values of both maximum output voltage V_{OH} and minimum output voltage V_{OL} for different input combinations. Consequently, the voltage swing, V_{SWING1} for the same differential inputs (A and B) can be expressed as

Differential inputs			Currents through the transistors						Differential output $\left(V_Q - \overline{V}_Q\right)$	
SEL	**A**	**B**	M_{LV3}	M_{LV4}	M_{LV5}	M_{LV6}	M_{LV7}	M_{LV8}	**Level**	$R_P\left[\left(i_{D,4}+i_{D,6}\right)-\left(i_{D,3}+i_{D,5}\right)\right]$
L	L	L	I_3	0	I_1	0	I_2	0	V_{OL1}	$-R_P\frac{I_{SS}}{2}\left(1+\frac{1}{1+N}\right)$
	L	H	I_3	0	0	I_1	I_2	0	V_{OH2}	$R_P\frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$
	H	L	0	I_3	I_1	0	I_2	0	V_{OL2}	$-R_P\frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$
	H	H	0	I_3	0	I_1	I_2	0	V_{OH1}	$R_P\frac{I_{SS}}{2}\left(1+\frac{1}{1+N}\right)$
H	L	L	I_1	0	I_3	0	0	I_2	V_{OL1}	$-R_P\frac{I_{SS}}{2}\left(1+\frac{1}{1+N}\right)$
	L	H	I_1	0	0	I_3	0	I_2	V_{OL2}	$-R_P\frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$
	H	L	0	I_1	I_3	0	0	I_2	V_{OH2}	$R_P\frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$
	H	H	0	I_1	0	I_3	0	I_2	V_{OH1}	$R_P\frac{I_{SS}}{2}\left(1+\frac{1}{1+N}\right)$

Tab. 1. Differential output voltages for various input combinations. L/H= low/high differential input voltage. $I_1 = I_{SS}/2$, $I_2 = I_{SS}/2\ (N/(1+N))$, $I_3 = I_{SS}/2\ (1/(1+N))$.

$$V_{SWING1} = V_{OH1} - V_{OL1} = R_p I_{SS}\left(1+\frac{1}{1+N}\right) \tag{7a}$$

where V_{OH1}, V_{OL1} are maximum output voltage and minimum output voltage respectively for the same differential inputs. The voltage swing, V_{SWING2} for the different differential inputs (A and B) can be expressed as

$$V_{SWING2} = V_{OH2} - V_{OL2} = R_p I_{SS}\left(\frac{N}{1+N}\right) \tag{7b}$$

where V_{OH2}, V_{OL2} are maximum output voltage and minimum output voltage respectively for different differential inputs.

As $V_{SWING2} < V_{SWING1}$, V_{SWING2} has been considered as the worst case voltage swing, V_{SWING} and has been further approximated as

$$V_{SWING} = R_p I_{SS} \text{ for large values of } N. \tag{8}$$

The small-signal voltage gain (A_V) and noise margin (NM) for the proposed multiplexer have been computed by the method outlined in [30] as

$$A_V = g_{m,n} R_p = \frac{V_{SWING}}{2}\sqrt{2\mu_{eff,n} C_{OX} \frac{W_N}{L_N}\frac{1}{I_{SS}}}, \tag{9}$$

$$NM = \frac{V_{SWING}}{2}\left[1-\frac{\sqrt{2}}{A_V}\right] \tag{10}$$

where $\mu_{eff,n}$, $g_{m,n}$, W_N and L_N are the effective electron mobility, the transconductance, the effective channel width and length of transistors $M_{LV3,4,5,6}$ respectively.

3.2 Transistor Sizing

In this section, an approach to size the transistors of the proposed multiplexer based on the static model is developed. For a specified value of NM and A_V (> 1.4 for MCML [31]), the voltage swing of the proposed multiplexer has been calculated using (10) as

$$V_{SWING} = \frac{2NM}{1-\frac{\sqrt{2}}{A_V}}. \tag{11}$$

It may be noted that V_{SWING} should be lower than the maximum value of 2 V_T so as to ensure that transistors $M_{LV3,4,5,6}$ operates in saturation region. The voltage swing obtained from (11) requires sizing of the load transistor with equivalent resistance R_p (= V_{SWING}/I_{SS}). To this end, the equivalent resistance, R_{P_MIN}, for the minimum sized PMOS transistor is first determined and then the bias current I_{HIGH} for the required voltage swing is determined as

$$I_{HIGH} = \frac{V_{SWING}}{R_{P\_MIN}}. \tag{12}$$

If the bias current is higher than I_{HIGH}, then R_P should be less than R_{P_MIN} and this is achieved by setting L_P to its minimum value i.e. L_{MIN} and W_P which is calculated by solving (3) and (4) as

$$W_p = \frac{I_{SS}}{V_{SWING}} \cdot \frac{L_{MIN}}{\mu_{eff,p} C_{OX}\left(V_{DD}-\left|V_{T,p}\right|\right)\left\{1-\frac{R_{DSW}\cdot 10^{-6}}{L_{MIN}}\left[\mu_{eff,p} C_{OX}\left(V_{DD}-\left|V_{T,p}\right|\right)\right]\right\}}. \tag{13}$$

Simulation Condition: $A_V = 4$, $V_{SWING} = 0.4$ V, $C_L = 50$ fF, $I_{SS} = 100$ µA						
Parameter	NMOS / PMOS	T / T	F / F	S / S	F / S	S / F
V_{SWING} (mV)	Proposed	344	481	260	430	350
	Traditional	366	465	267	378	370
A_V	Proposed	3.1	2.1	5.2	3.1	3.1
	Traditional	3.2	2.1	4.3	3.1	3.1
NM (mV)	Proposed	94.2	78.5	94.6	116.6	95.4
	Traditional	100.6	76.7	90	103.1	101.1
Simulation Condition: $A_V = 4$, $V_{SWING} = 0.4$ V, $C_L = 50$ fF, $I_{SS} = 10$ µA						
V_{SWING} (mV)	Proposed	410	498	265	420	415
	Traditional	342	519	294	443	407
A_V	Proposed	3.8	1.9	5.5	2.9	3.7
	Traditional	2.98	1.81	4.39	2.67	2.81
NM (mV)	Proposed	130.2	63.6	98.9	110.6	129.4
	Traditional	89.8	56.7	99.6	104.2	101.1

Tab. 2. Effect of process variation on static parameters. Different design corners are denoted by T = Typical, F= Fast, S= Slow.

Similarly, if the bias current is lower than I_{HIGH}, then R_P should be greater than R_{P_MIN} which is achieved by setting W_P to its minimum value i.e. W_{MIN}, and L_P which is calculated by solving (3) and (4) as

$$L_p = W_{MIN}\mu_{eff,p}C_{OX}\left(V_{DD} - \left|V_{T,p}\right|\right)\left(\frac{V_{SWING}}{I_{SS}} - \frac{R_{DSW}\cdot 10^{-6}}{W_{MIN}}\right). \quad (14)$$

The small-signal voltage gain (A_V) computed in (9) has been used to size transistors $M_{LV3,4,5,6}$. Assuming minimum channel length for the said transistors, the width has been computed as

$$W_N = \frac{2}{\mu_{eff,n}C_{OX}}\left(\frac{A_V}{V_{SWING}}\right)^2 I_{SS}L_{MIN}. \quad (15)$$

Sometimes (15) results in a value of W_N smaller than the minimum channel width. This happens when the bias current is lower than the current of the minimum sized NMOS transistor, I_{LOW} given as

$$I_{LOW} = \frac{1}{2}\frac{W_{MIN}}{L_{MIN}}\mu_{eff,n}C_{OX}\left(\frac{V_{SWING}}{A_V}\right)^2. \quad (16)$$

Therefore, in such cases, W_N is also set to W_{MIN}.

The accuracy of the static model for the proposed multiplexer has been validated through SPICE simulations by using TSMC 0.18 µm CMOS process parameters. The proposed multiplexer is designed for wide range of operating conditions: voltage swing of 300 mV and 400 mV, small-signal voltage gain of 2 and 4, and the bias current ranging from 10 µA to 100 µA.

The designs were simulated and the error in simulated and theoretical values for voltage swing, small-signal voltage gain and noise margin using equations (8), (9) and (10) respectively are calculated and are plotted in Fig. 3. It may be noted that maximum error in voltage swing, small-signal voltage gain and noise margin are 16 %, 15 % and 19 % respectively.

The impact of parameter variation on the proposed low-voltage and traditional MCML multiplexer performance is studied at different design corners. The findings for various operating conditions are given in Tab. 2. It is found that the voltage swing, small-signal voltage gain, and noise margin of the proposed low-voltage multiplexer varies by a factor of 1.87, 2.94, and 2.28 respectively between the best and the worst cases. For the traditional MCML multiplexer, the voltage swing, small-signal voltage gain, and noise margin varies by a factor of 1.76, 2.42, and 1.8 respectively between the best and the worst cases. Thus, the proposed low-voltage multiplexer shows slightly higher variations than the traditional MCML multiplexer for different design corners which can be attributed to the smaller aspect ratio of transistors in the proposed low-voltage multiplexer [31].

The effect of temperature variation on proposed low-voltage and traditional MCML multiplexers performance is studied for a typical process corner. The results are shown in Tab. 3. It is found that the voltage swing, small-signal voltage gain, and noise margin of the proposed low-voltage multiplexer varies by about 0.025 %/°C, 0.17 %/°C and 0.122 %/°C respectively. For the traditional MCML multiplexer, the voltage swing, small-signal voltage gain, and noise margin varies by about 0.022 %/°C, 0.11 %/°C and 0.098 %/°C respectively. Thus, the proposed low-voltage multiplexer shows slightly higher variations than the traditional MCML multiplexer.

3.3 Delay Model

In this section, a delay model of the proposed multiplexer is formulated in terms of bias current and voltage swing. There are two delay parameters, namely select to Q (SEL-Q) and input to Q (A-Q or B-Q), described for a multiplexer. The SEL-Q delay is evaluated when SEL changes with constant inputs (A and B) whereas A-Q (B-Q) delay is evaluated when A (B) switches while SEL remains constant. However in practical cases, the SEL-Q delay is prominent and is therefore considered for further discussion.

Simulation Condition: $A_V = 4$, $V_{SWING} = 0.4$ V, $C_L = 50$ fF, $I_{SS} = 100$ µA				
Parameter \ Temp (°C)		0°	70°	125°
V_{SWING} (mV)	Proposed	387	394	399
	Traditional	386	392	396
A_V	Proposed	3.6	4.0	4.3
	Traditional	3.58	3.9	4.1
NM (mV)	Proposed	117	127	134.8
	Traditional	116	124	130.21

Tab. 3. Effect of temperature variations on static parameters.

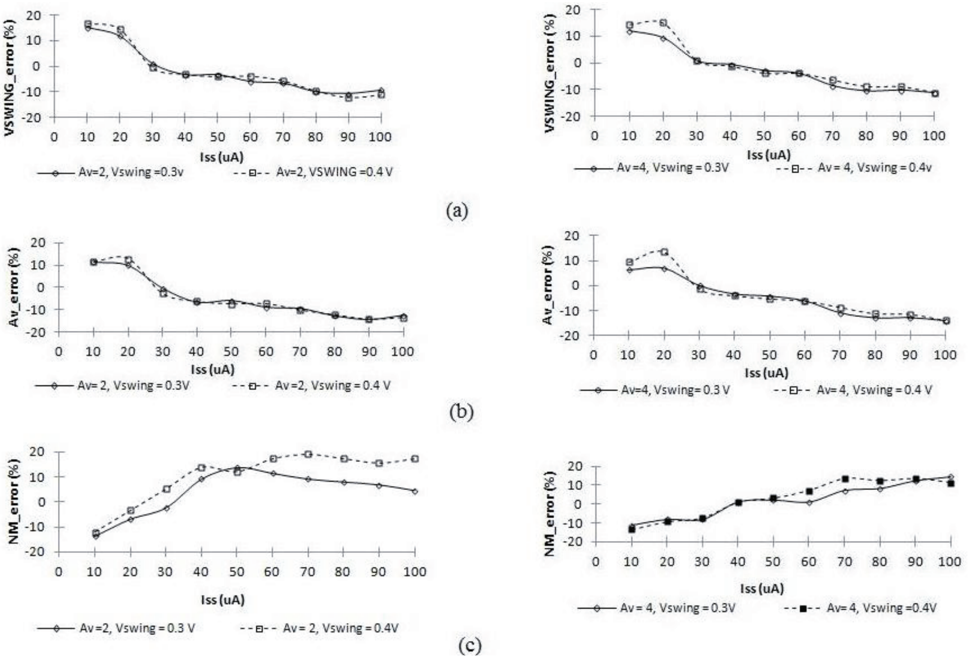

Fig. 3. Error in the static parameters versus I_{SS} for different values of V_{SWING} and Av, (a) V_{SWING}, (b) Av, (c) NM.

In case of a low-to-high transition on SEL input that causes output to switch by activating (deactivating) the transistor pair M_{LV3}-M_{LV4} (M_{LV5}-M_{LV6}), the circuit reduces to a simple MCML inverter. The equivalent linear half circuit is shown in Fig. 4 where C_{gdi}, C_{dbi} represent the gate-drain capacitance and the drain-bulk junction capacitance of the i^{th} transistor. For NMOS transistors operating in saturation region, C_{gd} is equal to the overlap capacitance $C_{gdo}W_n$ between the gate and the drain where C_{gdo} is the drain-gate overlap capacitance per unit transistor width [30]. For the PMOS transistor operating in linear region, C_{gd} is evaluated as the sum of the overlap capacitance and the intrinsic contribution associated with its channel charge [30]. The junction capacitance C_{db} for the transistors has been computed as explained in [32].

The SEL-Q delay (t_{PD_SEL}) of the proposed multiplexer can be expressed as

$$t_{PD\_SEL} = 0.69Rp \cdot \left(C_{db3} + C_{gd3} + C_{gd9} + C_{db9} + C_{db5} + C_{gd5} + C_L\right) \quad (17)$$

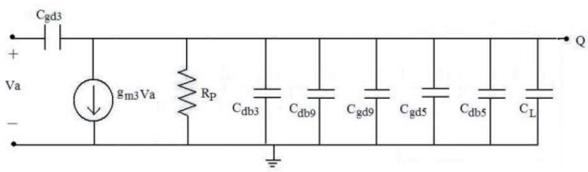

Fig. 4. Linear half-circuit (with low differential input A).

with

$C_{db3} = C_{db5}$, $C_{gd3} = C_{gd5}$ and $R_P = \frac{V_{SWING}}{I_{SS}}$, (17) can be rewritten as

$$t_{PD\_SEL} = 0.69\frac{V_{SWING}}{I_{SS}} \cdot \left(2C_{db3} + 2C_{gd3} + C_{gd9} + C_{db9} + C_L\right). \quad (18)$$

The capacitances may be expressed in terms of bias current and voltage swing as

$$C_{\rm xy} = \frac{a_{\rm xy}}{(V_{\rm SWING})^2} I_{\rm SS} + b_{\rm xy}\frac{V_{\rm SWING}}{I_{\rm SS}} + c_{\rm xy}$$

where C_{xy} is the capacitance between the terminals x and y and a_{xy}, b_{xy}, c_{xy} are the associated coefficients. Using (14) and (15), various capacitances in (18) for I_{SS} ranging from I_{LOW} to I_{HIGH} have been expressed as

$$C_{\rm gd3} = C_{\rm gdo} W_3 = 2A_V^2 C_{\rm gdo}\frac{L_{\rm MIN}}{\mu_{\rm eff,n} c_{\rm OX}}\frac{I_{\rm SS}}{(V_{\rm SWING})^2}, \tag{20}$$

$$C_{\rm db3} = W_3\left(K_{\rm jn}C_{\rm jn}L_{\rm dn} + 2K_{\rm jswn}C_{\rm jswn}\right) + 2K_{\rm jswn}C_{\rm jswn}L_{\rm dn} \tag{21}$$

$$= 2A_V^2\frac{L_{\rm MIN}}{\mu_{\rm eff,n}C_{OX}}\left(K_{\rm jn}C_{\rm jn}L_{\rm dn} + 2K_{\rm jswn}C_{\rm jswn}\right)\frac{I_{\rm SS}}{(V_{\rm SWING})^2} + 2K_{\rm jswn}C_{\rm jswn}L_{\rm dn} \tag{22}$$

where C_{jn}, C_{jswn} are the zero-bias junction capacitance per unit area and zero-bias sidewall capacitance per unit parameter respectively. The coefficients K_{jn}, K_{jswn} are the voltage equivalence factor for the junction and the sidewall capacitances of the NMOS transistor respectively [32]. Parameter L_{dn} is extrapolated from design rules [22].

$$C_{\rm gd9} = C_{\rm gdo}W_{\rm MIN} + \frac{3}{4}A_{\rm bulk,max}W_{\rm MIN}L_{\rm P}C_{\rm OX} \tag{23}$$

$$= C_{\rm gdo}W_{\rm MIN} + \frac{3}{4}A_{\rm bulk,max}W_{\rm MIN}C_{\rm OX}\cdot \left\{\mu_{\rm eff,p}C_{\rm OX}W_{\rm MIN}\left(V_{\rm DD} - \left|V_{\rm T,p}\right|\right)\left[\frac{V_{\rm SWING}}{I_{\rm SS}} - \frac{R_{\rm DSW}10^{-6}}{W_{\rm MIN}}\right]\right\} \tag{24}$$

where $A_{bulk,max}$ is a parameter defined in BSIM3v3 model [28].

$$C_{\rm db9} = W_{\rm MIN}\left(K_{\rm jp}C_{\rm jp}L_{\rm dp} + 2K_{\rm jswp}C_{\rm jswp}\right) + 2K_{\rm jswp}C_{\rm jswp}L_{\rm dp} \tag{25}$$

where C_{jp}, C_{jswp} are the zero-bias junction capacitance per unit area and zero-bias sidewall capacitance per unit parameter respectively. The coefficients K_{jp}, K_{jswp} are the voltage equivalence factor for the junction and the sidewall capacitances of the PMOS transistor respectively [32]. Parameter L_{db} is extrapolated from design rules [22].

The coefficients a_{xy}, b_{xy} and c_{xy} of all the capacitances in (18) are summarized in Tab. 4. Using equations (20) – (25), equation (18) can be written as

$$t_{\rm PD\_SEL} = 0.69V_{\rm SWING}\left(\frac{a}{V_{\rm SWING}^2} + b\frac{V_{\rm SWING}}{I_{\rm SS}^2} + \frac{c + C_{\rm L}}{I_{\rm SS}}\right) \tag{26}$$

where

$$a = 2a_{\rm db3} + 2a_{gd3}, \tag{27a}$$

$$b = b_{\rm gd9}, \tag{27b}$$

$$c = 2c_{\rm db3} + 2c_{gd9} + c_{\rm db9}. \tag{27c}$$

The delay model can also be used for I_{SS} value outside the range [I_{LOW}, I_{HIGH}]. This is because for $I_{SS} > I_{HIGH}$, the capacitance coefficients of PMOS transistor in (26) differ as explained in Section 3.2. But, since for high values of I_{SS}, the capacitive contribution of PMOS transistor is negligible, therefore (26) can predict the delay. Similarly, for $I_{SS} < I_{LOW}$, the capacitance coefficients of NMOS transistor in (26) differs. But, since for low values of I_{SS}, the delay majorly depends on the capacitances of PMOS transistor. So, the expression in (26) can estimate the delay of the proposed multiplexer.

The accuracy of the delay model for the proposed multiplexer has been validated through SPICE simulations by using TSMC 0.18 µm CMOS process parameters. The proposed multiplexer is designed for wide range of operating conditions: voltage swing of 300 mV and 400 mV, small-signal voltage gain of 2 and 4, bias current ranging from 10 µA to 100 µA, and load capacitance of 0 fF, 10 fF, 100 fF and 1 pF. It is found that there is a close agreement between the simulated and the predicted delay for all the operating conditions. The simulated and the predicted delay in particular for V_{SWING} = 400 mV, A_V= 4 and with different load capacitances are plotted in Fig. 5.

The impact of parameter variation on proposed low-voltage and traditional multiplexers delay is studied at different design corners. The findings for various operating conditions are given in Tab. 5. It is found that the propagation delay of the proposed low-voltage multiplexer varies by a factor of 1.89 between the best and the worst cases. For the traditional MCML multiplexer, the delay varies by a factor of 1.85 between the best and the worst cases. Thus, the proposed low-voltage multiplexer shows slightly higher variation than the traditional MCML multiplexer in delay for different design corners. The process variations are more prevalent in the designs with smaller aspect ratio [31] and the results for proposed low-voltage multiplexer conform to this fact.

The effect of temperature variation on proposed low-voltage and traditional MCML multiplexers delay is studied for a typical process corner. The results are shown in Tab. 6. It is found that delay of the proposed low-voltage multiplexer varies by about 1.2 %/°C. For the traditional MCML multiplexer the delay shows a variation of 1 %/°C. Thus, the proposed low-voltage multiplexer shows slightly higher variations than the traditional MCML multiplexer.

NMOS coefficients	
a_{db3}	$\frac{2A_V^2 L_{MIN}}{\mu_{eff,n} C_{OX}}\left(K_{jn}C_{jn}L_{dn} + 2K_{jswn}C_{jswn}\right)$
a_{gd3}	$2A_V^2 C_{gdo}\frac{L_{MIN}}{\mu_{eff,n}C_{OX}}$
c_{db3}	$2K_{jswn}C_{jswn}L_{dn}$
b_{db3}, b_{gd3}, c_{gd3}	0
PMOS coefficients	
b_{gd9}	$\frac{3}{4}A_{bulkmax}\mu_{eff,p}C_{OX}^2 W_{MIN}^2\left(V_{DD}-\lvert V_{T,p}\rvert\right)$
c_{gd9}	$C_{gdo}W_{MIN} - \frac{3}{4}A_{bulkmax}\mu_{eff,p}C_{OX}^2 W_{MIN}\left(V_{DD}-\lvert V_{T,p}\rvert\right)R_{DSW}10^{-6}$
c_{db9}	$K_{jp}C_{jp}L_{dp}W_{MIN}+2K_{jswp}C_{jswp}\left(L_{dp}+W_{MIN}\right)$
a_{gd9}, a_{db9}, b_{db9}	0

Tab. 4. The capacitance coefficients for the proposed multiplexer. The symbols have their usual meanings.

Simulation Condition: $A_V = 4$, $V_{SWING} = 0.4$ V, $C_L = 50$ fF, $I_{SS} = 100$ µA						
Parameter	NMOS / PMOS	T / T	F / F	S / S	F / S	S / F
t_{PD} (ps)	Proposed	265	237	448	255	262
	Traditional	553	515	954	527	550
Simulation Condition: $A_V = 4$, $V_{SWING} = 0.4$ V, $C_L = 50$ fF, $I_{SS} = 10$ µA						
t_{PD} (ns)	Proposed	2.4	1.7	3.2	2.1	2.3
	Traditional	3.7	3.2	4.6	3.5	3.6

Tab. 5. Effect of process variation on delay.

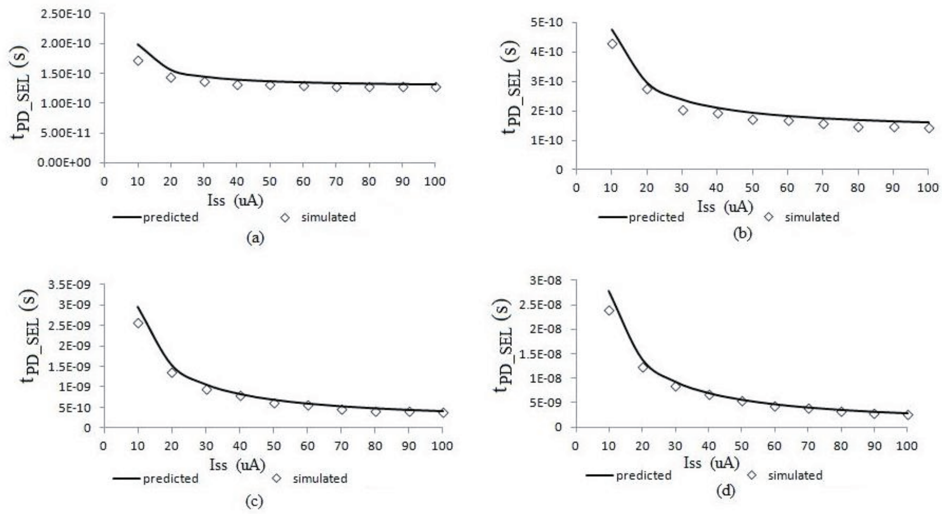

Fig. 5. Simulated and the predicted delay of the proposed low-voltage multiplexer versus I_{SS} with NM =130 mV, A_V= 4 for different C_L values: (a) 0 fF, (b) 10 fF, (c) 100 fF, (d) 1 pF.

Simulation Condition: $A_V = 4$, $V_{SWING} = 0.4$ V, $C_L = 50$ fF, $I_{SS} = 100$ µA				
Parameter \ Temp		0°	70°	125°
t_{PD} (ps)	Proposed	151	280	387
	Traditional	339	590	762

Tab. 6. Effect of temperature variation on delay.

4. Design Cases

In the previous section, the proposed multiplexer has been modeled and various parameters are expressed as a function of bias current and voltage swing. In practice, the voltage swing is set on the basis of the specified noise margin while the bias current is chosen according to power-delay considerations. Therefore, the proposed low-voltage multiplexer for high-speed, power-efficient, and low-power cases is discussed.

4.1 High-Speed Design

A high-speed design requires bias current that results in minimum delay. The delay in (26) decreases with the increasing I_{SS} and tends to an asymptotic minimum value of $0.69\cdot(a / V_{SWING})$ for $I_{SS} \to \infty$. A substantial improvement in delay with increasing bias current may be achieved if condition

$$\frac{a}{V_{SWING}^2} \geq b\frac{V_{SWING}}{I_{SS}^2} + \frac{c+C_L}{I_{SS}} \tag{28}$$

is satisfied. However, high value of bias current results in large transistor sizes. Therefore, the bias current should be set to such a value after which the improvement in speed is not significant. If equality sign in (28) is considered then the delay is close to its minimum value and the use of high bias current is avoided. Therefore, this assumption leads to a bias current (I_{SS_HS}) and delay (t_{PD_MIN}) as

$$I_{SS\_HS} = \frac{c+C_L}{2a}V_{SWING}^2\left(1+\sqrt{1+4\frac{ab}{\left(c+C_L\right)^2}\frac{1}{V_{SWING}}}\right), \tag{29}$$

$$t_{PD\_MIN} = 2\cdot 0.69\frac{a}{V_{SWING}}. \tag{30}$$

The proposed high-speed multiplexer designed with a noise margin of 130 mV, small-signal gain of 4, and load capacitance of 50 fF, gives I_{SS_HS} as 112 µA. A delay of 254 ps and 224 ps are obtained from (30) and simulations respectively. On the contrary, a traditional high-speed multiplexer designed using the method outlined in [28] for the same specifications results in a delay of 528 ps. This indicates that the proposed multiplexer can achieve much higher speed than the traditional one.

4.2 Power Efficient Design

A power efficient design requires bias current that results in minimum power-delay product (PDP). The power is calculated as the product of V_{DD} and I_{SS}. So, the PDP of the proposed multiplexer may be expressed as:

$$\mathrm{PDP} = 0.69V_{DD}V_{SWING}\left(\frac{a}{V_{SWING}^2}I_{SS} + b\frac{V_{SWING}}{I_{SS}} + c + C_L\right). \tag{31}$$

Therefore, the current I_{SS_PDP} for minimum PDP may be given as

$$I_{SS\_PDP} = \sqrt{\frac{b}{a}}\left(V_{SWING}\right)^{\frac{3}{2}}. \tag{32}$$

Accordingly, the minimum PDP results to

$$\mathrm{PDP} = 0.69V_{DD}V_{SWING}\left(\frac{2\sqrt{ab}}{\sqrt{V_{SWING}}} + c + C_L\right). \tag{33}$$

The proposed power-efficient multiplexer designed with a noise margin of 130 mV, small signal gain of 4, and load capacitance of 50 fF, gives I_{SS_PSP} as 4.5 µA. A PDP value of 19 fJ has been obtained for the proposed multiplexer. On the other hand, a traditional power-efficient multiplexer designed using the method outlined in [28] for the same specifications results in a PDP value of 13 fJ. The result signifies that the proposed multiplexer results in higher PDP values than the traditional one.

4.3 Low-Power Design

In low-power designs, the bias current I_{SS} is set to low values so that the term

$$b\frac{V_{SWING}}{I_{SS}^2}$$

is dominant in (26). Hence, the delay reduces to

$$t_{PD\_SEL} = 0.69b\left(\frac{V_{SWING}}{I_{SS}}\right)^2. \tag{34}$$

The proposed low-power multiplexer designed with a noise margin of 130 mV, small signal gain of 4, load capacitance of 5 fF, and with value of I_{SS} as 2 µA gives a power consumption of 2.2 µW while the traditional low-power multiplexer designed using the method outlined in [28] for the same specifications results in power consumption of 2.8 µW.

5. Conclusions

A new low-voltage MCML multiplexer based on the triple-tail cell concept is proposed. Its static parameters are analytically modeled and are used to develop a design approach for the proposed low-voltage MCML multiplexer. The delay is formulated as a function of the bias current and the voltage swing and is traded off with power consumption for high-speed, power-efficient, and low-power design cases. An improvement in performance is obtained for the proposed low-voltage multiplexer in comparison to traditional MCML multiplexer for high-speed and low-power design cases.

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