Novel Low Voltage CMOS Current Controlled Floating Resistor Using Differential Pair

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Abstract. *In this paper, a low voltage CMOS current controlled floating resistor which is convenient for integrated circuit implementation is designed by using differential pair. The proposed resistor has a simple circuit structure and low power dissipation. This circuit is required ±0.75 V as a power supply. The basic advantages of this circuit are wide tuning range of the resistance value, satisfied frequency performance and worthwhile dynamic range. As well as the proposed circuit has floating structure, it is able to be used both positive and negative resistor. The performances of the proposed circuit are simulated with SPICE to justify the presented theory.*

Keywords

CMOS active resistor, differential pair, low voltage circuits.

1. Introduction

It is mainly utilized resistor in analogue electronic circuits. However, owing to obtain resistance in silicon chip, it is necessary to detain large areas in the chip. This situation is not appropriate in terms of production efficiency. Also, these resistors, which are generated in the chip, may not provide determined resistance value. Because of these reasons, active resistor circuits are highly important for integrated circuits. It was introduced many varieties of active resistor and applications in previous studies [1-5].

Bipolar-based floating resistor was presented, such as class AB controlled resistor, resistor using operational tranconductance amplifier (OTA) based on bipolar transistor, in the literature [1-3]. Although these resistors have good frequency performance, the dynamic range of the circuit is restricted. Furthermore, the resistor circuits inherently consume more power compared with MOS-based active resistors. Active resistor using MOS transistors and its applications are introduced in the previous works [6-12]. But this resistor is limited in point of frequency response and adjustability.

On the other hand, active resistors using current conveyors are reported as different resistor designing techniques [13], [14]. But, these structures have passive components as resistor. Moreover, these circuits are inconvenient for integrated circuits (IC).

Tunable active resistors are controlled by using either voltage or current. Voltage controlled resistors (VCR) are introduced in [9-11]. VCRs present good dynamic range performance. But, adjustable range of the VCRs is restricted for generally utilized gate voltages as a control argument. Control voltage is limited by supply voltage. Current controlled resistors (CCR) provide facility to tune wide resistance value range [1-4]. This capability of the CCR is an important advantage for programmable analog circuit's applications. In additional, it can be interpreted that CCRs exhibit acceptable frequency performance. Also, VCRs having good linearity are presented in literature [15], [16]. But these proposed circuits require high supply voltage and have restricted control range comparing with CCRs.

Recently, low voltage disposition has been raised on electronic circuits design. Numerous electronic applications employing in the low voltage are introduced in the literature [17], [18]. Circuits using lower supply voltage allow operating in lower power dissipation. Low voltage active resistors and their applications are included in only a few studies in the literature [4], [10]. Floating gate MOS-based low voltage resistor is reported in [10]. But, this resistor is tuned by voltage and adjustable value range of the resistance is a few kΩs.

In this paper, floating active resistor is designed by utilizing CMOS differential pair. The resistor consists of only two differential pairs. Also, the circuit can be realized easily considering IC. This circuit is able to achieve both negative and positive resistance with small modification in the circuit. Control argument is biasing current for proposed circuit. Hereby, adjustable range of the resistance value is rather wide. The paper presents CMOS based current–controlled floating resistor operating at supply voltage of ±0.75 V. Therefore, power consumption of the circuit is at reasonable levels. The proposed circuits have been simulated using SPICE in 0.35 μm CMOS technology. Also, a bandpass filter is employed to demonstrate the capability of the proposed resistor.

2. Proposed Floating Active Resistor

Fig. 1 indicates differential pair as the core of floating resistor. Assuming that all the transistors are operated saturation region with their sources connected to the bulk. Drain currents of transistors M_A and M_B can be written as,

$$I_{DA} = \frac{1}{2}\mu_n C_{ox}(W/L)(V_{GSA} - V_{THN})^2, \quad (1.a)$$

$$I_{DB} = \frac{1}{2}\mu_n C_{ox}(W/L)(V_{GSB} - V_{THN})^2 \quad (1.b)$$

where μ_n is the electron mobility and C_{ox} is the oxide capacitance per unit area. I_{DA} and I_{DB} are the drain currents of transistors M_A and M_B, respectively. In addition, V_{THN} is the threshold voltage for the NMOS transistors. Transistor M_C utilizes to reduce impedance value at drain of transistor M_B. Therefore, the differential pair needs low supply voltage.

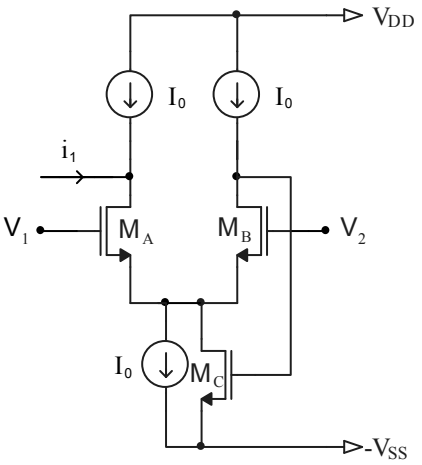

Fig. 1. The differential pair structure.

V_1 and V_2 are two input voltages applied at the gates as shown in Fig. 1. Input voltages are described as

$$V_1 - V_2 = V_{GSA} - V_{GSB} \quad (2)$$

where V_{GSA} and V_{GSB} are the gate voltages of transistors M_A and M_B, respectively. Drain current I_{DA} for transistor M_A is equal to $I_0 + i_1$ and drain current I_{DB} is similar to I_0. From (1) and (2), the difference of input voltages is given by

$$V_1 - V_2 = \sqrt{\frac{2(I_0 + i_1)}{\mu_n C_{ox}(W/L)}} - \sqrt{\frac{2I_0}{\mu_n C_{ox}(W/L)}}. \quad (3)$$

If equation (3) is arranged, current i_1 will be expressed as

$$i_1 = (V_1 - V_2)\sqrt{\frac{1}{2}k_n}\sqrt{4I_0 - \frac{1}{2}k_n(W/L)(V_1 - V_2)^2} \quad (4)$$

where $k_n = \mu_n C_{ox}$ is the transconductance parameter of the NMOS transistor. In (4), it is $4I_0 >> (1/2)k_n(W/L)(V_1\text{-}V_2)^2$. So, i_1 can be modified as

$$i_1 \cong (V_1 - V_2)\sqrt{\frac{1}{2}k_n(W/L)}\sqrt{4I_0}. \quad (5)$$

Equation (5) shows that i_1 depends on the biasing current I_0.

The body effect upon the channel of the NMOS transistors used in differential pair can be described using a modification of the threshold voltage, approximated by the following equation,

$$V_{THN} = V_{THNO} + \gamma\sqrt{2\varphi_B}\left[\sqrt{\left(1 - \frac{V_{BS}}{2\varphi_B}\right)} - 1\right] \quad (6)$$

where V_{THN} is the threshold voltage with substrate bias present, and V_{THNO} is the zero-V_{BS} value of threshold voltage, γ is the body effect parameter, and $2\varphi_B$ is the surface inversion potential of silicon and V_{BS} is the bulk-source voltage. Assume that V_{BS} is zero and gate bias is sufficient to insure that a channel is present, bulk effect can be neglected for differential pair in Fig. 1 [19].

If both inputs of the MOS differential pair structure are grounded, transistors M_A and M_B are perfectly matched and current i_1 would be zero. Practical circuits exhibit mismatch effect between the transistors. For the differential pair shown in Fig. 1, the effect of a mismatch in the *W/L* ratios of M_A and M_B, expressed as

$$\left(\frac{W}{L}\right)_A = \frac{W}{L} + \Delta\left(\frac{W}{L}\right), \quad (7.a)$$

$$\left(\frac{W}{L}\right)_B = \frac{W}{L}. \quad (7.b)$$

Effect of a mismatch ΔV_{THN} between the two threshold voltages are described as $V_{THNA} = V_{THN} + \Delta V_{THN}$ and $V_{THNB} = V_{THN}$. Therefore, offset current Δi_1 can be calculated as

$$\Delta i_1 = I_0\left(\frac{\Delta(W/L)}{W/L} + \frac{\Delta V_{THN}}{V_{GS} - V_{THN}}\right) \quad (8.a)$$

where V_{GS} is the gate-source voltage of the M_A and M_B. The offset current is extremely depended on the biasing current.

Fig. 2 indicates the proposed resistor using two differential pairs. M_1 and M_4, M_2 and M_3 are generated as differential pairs. All other transistors act as current mirror injected biasing current I_0. Using (5), resistance value of the resistor will be expressed as

$$R_{12} \cong \frac{(V_1 - V_2)}{i_1} = \frac{1}{\sqrt{2I_0 k_n(W/L)}} \quad (9)$$

where $i_2 = -i_1$, because differential pairs are connected in symmetric. It is obvious that resistance value is easily tuned by biasing current I_0.

Resistance value of the proposed circuit has change with temperature. PTAT current generator as biasing current of the proposed circuit can be used for temperature compensation. It is essential for ultra-low-power circuit realizations [20].

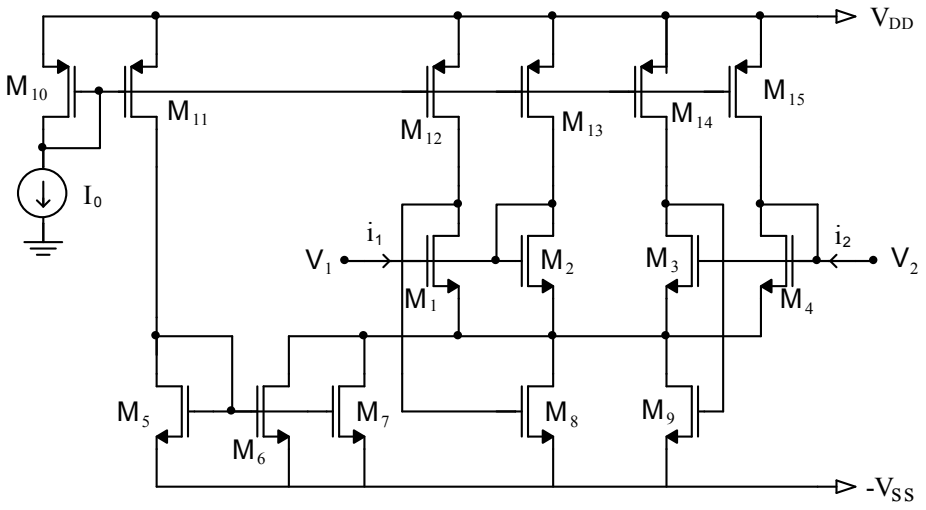

Fig. 2. Floating positive resistor.

All transistors of this circuit are aimed to operate in saturation region. M_8 and M_{12} remain in the saturation region if the following conditions are fulfilled:

$$(V_{DD}+V_{SS})-V_1-\sqrt{\frac{2(I_0+i_1)}{k_n(W/L)_{M2}}}-\sqrt{\frac{2(I_0)}{k_p(W/L)_{M13}}} \geq \sqrt{\frac{2(I_0+i_1)}{k_n(W/L)_{M8}}} \quad (10.a)$$

$$(V_{DD}+V_{SS})-\sqrt{\frac{2(I_0+i_1)}{k_n(W/L)_{M8}}}-V_{THN} \geq \sqrt{\frac{2(I_0)}{k_p(W/L)_{M12}}} \quad (10.b)$$

where $k_p = \mu_n C_{ox}$ is the transconductance parameter of PMOS transistors and V_{DD}, V_{SS} are supply voltages. In order to remain M_1 in the saturation region, the condition is:

$$(V_{DD}+V_{SS})-\sqrt{\frac{2(I_0)}{k_p(W/L)_{M12}}} \geq V_1+\sqrt{\frac{2(I_0+i_1)}{k_p(W/L)_{M2}}}-V_{THN} \quad (11)$$

In addition, M_2 and M_4 act as a diode. Also, the definitions in (10) and (11) valid for the other transistors generated differential pair. It seems that this resistor circuit can be operated in saturation region if $V_{DD} + V_{SS} > 2V_{DS,sat} + V_{THN}$ where $V_{DS,sat}$ is drain-to-source voltage for all transistors of the circuits in the saturation region.

The proposed positive resistor in Fig. 2 is easily able to be converted to the negative resistor. A connection is made between the drain of transistor M_2 and gates of M_3 instead of M_2's gate. Additionally, the drain of M_4 is connected to the gate of M_2 instead of M_4's gate. In this instance, it is clear that $i_1 = -i_2$. The definition of the negative resistance may be as follows:

$$R_{12} \cong \frac{(V_1-V_2)}{i_1} = -\frac{1}{\sqrt{2I_0k_n(W/L)}}. \quad (12)$$

Negative resistance is controlled by biasing current in the same way with the positive resistor. It is clear that the electronic adjustment of the resistance is offered by this circuit. Creating two different kinds of in a single circuit is one of the advantages of the proposed circuit.

3. Simulation Results

The proposed resistor was simulated by SPICE, owing to verify the theoretical approaches. The SPICE model 0.35 μm CMOS parameter for NMOS and PMOS is used in [21]. The supply voltage is ±0.75 V. Aspect ratio of the transistors is given in Tab. 1. Fig. 3 shows input differential voltage versus input current of the simulated resistor.

Transistor	W/L
M_1-M_4	2/0.7
M_5-M_{15}	30/0.7

Tab. 1. Aspect ratio of the transistors.

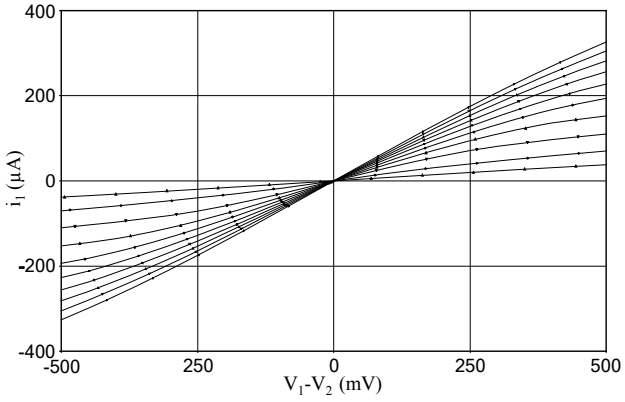

Fig. 3. Current / voltage characteristic of the proposed circuit.

The biasing current of the resistor is varied from 50 μA to 500 μA step by step. It is shown that behavior of the resistor is highly linear between -500 mV and +500 mV. The linearity of the proposed resistor depends on the linear range of the transconductance amplifier which consists of the differential pair. There are some circuit topologies exhibiting linear behavior in literature. But these circuits can be controlled by voltage and operate at high supply voltage comparing with our proposed circuit [22]. Resistance value of the proposed resistor can be easily tuned by biasing current of the circuit as shown in Fig. 3.

Frequency response of the circuit seen in Fig. 2 is shown in Fig. 4. The variation of the resistance magnitude with frequency for a biasing current of 50 μA and resistance value of 12.4 kΩ is illustrated in Fig. 4.

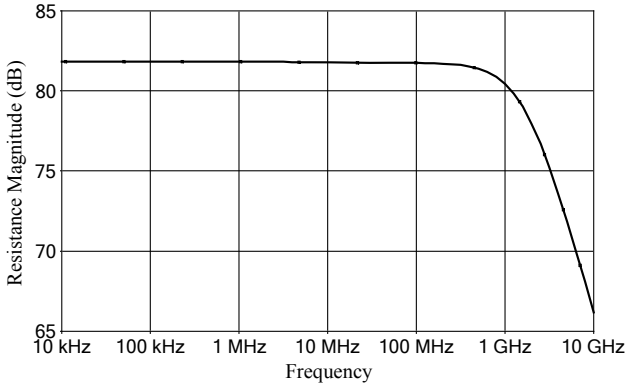

Fig. 4. Frequency response of the proposed circuit.

The variation of the total harmonic distortion with peak to peak input voltage for $I_0 = 50$ μA and $R_{12} =$ 12.4 kΩ is displayed in Fig. 5.

When the frequencies were increased, it was found that the proposed structure could be operated with the –3dB bandwidth of about 1.66 GHz. This circuit exhibits a good performance in terms of the frequency response.

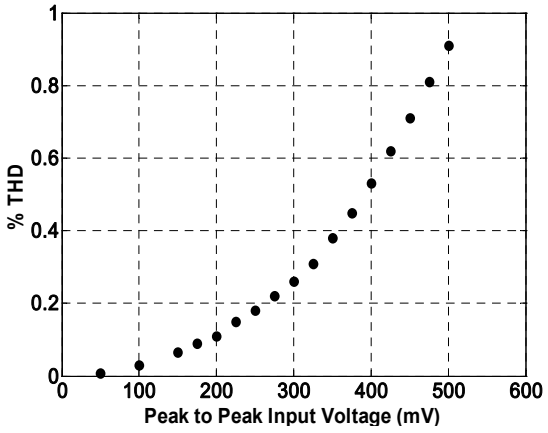

Fig. 5. THD % versus input voltage.

The variation of the THD with input signal amplitude for a biasing current of 50 μA is illustrated in Fig. 5. The THD value is 0.91 % at 500 mV. It is shown that THD values obtained according to different peak to peak input voltages are reasonable values. Also, the total power dissipation of the proposed circuit is 0.41 mW.

Comparison of the performance parameters belonging to some circuits and the proposed circuit is indicated in Tab. 2.

Parameters	This study	[3]	[10]	[4]
Supply voltage	±0.75 V	±1.5 V	±0.75 V	±3 V
Input range	±500 mV	±50 mV	±320 mV	±500 mV
Tuning range	1.5kΩ-1MΩ	250Ω-3kΩ	2kΩ-4kΩ	40kΩ-4MΩ
THD	0.91% (at1MHz)	0.24% (at1MHz)	0.28% (at 45 kHz)	1%
Power dissipation	0.41 mW	6.2 mW	0.254 mW	-
Bandwidth	1.66 GHz	35 MHz	-	-
Technology	CMOS	BJT	FGMOS	CMOS
Negative resistance	Yes	No	No	Yes
Floating	Yes	Yes	No	Yes

Tab. 2. Comparing of the active resistors' performance parameters.

When Tab. 2 is investigated, it is clear that the proposed circuit has some advantages. If the circuits are compared in terms of supply voltage, the proposed resistor and the circuit in [10] require a small supply voltage. Input range and tuning range of the proposed circuit are wider than those of the circuit in [10]. Although the circuit in [4] has wide tuning range, it uses high supply voltage considering the proposed circuit. Having a negative resistance is an important advantage for the proposed circuit. Also, frequency performance of the proposed resistor is elegant.

4. Bandpass Filter Application

As an application, in order to demonstrate the proposed resistor's capability, bandpass filter is used. Aforementioned filter structure is seen in Fig. 6.

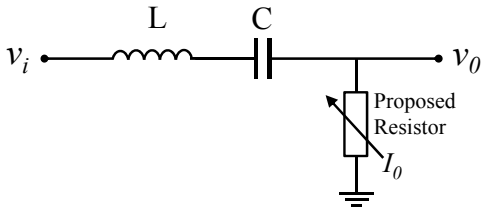

Fig. 6. Electronically tunable bandpass filter.

The circuit shown in Fig. 6 consists of a capacitor, inductor and current-controlled active resistor. The capacitance of the capacitor is 2.5 pF and inductance value is 0.1 mH. The center frequency of the circuit depends on L and C values. The center frequency is written as

$$w_0 = \frac{1}{\sqrt{LC}}. \tag{13}$$

The bandwidth (BW) of the filter can be defined as

$$BW = \frac{R(I_0)}{L} \tag{14}$$

where it is obvious that BW is the function of the proposed resistor. Also, the proposed resistor is defined as $R(I_0)$ in (14). The frequency response of the filter is shown in Fig. 7. As shown in Fig. 7 bandwidth of the filter can be easily adjust with changing biasing current of the proposed resistor.

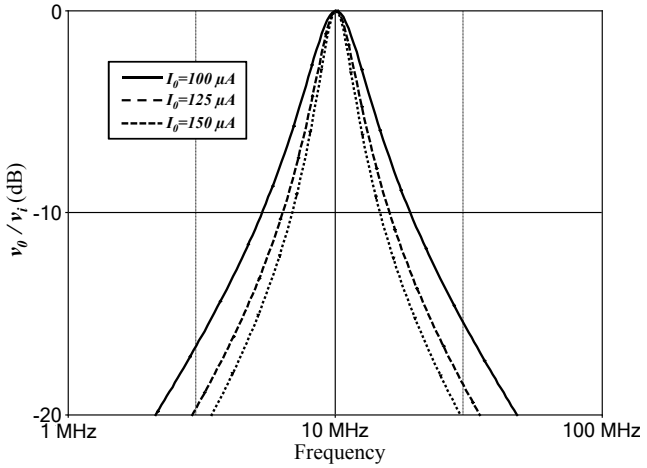

Fig. 7. Frequency response of the filter.

5. Conclusion

In this work, low voltage CMOS based active resistor structure is proposed and electronically tunable bandpass filter is tested as an application. The proposed circuit has no passive components which are excellent for IC implementations. In addition, the circuit has highly basic structure. The proposed circuit and bandpass filter are simulated using a Spice simulation program and to confirm the theory their simulation results are compared with the theoretical approaches. The value of the proposed resistance can be varied from 1.5 kΩ to 1 MΩ, with excellent correspondence between the theoretical and simulation results by changing the value of control current I_0.

Also, the proposed circuit is required a low voltage as well as ± 0.75 V. It is worthy for low power dissipation. Resistance of the active resistor can be obtained either positive or negative by using different connection structures as it is indicated in Section 2. Dynamic range of the resistor is wide as seen in Fig. 3. Also, thanks to the wide tuning range of the resistors, the proposed bandpass filter can be applied in a very wide frequency range. Finally, such a tunable behavior of the proposed circuit is an attractive feature in general electronic circuit designs and the circuit is rather convenient for low voltage IC realizations of which result in decreasing of power consumption.

References

[1] SENANI, R., SINGH, A., SINGH, V. K. A new floating current-controlled positive resistance using mixed translinear cells. *IEEE Transactions on Circuits and Systems II*, 2004, no. 51, p. 374–377.

[2] KHAN, A., AHMED, M. T. Realisation of tunable floating resistors. *Electronics Letters,* 17th July 1986, vol. 22, no. 15, p. 799-800.

[3] BARTHELEMY, M., FABRE, A. A new floating controlled resistance operating in class AB. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 2000, no. 47, p. 67–72.

[4] MANOLESCU, A., POPA, C. Low-voltage low-power improved linearity CMOS active resistor circuits. *Analog Integrated Circuits and Signal Processing*, 2010, vol. 62, no. 3, p. 373–387.

[5] ERCAN, H., TEKIN, S. A., ALÇI, M. Voltage- and current-controlled high CMRR instrumentation amplifier using CMOS current conveyors. *Turkish Journal of Electrical Engineering & Computer Sciences,* 2012, vol. 20, no. 4, p. 547–556.

[6] TAJALLI, A., LEBLEBICI, Y., BRAUER, E. J. Implementing ultra-high-value floating tunable CMOS resistors. *Electronics Letters*, 2008, vol. 44, no. 5, p. 349–350.

[7] MAUNDY, B., GIFT, S., ARONHIME P. Practical voltage/current-controlled grounded resistor with dynamic range extension. *IET Circuits Devices Syst.*, 2008, vol. 2, no. 2, p. 201–206.

[8] LANGLOIS, P., TAYLOR, J., DEMOSTHENOUS, A. Realization of a simple high-value grounded linear resistance in CMOS technology. In *Proceedings of ESSCIRC.* Grenoble (France), 2005, p. 383–386.

[9] KUSHIMA, M., INABA, M., TANNO, K., ISHIZUKA, O. Design of a floating node voltage-controlled linear variable resistor circuit. In *The 47th IEEE International Midwest Symposium on Circuits and Systems.* 2004, p. 1–5.

[10] GUPTA, M., PANDEY, R. FGMOS based voltage-controlled grounded resistor. *Radioengineering*, 2010, vol. 19, no. 3, p. 455 to 459.

[11] MAHMOUD, S. A. A low voltage CMOS floating resistor. In *ICEEC'04, International Conference on Electrical, Electronic and Computer Engineering*, 2004, p. 453–456.

[12] GUPTA, M., PANDEY, R. FGMOS based voltage-controlled resistor and its applications. *Microelectronics Journal*, 2010, vol. 41, no. 6, p. 25–32.

[13] ZOUAOUI-ABOUDA, H., FABRE, A. New high-value floating controlled resistor in CMOS technology. *IEEE Transactions on Instrumentation and Measurement*, 2006, vol. 55, no. 3, p. 1017 to 1020.

[14] RIEWRUJA, V., PETCHMANEELUMKA, W. Floating current controlled resistance converters using OTAs. *International Journal of Electronics and Communications*, 2008, vol. 62, p. 725–731.

[15] SAKURAI, S., ISMAIL, M. A CMOS square-law programmable floating resistor independent on the threshold voltage. *IEEE Transact. on Circuits and Systems II*, 1992, vol. 39, p. 565 to 574.

[16] ELWAN, H. O., MAHMOUD, S. A., SOLIMAN, A. M. CMOS voltage controlled floating resistor. *International Journal of Electronics*, 1996, vol. 81, no. 5, p. 571 – 576.

[17] WANG, S., CHAWLA, V., HA, D. S., KIM, B. Low-voltage low-power 1.6 GHz quadrature signal generation through stacking a transformer-based VCO and a divide-by-two. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2012, vol. 59, no. 12, p. 2901-2910.

[18] VALERO BERNAL, M. R., CELMA, S., MEDRANO, N., CALVO, B. An ultralow-power low-voltage class-AB fully

differential opamp for long-life autonomous portable equipment. *IEEE Transactions on Circuits and Systems II: Express Briefs,* 2012, vol. 59, no. 10, p. 643 - 647.

[19] PAPANANOS, Y. E. *Radio-Frequency Microelectronic Circuits for Telecommunication Applications.* London, (UK): Kluwer Academic Publishers, 1999.

[20] LAHIRI, A. New CMOS-based resistorless current-mode first-order all-pass filter using only ten transistors and one external capacitor. *Radioengineering*, 2011, vol. 20, no. 3, p. 638 – 643.

[21] MINAEI, S., YÜCE, E., ÇIÇEKOĞLU, O. ICCII based voltage-mode filter with single input and six outputs employing grounded capacitors. *Circuits Systems and Signal Processing*, 2006, vol. 25, no. 4, p. 559 – 566.

[22] MAHMOUD, S. A., SOLIMAN, A. M. CMOS balanced output transconductor and applications for analog VLSI. *Microelectronics Journal*, 1999, vol. 30, no.1, p. 29 – 39.

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