Voltage-Mode Multifunction Biquadratic Filters Using New Ultra-Low-Power Differential Difference Current Conveyors

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Abstract. *This paper presents two low-power voltage-mode multifunction biquadratic filters using differential difference current conveyors. Each proposed circuit employs three differential difference current conveyors, two grounded capacitors and two grounded resistors. The low-voltage ultra-low-power differential difference current conveyor is used to provide low-power consumption of the proposed filters. By appropriately connecting the input and output terminals, the proposed filters can provide low-pass, band-pass, high-pass, band-stop and all-pass voltage responses at high-input terminals, which is a desirable feature for voltage-mode operations. The natural frequency and the quality factor can be orthogonally set by adjusting the circuit components. For realizing all the filter responses, no inverting-type input signal requirements as well as no component-matching conditional requirements are imposed. The incremental parameter sensitivities are also low. The characteristics of the proposed circuits are simulated by using PSPICE simulators to confirm the presented theory.*

Keywords

Biquadratic filter, voltage-mode circuit, low-power circuit, differential difference current conveyor.

1. Introduction

At present, there is growing interest in designing of low-voltage (LV) supply and consuming low-power (LP) analog signal processing [1]-[5]. This is due to the demand that portable equipments, biomedical devices, embedded sensor interfaces are increasingly needed. Several LV LP active elements have been reported in the technical literature [6]-[15]. These active elements can be used to design LP consumption analog signal processing circuits. For this paper, floating-gate (FG) active element in [12] is interesting, because this device has the features of low power supply (±0.5 V), ultra-low-power consumption (10 μW) and rail-to-rail input voltage swing. Therefore, LP analog signal processing applications can be achieved by using this device as active element.

Active filters are ones of analog signal processing that can apply in telecommunication, electronic and control systems. They can be widely used in the implementation of phase-locked loop (PLL) frequency modulation (FM) stereo demodulation, touch-tone telephone tone decode, cross-over network used in a three-way high-fidelity loudspeaker [16]-[18]. In addition, LV and LP active filters can also be used in biomedical systems [19]-[23] and wireless systems [24], [25]. Besides, voltage-mode active filters with high-input impedance are great of interest because several cells of this kind can be directly connected in cascade to implement higher order filters [26]. Also, the circuits are attractive for monolithic integrated circuit (IC) implementation, if it employs grounded capacitors [27]. Over the past few decades, many voltage-mode universal biquadratic filters based on different design techniques have been developed in the literature, see, for example [28]-[35]. It is well-known that the main problem of the voltage-mode filters is the arithmetic operation (addition and subtraction) of voltage signals. Therefore, voltage-mode universal filters in [28]-[35] suffer from one or more of the following disadvantages: (a) they cannot provide high-input impedance for realizing five standard filter responses [28]-[30], [34], (b) for realizing five standard filter responses, they require the component-matching condition [28]-[30], [32]-[34], (c) they use an excessive number of active or passive components [32], [33], [35], (d) they use floating capacitors or floating resistors in the circuit design [28]-[31], (e) they require inverting-type input signals for realizing some filtering functions, i.e. all-pass filter response [31], [34]. Recently, Chiu et al. [36] proposed a new current conveyor circuit so-called differential difference current conveyor (DDCC). The DDCC has the advantages of both the CCII and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability) [36]. Thus, the arithmetic operation of voltage signals can easily be achieved by using DDCC as active elements. Many voltage-mode filters using DDCC as active building block have been reported in technical literature [37]-[56]. Nevertheless, some of these filters still suffer from one or more of the following weaknesses: (i) cannot provide all the five standard biquadratic filtering functions, namely, low-pass (LP), band-pass (BP), high-pass (HP), band-stop (BS), all-pass (AP) responses from the same configuration [38], [39], [40], [45], [52], (ii) use of floating passive elements (capacitor and/or resistor) which is not desirable for integrated circuit (IC) implementation [37], [39], [42], [44], [47], [49], [50], [51], [52], [53], (iii) cannot offer high-input impedance, which is not desirable for cascading in voltage-mode operation [42], [44], [47], [49], (iv) need of component-matching conditions for realizing all the five standard biquadratic filtering functions [39], [47], [49], [51], [52], (v) use two kinds of active elements [44], [48], (vi) provide only a first-order all-pass filtering function [54]-[56].

Therefore, two new high-input impedance voltage-mode multifunction biquadratic filters with four inputs and two/three outputs using three DDCCs and all grounded passive components are presented. The proposed circuits employ ultra-low-power active building block by Khateb et al. [12] as active building block, hence micro-power filter can be obtained, which is suitable for biological signal processing applications. The use of all grounded passive elements makes the circuits highly suitable for IC implementation. By appropriately connecting the input and output terminals, the circuit can realize all the five standard biquadratic filtering functions. For realizing these filtering responses, no component-matching conditions and no inverting-type input signals are required. The circuit also offers high-input impedance, which is desirable for cascading in voltage-mode operation. Low active and low passive sensitivities are possessed. The parameters ω_0 and Q can be set orthogonally by adjusting the circuit components. The comparison between the proposed circuits and some previously DDCC-based filters is summarized in Tab. 1.

2. Proposed Circuits

Fig. 1 shows the electrical symbol of DDCC. It was proposed in 1996 by Chiu et al. [36]. This device, the addition and subtraction operations can be obtained by appropriately applying the voltages at terminals y_1, y_2 and y_3. This property makes it different from conventional current conveyors.

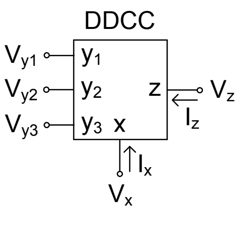

Fig. 1. Electrical symbol of DDCC.

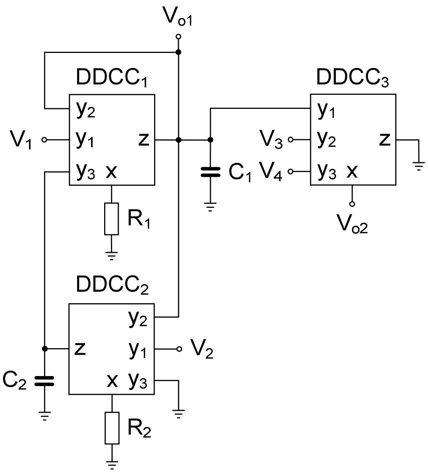

Fig. 2. First proposed multifunction filter.

The DDCC enjoys the advantages of CCII and DDA such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, low power consumption and high-input impedance. The characteristics of the DDCC is described as

$$\begin{pmatrix} V_x \\ I_{y1} \\ I_{y2} \\ I_{y3} \\ I_z \end{pmatrix} = \begin{pmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} V_{y1} \\ V_{y2} \\ V_{y3} \\ I_x \end{pmatrix}. \tag{1}$$

The DDCC has three voltage input terminals: y_1, y_2 and y_3, which possesses high-input impedance. Terminal x is a low-impedance current output terminal. Thus, if the realization is connected the input signal at y terminal and the output signal at x terminal, it will be possessed high-input and low-output impedance, which is a desirable feature for voltage-mode circuits.

The first proposed multifunction biquadratic filter employing three DDCCs, two grounded capacitors and two grounded resistors is shown in Fig. 2. Using equation (1), the output signals V_{o1} and V_{o2} of Fig. 2 can be obtained as

$$V_{o1} = \frac{s\left(\frac{1}{R_1 C_1}\right)V_1 + \left(\frac{1}{R_1 R_2 C_1 C_2}\right)V_2}{D(s)}, \tag{2}$$

$$V_{o2} = \frac{s\left(\frac{1}{R_1 C_1}\right)V_1 + \left(\frac{1}{R_1 R_2 C_1 C_2}\right)V_2 - D(s)V_3 + V_4}{D(s)} \tag{3}$$

where $D(s) = s^2 + s\frac{1}{R_1 C_1} + \frac{1}{R_1 R_2 C_1 C_2}$.

It is clearly seen from (2) and (3) that:

- The non-inverting LP response can be obtained when $V_2 = V_{in}$, $V_1 = V_3 = V_4 = 0$ (grounded) and V_{o1} or $V_{o2} = V_{out}$.

Circuits	Number of active elements	Number of resistor (R) & capacitor (C)	Offer five standard filters	All-grounded passive elements	Offer high-input & low-impedance	No need matching-condition	Only a kind of active element
Proposed filters	3 DDCCs	2-R & 2-C	Yes	Yes	Yes & Yes	Yes	Yes
Ref. [37] in 2003	2 DDCCs	2-R & 2-C	Yes	No	No & No	Yes	Yes
Ref. [38] in 2004	2 DDCCs	2-R & 2-C	No	Yes	Yes & No	Yes	Yes
Ref. [39] in 2005 (Fig.5)	1 DDCC	2-R & 2-C	No	No	Yes & No	No	Yes
Ref. [40] in 2007 (Fig.1)	2 DDCCs	2-R & 2-C	No	Yes	Yes	Yes	Yes
Ref. [41] in 2007	1 DDCC	3-R & 2-C	No	No	No & No	No	Yes
Ref. [42] in 2007	2 DDCCs	3-R & 2-C	Yes	No	No & No	No	Yes
Ref. [43] in 2007	3 DDCCs	2-R & 2-C	Yes	Yes	Yes & Yes	Yes	Yes
Ref. [44] in 2008	1 DDCC, 2 OTAs	2-C	Yes	No	No & No	Yes	No
Ref. [45] in 2008	1 DDCC, 2 OTAs	2-C	No	Yes	Yes & No	Yes	No
Ref. [46] in 2008	3 DDCCs	2-R & 2-C	Yes	Yes	Yes & No	Yes	Yes
Ref. [47] in 2009	2 DDCCs	3-R & 2-C	Yes	No	No	No	Yes
Ref. [48] in 2010	1 DDCC, 1 FDCCII	2-R & 2-C	Yes	Yes	Yes & No	Yes	No
Ref. [49] in 2011	3 DDCCs	3-R & 2-C	Yes	No	No & No	No	Yes
Ref. [50] in 2011	3 DDCCs	2-R & 2-C	Yes	No	Yes & No	Yes	Yes
Ref. [51] in 2012 (Fig.2)	3 DDCCs	4-R & 2-C	Yes	Yes	Yes & No	No	Yes
Ref. [52] in 2012	1 DDCC	3-R & 2-C	No	No	No & No	No	Yes
Ref. [53] in 2012	3 DDCCs	3-R & 2-C	Yes	No	Yes & No	Yes	Yes

Tab. 1. Comparison of proposed filters with those of previous circuits.

- The non-inverting BP response can be obtained when $V_1=V_{in}$, $V_2=V_3=V_4=0$ (grounded) and V_{o1} or $V_{o2}=V_{out}$.
- The inverting HP response can be obtained when $V_1=V_2=V_3=V_{in}$, $V_4=0$ (grounded) and $V_{o2}=V_{out}$.
- The inverting BS response can be obtained when $V_1=V_3=V_{in}$, $V_2=V_4=0$ (grounded) and $V_{o2}=V_{out}$.
- The inverting AP response can be obtained when $V_1=V_3=V_{in}$, $V_3=0$ (grounded), V_4 and V_{o1} are connected, and $V_{o2}=V_{out}$.

Thus, the proposed filter can realize all the standard types of the biquadratic filtering function without component-matching condition requirements as well as without inverting-type voltage input signals requirements. Since all the passive components are grounded, thus the circuit is beneficial to an IC implementation [27]. It should be noted that the input signals V_3 and V_4 of the proposed filter are applied to the y_2 and y_3 terminals, respectively, of the $DDCC_3$ while the input signals V_1 and V_2 of the proposed filter are applied to the y_1 terminal of the $DDCC_1$ and $DDCC_2$, respectively. Thus, the circuit enjoys of high-input impedance, which is suitable for cascading in voltage-mode operation. Moreover, the output signal V_{o2} of the proposed filter is connected to the x terminal of the $DDCC_3$. Then, the output voltage V_{o2} has the feature of low-output impedance, which makes the output voltage V_{o2} easily connected to the next stage without any buffer. The parameters ω_o and Q of Fig. 2 can be given by

$$\omega_o=\frac{1}{\sqrt{R_1R_2C_1C_2}}, \quad (4)$$

$$Q=\sqrt{\frac{R_1C_1}{R_2C_2}}. \quad (5)$$

Letting $R_1=R_2=R$, the circuit parameters can be simply rewritten as

$$\omega_o=\frac{1}{R\sqrt{C_1C_2}}, \quad (6)$$

$$Q=\sqrt{\frac{C_1}{C_2}}. \quad (7)$$

From (6) and (7) the parameter Q can be set by C_1 and C_2 and parameter ω_o can be set by resistor R without disturbing Q. Thus, the biquadratic filter has also orthogonal tuning capability for the circuit parameters Q and ω_o. Note from the proposed filter in Fig. 2 that it requires no component-matching condition for realizing all filter responses. In fact, for the case of $R_1=R_2$, the component-matching condition is imposed. This problem can be solved by using two JFETs or two MOSFETs to replace R_1 and R_2 with its gate connected by the same voltage control [57], [58]. Then, the tracking problems inherent dual-element controlled can be avoided. Also, a voltage-controlled universal filter can be obtained.

By slightly modifying the proposed circuit in Fig. 2, the second proposed filter is shown in Fig. 3. The voltage across the capacitor C_2 (V_{o2}) is additional output signal. $DDCC_3$ is used for summing and subtracting the voltage signals from any terminals. Thus, this configuration can be confirmed that the addition and subtraction voltage can easily be achieved by using DDCC as active elements. It should be noted that the filter in Fig. 3 is employed equally active and passive elements with Fig. 2. Using (1), the output signals V_{o1}, V_{o2} and V_{o3} of the second proposed circuit can be obtained as

$$V_{o1} = \frac{s\left(\frac{1}{R_1C_1}\right)V_1 + \left(\frac{1}{R_1R_2C_1C_2}\right)V_2}{D(s)}, \tag{8}$$

$$V_{o2} = \frac{\left(s\frac{1}{R_2C_2} + \frac{1}{R_1R_2C_1C_2}\right)V_2 - \left(\frac{1}{R_1R_2C_1C_2}\right)V_1}{D(s)}, \tag{9}$$

$$V_{o3} = \frac{V_3 - D(s)V_1 + V_4}{D(s)} \tag{10}$$

where $D(s) = s^2 + s\frac{1}{R_1C_1} + \frac{1}{R_1R_2C_1C_2}$.

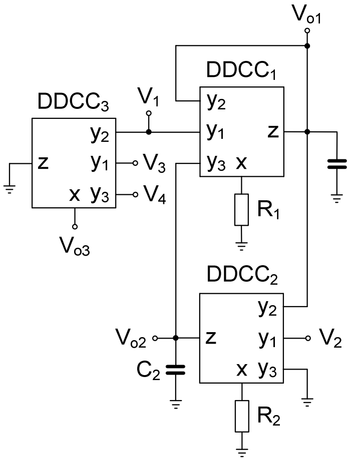

Fig. 3. Second proposed multifunction filter.

It is clearly seen from (8) to (10) that:

- The non-inverting LP response can be obtained when $V_2 = V_{in}$, $V_1 = V_3 = V_4 = 0$ (grounded) and $V_{o1} = V_{out}$.
- The inverting LP response can be obtained when $V_1 = V_{in}$, $V_2 = V_3 = V_4 = 0$ (grounded), and $V_{o2} = V_{out}$.
- The non-inverting BP response can be obtained when $V_1 = V_{in}$, $V_2 = V_3 = V_4 = 0$ (grounded), and $V_{o1} = V_{out}$.
- The inverting HP response can be obtained when $V_1 = V_2 = V_{in}$, $V_4 = 0$ (grounded), $V_3 = V_{o1}$ (connected) and $V_{o3} = V_{out}$.
- The inverting BS response can be obtained when $V_1 = V_{in}$, $V_2 = V_4 = 0$ (grounded), $V_3 = V_{o1}$ (connected) and $V_{o3} = V_{out}$.
- The inverting AP response can be obtained when $V_2 = 0$ (grounded), $V_1 = V_{in}$, $V_3 = V_4 = V_{o1}$ (connected) and $V_{o3} = V_{out}$.

Thus, the second proposed filter can realize all the standard types of the biquadratic filtering functions, i.e. LP, BP, HP, BS and AP filters. For realizing these filtering functions, it requires no component-matching condition requirements as well as no inverting-type voltage input signal requirements. In addition, the four input signals V_1, V_2, V_3 and V_4, are connected to the high-input impedance level of the DDCCs (y terminals). Then, the second proposed circuit enjoys the advantage of having high-input impedance. Also, the output voltage V_{o3} has the feature of low-output impedance. The parameters ω_o and Q of Fig. 3 are expressed by

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}}, \tag{11}$$

$$Q = \sqrt{\frac{R_1C_1}{R_2C_2}}. \tag{12}$$

From (11) and (12), if letting $R_1 = R_2 = R$, the parameter Q can be given by $(C_1/C_2)^{1/2}$ and parameter ω_o can be set by resistor R without disturbing Q. Thus, the second biquadratic filter has orthogonal tuning capability for the circuit parameters Q and ω_o.

3. Non-ideal Effects

The ideal circuit performance so far has been based on the assumptions that the DDCC has no tracking errors and parasitic parameters. Thus, tracking errors and parasitic parameters of DDCC will be considered in this section. To consider the non-ideal effect of a DDCC, taking the non-idealities of the DDCCs into account, the relationship of the terminal voltages and currents can be rewritten as:

$$\begin{pmatrix} V_x \\ I_{y1} \\ I_{y2} \\ I_{y3} \\ I_z \end{pmatrix} = \begin{pmatrix} \alpha_{k1} & -\alpha_{k2} & \alpha_{k3} & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \beta_k \end{pmatrix} \begin{pmatrix} V_{y1} \\ V_{y2} \\ V_{y3} \\ I_x \end{pmatrix} \tag{13}$$

where $\alpha_{k1} = 1 - \varepsilon_{k1v}$ and ε_{k1v} ($|\varepsilon_{k1v}| << 1$) denotes the voltage tracking error from V_{y1} terminal to V_x terminal of the k-th DDCC, $\alpha_{k2} = 1 - \varepsilon_{k2v}$ and ε_{k2v} ($|\varepsilon_{k2v}| << 1$) denotes the voltage tracking error from V_{y2} terminal to V_x terminal of the k-th DDCC, $\alpha_{k3} = 1 - \varepsilon_{k3v}$ and ε_{k3v} ($|\varepsilon_{k3v}| << 1$) denotes the voltage tracking error from V_{y3} terminal to V_x terminal of the k-th DDCC and $\beta_k = 1 - \varepsilon_i$ and ε_i ($\varepsilon_i << 1$) denotes the output current tracking error of the k-th DDCC. Re-analyzing the proposed configuration of Figs. 2 and 3 with equation (13), the modified parameters ω_{on1} and Q_{n2} are obtained by

$$\omega_{on1} = \sqrt{\frac{\alpha_{13}\alpha_{22}\beta_1\beta_2}{R_1R_2C_1C_2}}, \tag{14}$$

$$Q_{n1} = \frac{1}{\alpha_{12}}\sqrt{\frac{R_1C_1}{R_2C_2}\frac{\alpha_{13}\alpha_{22}\beta_2}{\beta_1}}. \tag{15}$$

From (14) and (15), the tracking errors slightly change the parameters ω_o and Q.

The incremental sensitivities of the parameters ω_{on1} and Q_{n1} are calculated as in Tab. 2. From this table, all the active and passive sensitivities are equal or less than unity in magnitude.

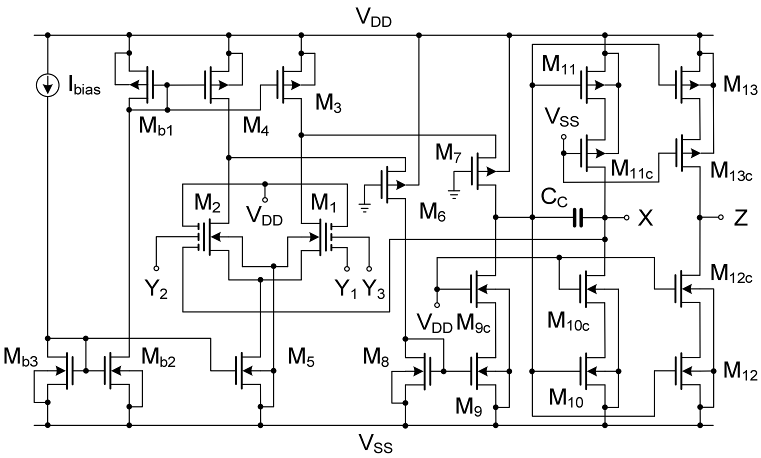

Fig. 4. CMOS realization of the DDCC [12].

X	$S_x^{\omega_{on1}}$	$S_x^{Q_{n1}}$
R_1	-0.5	0.5
R_2	-0.5	-0.5
C_1	-0.5	0.5
C_2	-0.5	-0.5
β_1	0.5	-0.5
β_2	0.5	0.5
α_{12}	0.0	-1.0
α_{13}	0.5	-0.5
α_{22}	0.5	0.5

Tab. 2. Sensitivities of circuit components.

In case of the filter operating at high frequency the parasitic impedances of the DDCCs should be considered. The most significant parasitic impedances in the filter are the parasitic intrinsic resistances of the x terminals and the parasitic capacitances of the y and z. The modified parameters ω_{on2} and Q_{n2} for the case of the filter operating at high frequency can be obtained as

$$\omega_{on} = \frac{1}{\sqrt{R_1' R_2' C_1' C_2'}}, \tag{16}$$

$$Q_n = \sqrt{\frac{R_1' C_1'}{R_2' C_2'}} \tag{17}$$

where $R'_1 = R_1 + R_{x1}$, $R_2' = R_2 + R_{x2}$, $C_1' = C_1 + C_{z1} + C_{y12} + C_{y22}$, $C_2' = C_1 + C_{z2} + C_{y23}$, R_{x1} and R_{x2} are the terminal x parasitic resistances of DDCC$_1$ and DDCC$_2$, respectively, C_{y12} and C_{y22} are the terminal y_2 parasitic capacitances of DDCC$_1$ and DDCC$_2$, respectively, C_{z1} and C_{z2} are the terminal z parasitic capacitances of DDCC$_1$ and DDCC$_2$, respectively, C_{y13} is the terminal y_3 parasitic capacitances of DDCC$_1$. From (16) and (17) it is evident that the influence of the parasitic resistances and capacitances affect mainly ω_o whereas this influence can be neglected for Q. To eliminate the influence of the parasitic impedances on ω_o the parasitic intrinsic resistances of x terminals must be taken in account during the selection of the values of R_1 and R_2. Also, the values of C_1 and C_2 should be chosen much higher than the values of the parasitic capacitance of y and z terminals. All the above mentioned requirements were respected and the deviation of ω_o and Q values can be neglected.

4. Simulation Results

The proposed circuits are verified by using PSPICE simulation with the 0.18 μm CMOS technology. The DDCC is realized by the CMOS implementation of Fig. 2 in Khateb et al. [12] by un-grounding a floating gate M_1 and treating this as the third y-input y_3. The revised version is shown in Fig. 4. The transistor aspect ratios are shown as Tab. 3. Other component values are $C_C = 0.4$ pF, $I_{bias} = 0.5$ μA, $V_{DD} = 0.5$ V and $V_{SS} = -0.5$ V. To verify the theoretical prediction of the proposed circuits, only Fig. 2 has been simulated using PSPICE simulation program, because of two proposed circuits are same the basis. As an example design, the capacitors $C_1 = C_2 = 10$ nF and the resistors $R_1 = R_2 = 15.9$ kΩ are given. This setting has been designed to obtain the LP, BP, HP, BS and AP filter responses with $f_o = 1$ kHz and $Q = 1$.

FG-DDCC	W/L (μm/μm)
M_1, M_2	1/0.5
M_3, M_4	12/1
M_5, M_{b1}	6/1
M_{9c}	2/1
M_{10c}, M_{12c}	3/0.5
M_{11c}, M_{13c}	4/0.5
M_6, M_7	25/1
M_8, M_9	2/1
M_{10}, M_{12}	15/3
M_{11}, M_{13}	20/3
M_{b2}, M_{b3}	2/1

Tab. 3. Transistors aspect ratios and component values Fig. 4 [12].

The simulated results for the LP, BP, HP, and BS filter characteristics are shown in Fig. 5. Fig. 6 shows the simulated frequency responses of the gain and phase characteristics of the AP filter. Therefore, it can be observed from Figs. 5 and 6 that the proposed filter performs five standard biquadratic filtering functions well. For these results, the power consumption of only 29.7 μW is obtained.

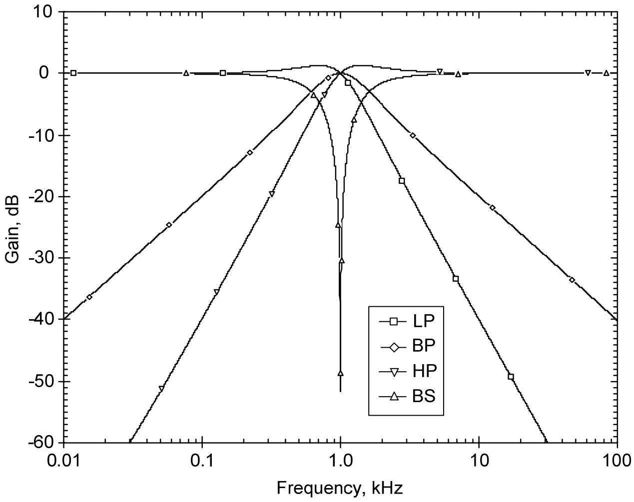

Fig. 5. Simulated LP, BP, HP and BS responses.

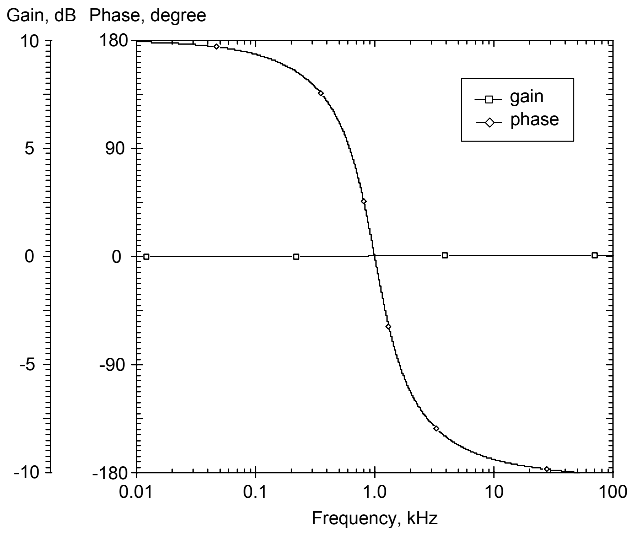

Fig. 6. Simulated gain and phase responses of AP filter.

In order to test the input dynamic range of the proposed filter, the simulation has been repeated for a sinusoidal input signal at $f_o \cong 1$ kHz. Fig. 7 shows that the input dynamic range of the BP response with $R_1 = R_2 = 15.9$ kΩ and $C_1 = C_2 = 10$ nF, which extends up to amplitude of 240 mV (peak) without signification distortion. The THD about 0.99 % is informed in this figure. The dependence of the output harmonic distortion of BP filter on input voltage amplitude is summarized in Fig. 8. One can obtain from Fig. 8 that the THD is about 1.66 % when the input signal is increased to 260 mV (peak). Fig. 9 shows the simulated input and output noise amplitude responses for BP filters with INOISE and ONOISE. The simulated equivalent input noise and total output noise are 23.03 μV/√Hz and 0.22 μV/√Hz for the frequency between 10 Hz to 100 kHz.

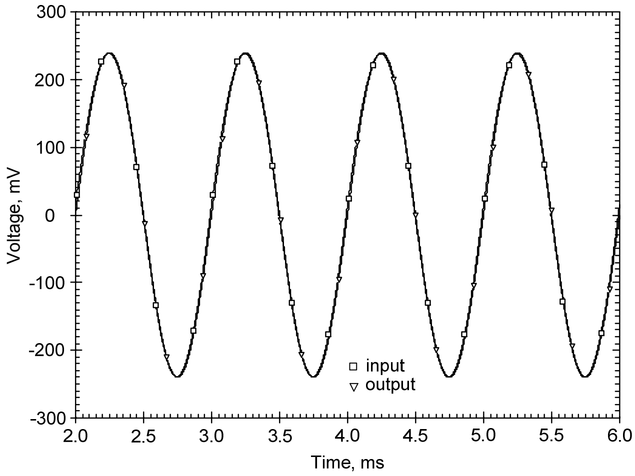

Fig. 7. The input and output waveforms of the BP response for a 1 kHz sinusoidal input voltage of 240 mV (peak).

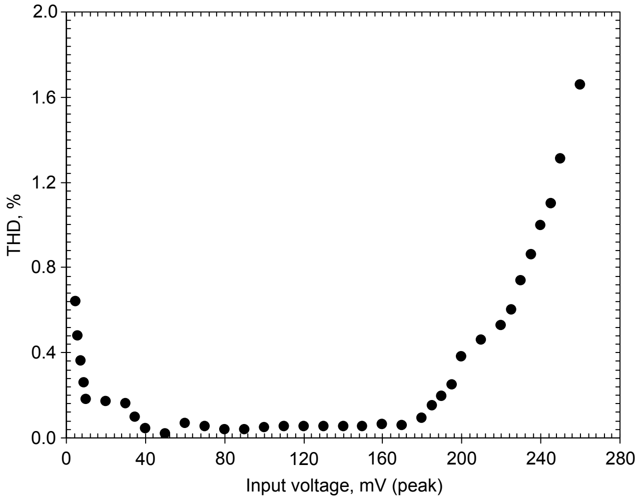

Fig. 8. Dependence of the output harmonic distortion of BP filter on input voltage amplitude.

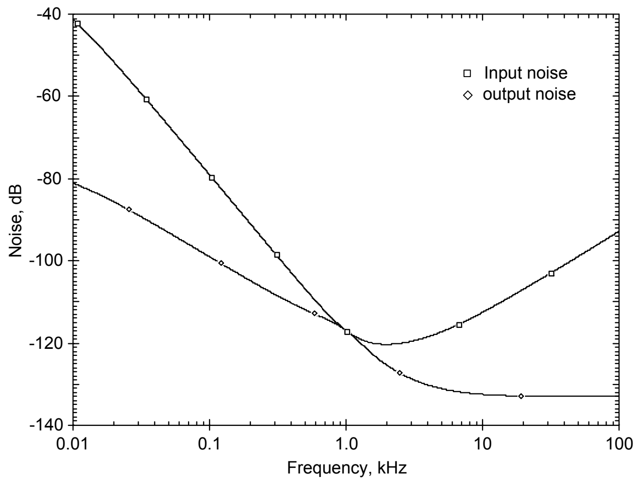

Fig. 9. The equivalence input and output noise against frequency.

Fig. 10 shows the simulated a BP filter response of the proposed filter in Fig. 2 using parameter as,

$C_1 = C_2 = 10$ nF and $R = 53$ kΩ, 15.9 kΩ and 5.3 kΩ (i.e. $R = R_1 = R_2$). From this figure, when the resistors are 53 kΩ, 15.9 kΩ and 5.3 kΩ, the natural frequencies are obtained as 0.301 kHz, 0.998 kHz and 2.988 kHz, respectively, while the theoretical value should be 0.302 kHz,

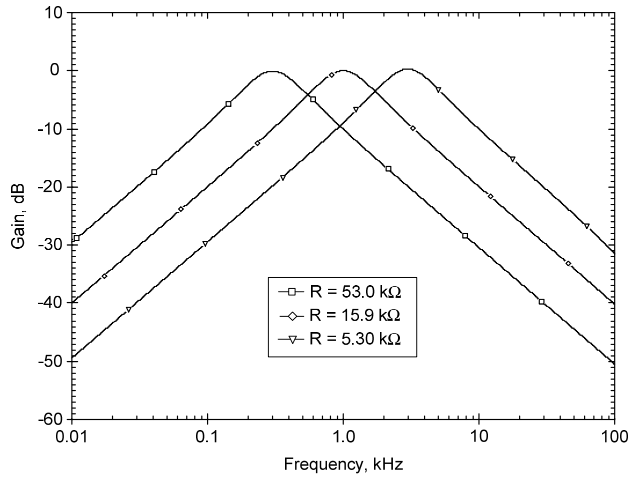

Fig. 10. Simulated BP responses when resistors are varied.

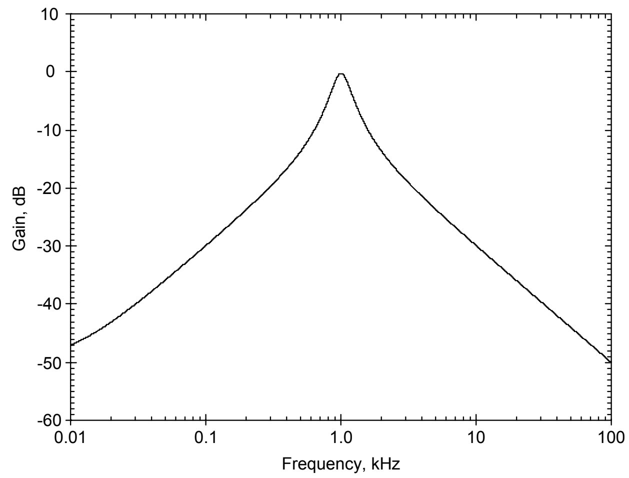

Fig. 11. Simulated BP response when $C_1 = 10$ nF, $C_2 = 1$ nF, $R_1 = R_2 = 50.32$ kΩ ($Q = 3.16$) are given.

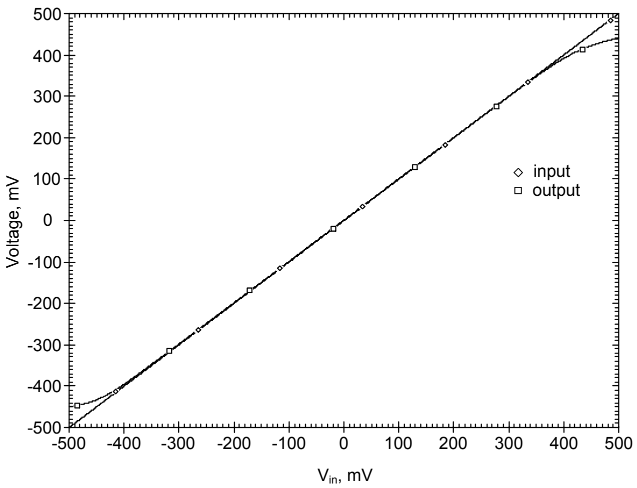

Fig. 12. DC analysis with input voltage of the proposed filter swept from -500 mV to +500 mV.

1 kHz and 3 kHz, respectively. This result is confirmed by (6). Fig. 11 shows the simulated frequency response of BP filters with $R_1 = R_2 = 50.32$ kΩ, $C_1 = 10$ nF and $C_2 = 1$ nF, resulting to a natural frequency $f_o \cong 1$ kHz and $Q \cong 3.16$. This simulation result is confirmed by (7). However, setting of factor Q by the ratio of capacitors maybe difficult in the practice, electronic controlling of factor Q via the bias current or the bias voltage is easier [59]-[61]. Fig. 12 shows the DC V_{out} versus V_{in} characteristic that clearly expresses the limits of linear operation of the filter, which can be approximately described as ±400 mV. A DC offset is also evident from this figure.

5. Conclusions

In this paper, new micropower voltage-mode universal biquadratic filters are presented. The proposed filters are suitable mainly for battery-powered implantable and wearable medical devices and as recognized fact these devices process biological signals and their characteristics are low amplitudes and low frequencies, i.e. they vary from a fraction of a hertz to several kilohertz with amplitude in range of micro up to millivolts. The proposed circuits use three plus-type DDCCs, two grounded capacitors and two grounded resistors. The use of only grounded capacitors and grounded resistors makes the proposed circuits suitable for IC implementation. The proposed circuits can realize LP, BP, HP, BS and AP filter responses by appropriately connecting the input and output terminals. For realizing these filtering functions, no component-matching condition requirements and no inverting-type input signal requirements are needed. The proposed circuits also offer high-input impedance terminal, which allows easy cascading in voltage-mode operation. Low active and passive sensitivities of the circuits are possessed. An orthogonal control between parameters ω_0 and Q can be set by the circuit components.

Acknowledgements

This work was supported by King Mongkut's Institute of Technology Ladkrabang (KMITL) (KMITL Research Fund to M. Kumngern, P. Phasukkit, S. Tungjitkusolmun) and by the SIX project; the registration number CZ.1.05/2.1.00/03.0072, the operational program Research and Development for Innovation and has been supported by the Czech Science Foundation as project No. GA102/11/1379.

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