A Tunable Butterworth Low-Pass Filter with Digitally Controlled DDCC

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Abstract. *This paper presents a 6th-order tunable Butterworth low-pass active filter with Digitally Controlled Differential Difference Current Conveyor (DDCC). This active filter is synthesized using the systematic method of voltage-mode linear transformation (VMLT) which enables the filter to use fewer active components, grounded capacitors and grounded resistors to avoid the parasitical effects. The bandwidth of the filter can be tuned by digital switches to adjust the output current of the DDCC. The specifications of the filter are based on 3G standard, and the filter is controlled by 8-bit digital signals. The tunable bandwidth of the filter is from 12 kHz to 2.6 MHz. The filter chip layout is realized by TSMC 0.18 μm CMOS 1P6M mixed-mode technology. The supply voltage is 1.8 V and the power consumption is 3.6 mW.*

Keywords

Differential difference current conveyor (DDCC), voltage-mode linear transformation (VMLT), current division network (CDN), active filter.

1. Introduction

In recent years, CMOS circuits have become the main building blocks of VLSI circuits. In analog IC design, active filters have been used for communication and RF front-end processing such as channel selection filter [1], [2].

There are many methods to synthesize high-order active filters [3], [4], [5]: Follow-the-leader feedback, cascade synthesis, Bruton's transformation, active inductor approach, Leapfrog, Linear transformation, etc. Because the linear transformation method may be applied to prevent monolithic integrated filters from the effect of unpredictable variations of process parameters, it is applied in this study not only to simplify the design and to reduce the number of components but also to use grounded capacitors and resistors to avoid parasitical effects. The result is a simple but effective design of a high-order active filter.

Section II discusses the basic theory of Voltage-Mode Linear Transformation (VMLT), and digitally controlled differential difference current conveyor (DDCC). The design of an active filter and the implementation of the proposed filter are given in Section III. The simulation results are shown in Section IV, and the conclusions are given in Section V.

2. The VMLT and the Digitally Controlled DDCC

This section explains the concepts of the VMLT and the digitally controlled DDCC.

2.1 The VMLT

A conventional cascaded two-port network is shown in Fig. 1.

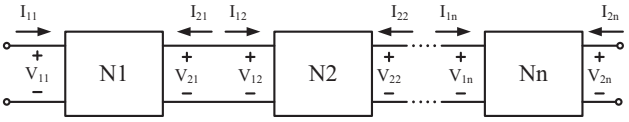

Fig.1. A conventional two-port network.

The variables of input and output are in the forms of voltage and current. The equation is shown in (1).

$$\begin{bmatrix} V_{1i} \\ I_{1i} \end{bmatrix} = T_i \begin{bmatrix} V_{2i} \\ I_{2i} \end{bmatrix} = \begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix} \begin{bmatrix} V_{2i} \\ I_{2i} \end{bmatrix} \tag{1}$$

where T_i is the transfer matrix.

The variables can be changed into voltage variables (x_{1i}, x_{2i}, y_{1i}, y_{2i}) through the VMLT method by the transfer matrices S_{1i} and S_{2i} as shown in (2) and (3).

$$\begin{bmatrix} x_{1i} \\ y_{1i} \end{bmatrix} = S_{1i} \begin{bmatrix} V_{1i} \\ I_{1i} \end{bmatrix} = \begin{bmatrix} \alpha_{1i} & \beta_{1i} \\ \gamma_{1i} & \delta_{1i} \end{bmatrix} \begin{bmatrix} V_{1i} \\ I_{1i} \end{bmatrix}, \tag{2}$$

$$\begin{bmatrix} x_{2i} \\ y_{2i} \end{bmatrix} = S_{2i} \begin{bmatrix} V_{2i} \\ I_{2i} \end{bmatrix} = \begin{bmatrix} \alpha_{2i} & \beta_{2i} \\ \gamma_{2i} & \delta_{2i} \end{bmatrix} \begin{bmatrix} V_{2i} \\ I_{2i} \end{bmatrix}. \tag{3}$$

x_{ji} and y_{ji} are voltage variables, α_{ji} and γ_{ji} are dimensionless, and the unit of β_{ji} and δ_{ji} is mho; j = 1, 2 and i = 1 ... n, where n is the order of the two-port network.

(4) can be derived from (1)~(3):

$$\begin{bmatrix} x_{1i} \\ y_{1i} \end{bmatrix} = S_{1i} T_i S_{2i}^{-1} \begin{bmatrix} x_{2i} \\ y_{2i} \end{bmatrix} = \frac{1}{\Delta_i} \begin{bmatrix} \alpha_{1i} & \beta_{1i} \\ \gamma_{1i} & \delta_{1i} \end{bmatrix} \begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix} \begin{bmatrix} \delta_{2i} & -\beta_{2i} \\ -\gamma_{2i} & \alpha_{2i} \end{bmatrix} \begin{bmatrix} x_{2i} \\ y_{2i} \end{bmatrix} = \begin{bmatrix} a_i & b_i \\ c_i & d_i \end{bmatrix} \begin{bmatrix} x_{2i} \\ y_{2i} \end{bmatrix}. \quad (4)$$

The y_{ji}'s can be represented by the x_{ji}'s. If the x_{ji}'s represent the inputs and the y_{ji}'s represent the outputs, a new cascaded two-port ladder prototype network can be developed. Equations (5) and (6) are introduced to simply the interconnection between the two-ports:

$$S_{12} \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} S_{21}, \quad (5)$$

$$\begin{bmatrix} x_{12} \\ y_{12} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} x_{21} \\ y_{21} \end{bmatrix}. \quad (6)$$

These equations can be called the cross-cascaded interconnection which means that the connection is cross-cascaded between every two of the new two-port networks as shown in Fig. 2.

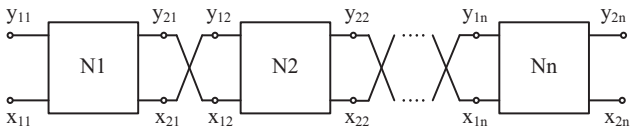

Fig. 2. The cross-cascaded two-port network after VMLT.

2.2 The Digitally Controlled DDCC

The symbol of the DDCC [6], [7], [8] is shown in Fig. 3. The DDCC is an active component that has four ports marked Y_1, Y_2, X and Z. The DDCC is an active component which is basically a second generation current conveyor combined with a differential difference amplifier. The small signal model of DDCC is shown in Fig. 4. There are two types of DDCC. The relationships among the variables are $I_{Y1} = I_{Y2} = 0$, $V_X = V_{Y1} - V_{Y2}$ and $I_Z = I_X$ for the positive type of DDCC as expressed by (7), or $I_{Y1} = I_{Y2} = 0$, $V_X = V_{Y1} - V_{Y2}$ and $I_Z = -I_X$ for the negative type of DDCC,

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ I_Z \end{bmatrix} \quad (7)$$

We use the DDCC configuration proposed in [9] and add four current-shunt transistors M1A, M2A, M3A and M4A at the input stage, as shown in Fig. 5. Such arrangement can improve the input common mode range as well as enhance the linearity of the DDCC. The component parameters of the proposed DDCC are listed in Tab. 1.

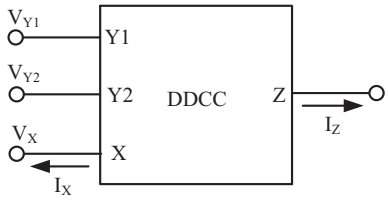

Fig. 3. Symbol of DDCC.

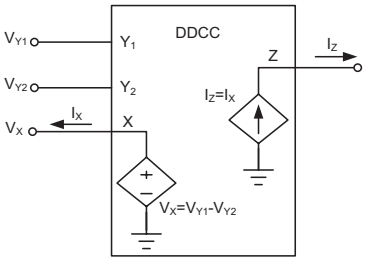

Fig. 4. Ideal model of DDCC.

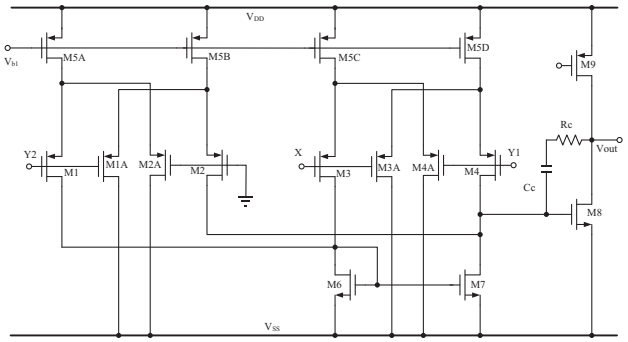

Fig. 5. The schematic of the DDCC.

Transistors (DDCC)	Sizes (W/L), μm
M5A, M5B, M5C, M5D	20/0.5
M1, M2, M3, M4	48/0.5
M1A, M2A, M3A, M4A	12/0.5
M6, M7	6/0.5
M8, M9	6.2/0.5, 30.4/0.5
Resistor and Capacitor	Value
Resistor (RC)	2 kΩ
Capacitor (CC)	0.25 pF

Tab. 1. The component parameters of the proposed DDCC.

Current division networks (CDNs) [10]-[14] are added in order to widen the range of the output current I_Z of the proposed DDCC. The CDNs can modify the current relationship from $I_Z = I_X$ to $I_Z = \alpha I_X$ for the positive type of DDCC and $I_Z = -\alpha I_X$ for the negative type of DDCC, where the digital control factor α is the digital value corresponding to the CDN binary switches with $0 < \alpha \leqq 1$. Thus a positive type digitally controlled DDCC can be represented by (8),

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & \alpha & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ I_Z \end{bmatrix}. \quad (8)$$

The block diagram of a 4-bit digitally controlled CDN is shown in Fig. 6 which consists of 4 current division cells (CDCs). According to the current division principle, each CDC has one input current I_{in} and three output currents I_{o1}, I_{o2} and I_{o3}. Their relationships are expressed as follows:

$$I_{o1\_i} = d_i \frac{I_{in\_i}}{2}, \quad (9)$$

$$I_{o2\_i} = \overline{d}_i \frac{I_{in\_i}}{2}, \quad (10)$$

$$I_{o3\_i} = \frac{I_{in\_i}}{2} \quad (11)$$

where d_i is the digital control bit of the i^{th} CDC. As also shown in Fig. 6, the two output currents I_{o1} and I_{o2} of the 4-bit CDN are given by

$$I_{o1} = I_{o3\_0} + \sum_{i=0}^{i=3} I_{o1\_i} = \frac{1}{2^4}(1 + \sum_{i=0}^{i=3} 2^i d_i) I_{in\_3}, \quad (12)$$

$$I_{o2} = \sum_{i=0}^{i=3} I_{o2\_i} = \frac{1}{2^4}(\sum_{i=0}^{i=3} 2^i \overline{d}_i) I_{in\_3} \quad (13)$$

and

$$\alpha = \frac{I_{o1}}{I_{in\_3}} = \frac{1}{2^4}(1 + \sum_{i=0}^{i=3} 2^i d_i) \cdot \quad (14)$$

Hence the current gain of the 4-bit CDN is controlled digitally.

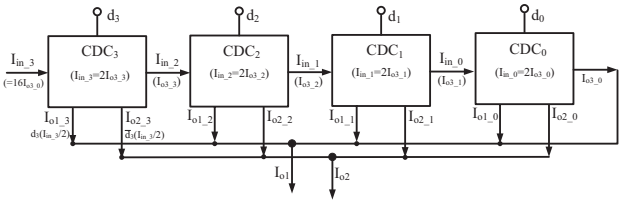

Fig. 6. The block diagram of a 4-bit digitally controlled CDN.

In this study, an 8-bit digitally controlled CDN is divided into two such 4-bit CDNs, each capable of mirroring and shunting the currents in the ratios 16:8:4:1, which are determined by the W/L sizes of the MOS transistors.

The schematic of the 8-bit digitally controlled CDN is shown in Fig. 7. The currents from the previous stage are mirrored by M13 and M18 which are controlled by the most significant (MSB) 4 bits and the least significant (LSB) 4 bits, respectively. As explained above, the currents are divided in the ratio 16:1 determined by the W/L sizes of M13 and M18, and each of M13 and M18 are connected to 8 MOS transistors with appropriate W/L sizes to shunt the current in the ratios 16:8:4:1. The two currents flow through M22 and M16 respectively and finally merge as the digitally controlled output current I_Z. The operations of the NMOS network are complementary to those of the PMOS network, and the two currents flow through M25 and M26 to merge as I_Z. The component parameters of the CDN are listed in Tab. 2.

Transistors (CDN)	Sizes (W/L)μm
M13a(b), M13c(d), M13e(f), M13g(h)	32/0.5, 16/0.5, 8/0.5, 4/0.5
M19a(b), M19c(d), M19e(f), M19g(h)	20.8/2, 10.4/2, 5.2/2, 2.6/2
M28a(b), M28c(d), M28e(f), M28g(h)	10.4/0.5, 5.2/0.5, 2.6/0.5, 1.3/0.5
M34a(b), M34c(d), M34e(f), M34g(h)	3.2/2.4, 1.6/2.4, 0.8/2.4, 0.4/2.4

Tab. 2. The component parameters of the CDN.

Finally, the DDCC and the CDN are combined to form a digitally controlled 8-bit DDCC. The symbol of the digitally controlled 8-bit DDCC is shown in Fig. 8, and the full schematic is shown in Fig.9. In next section, we will describe how VMLT is applied to the design of a high order filter by the digitally controlled DDCC circuit.

3. The Design of an Active Filter

To demonstrate the effectiveness and the flexibility of the proposed design, a 6th-order tunable Butterworth low-pass active filter using digitally controlled DDCCs is presented. The application of linear transformation and the realization of the filter using digitally controlled DDCCs are illustrated in this section.

The passive part of the filter is divided into three different portions: input portion, output portion, and middle portion. The middle portion is further divided into L series with $\alpha_{ji} = \delta_{ji} = 0$ and C shunt with $\beta_{ji} = \gamma_{ji} = 0$ to reduce the complexities of transformation matrices. Furthermore, we can choose either α_{ji} or $\gamma_{ji} = \pm 1$, and either β_{ji} or $\delta_{ji} = \pm R$ to reduce the number of the digitally controlled DDCCs.

Take the 6th-order Butterworth low-pass ladder filter shown in Fig. 10 for example. The transformation matrix of its input portion (the R-C shunt arm connected to the voltage source) can be expressed as

$$\begin{bmatrix} \alpha_{21} & \beta_{21} \\ \gamma_{21} & \delta_{21} \end{bmatrix} = \begin{bmatrix} 0 & \pm R \\ \pm 1 & 0 \end{bmatrix}. \quad (15)$$

Its output variables x_{21} and y_{21} can be expressed as

$$\pm y_{21} = \frac{\pm x_{21} + E}{sRC_1 + 1}. \quad (16)$$

The transfer functions can be derived for the digitally controlled DDCC circuits (DCDDCC-based circuits) and are also shown in Tab. 3 by

$$\pm y_{21} = \alpha \frac{\pm x_{21} + E}{1 + sR_aC_a} \cong \frac{\pm x_{21} + E}{1 + s\frac{R_aC_a}{\alpha}}. \quad (17)$$

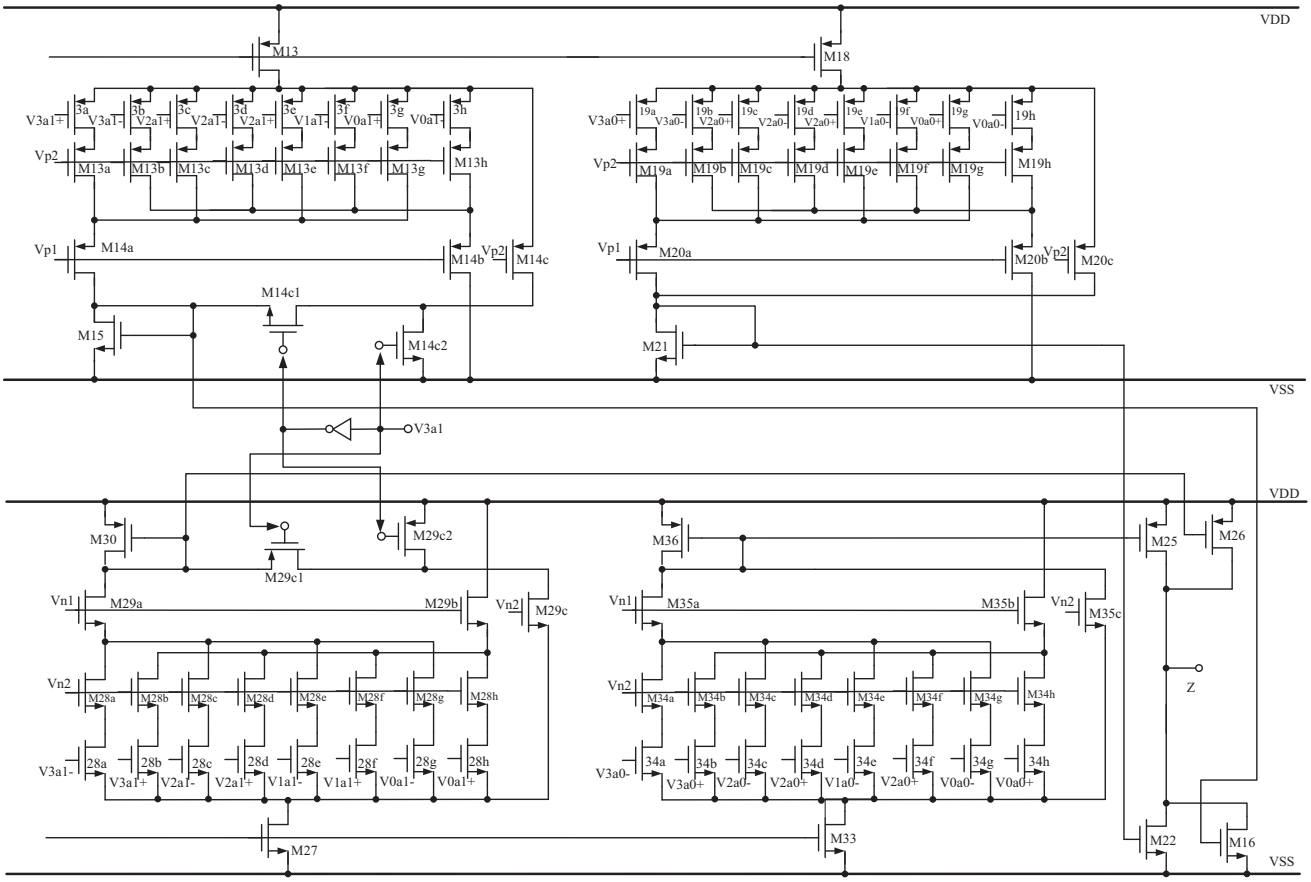

Fig. 7. The schematic of the 8-bit digitally controlled CDN.

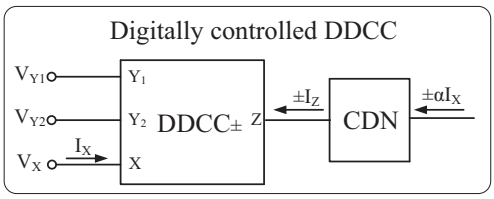

Fig. 8. The symbol of the digitally controlled 8-bit DDCC.

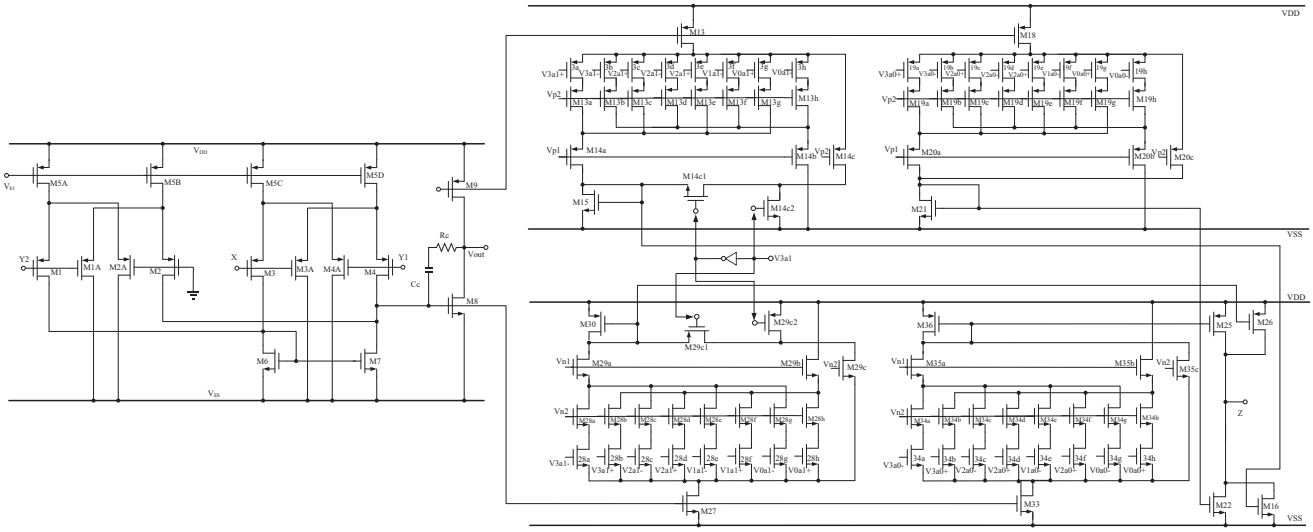

Fig. 9. The full schematic of the digitally controlled 8-bit DDCC.

The transformation matrix of the L series arm of the middle portion is

$$\begin{bmatrix}\alpha_{12} & \beta_{12}\\ \gamma_{12} & \delta_{12}\end{bmatrix}\begin{bmatrix}\alpha_{22} & \beta_{22}\\ \gamma_{22} & \delta_{22}\end{bmatrix}=\begin{bmatrix}\pm 1 & 0\\ 0 & \pm R\end{bmatrix}\begin{bmatrix}\pm 1 & 0\\ 0 & \pm R\end{bmatrix}. \quad (18)$$

It can be shown that

$$\pm y_{1i}=\pm y_{2i}=\frac{\mp x_{2i}\pm x_{1i}}{s\dfrac{L_2}{R}} \quad (19)$$

Its corresponding digitally controlled DDCC lossless integrator circuit can also be listed in Tab. 3 with its transfer function

$$\pm y_{1i}=\pm y_{2i}=\alpha\left(\frac{\mp x_{2i}\pm x_{1i}}{R_a}\cdot\frac{1}{sC_a}\right)=\frac{\mp x_{2i}\pm x_{1i}}{\dfrac{sR_aC_a}{\alpha}}. \quad (20)$$

The transformation matrix of the C shunt arm of the middle portion is

$$\begin{bmatrix}\alpha_{12} & \beta_{12}\\ \gamma_{12} & \delta_{12}\end{bmatrix}\begin{bmatrix}\alpha_{22} & \beta_{22}\\ \gamma_{22} & \delta_{22}\end{bmatrix}=\begin{bmatrix}0 & \pm R\\ \pm 1 & 0\end{bmatrix}\begin{bmatrix}0 & \pm R\\ \pm 1 & 0\end{bmatrix}. \quad (21)$$

It can be shown that

$$\pm y_{1i}=\pm y_{2i}=\frac{\mp x_{2i}\pm x_{1i}}{sRC_3}. \quad (22)$$

Its corresponding digitally controlled DDCC lossless integrator circuit can also be listed in Tab. 3 with its transfer function

$$\pm y_{1i}=\pm y_{2i}=\alpha\left(\frac{\mp x_{2i}\pm x_{1i}}{R_a}\cdot\frac{1}{sC_a}\right)=\frac{\mp x_{2i}\pm x_{1i}}{\dfrac{sR_aC_a}{\alpha}}. \quad (23)$$

The transformation matrix of the output portion (the R-L series arm) can be expressed as

$$\begin{bmatrix}\alpha_{12} & \beta_{12}\\ \gamma_{12} & \delta_{12}\end{bmatrix}=\begin{bmatrix}0 & \pm R\\ \pm 1 & 0\end{bmatrix}. \quad (24)$$

It can be shown that

$$\pm y_{16}=\frac{\pm x_{16}}{s\dfrac{L_6}{R}+1}=V_O. \quad (25)$$

Its corresponding digitally controlled DDCC lossless integrator circuit can be presented in Tab. 3 with its transfer function

$$\pm y_{16}=\alpha\left(\frac{\pm x_{16}}{R_a}\frac{R_a}{sC_aR_a+1}\right)\cong\frac{\pm x_{16}}{1+s\dfrac{C_aR_a}{\alpha}}=V_O. \quad (26)$$

In summary, we can divide the filter prototype into six sections and choose appropriate transformation matrices to obtain their x-y domain transfer functions.

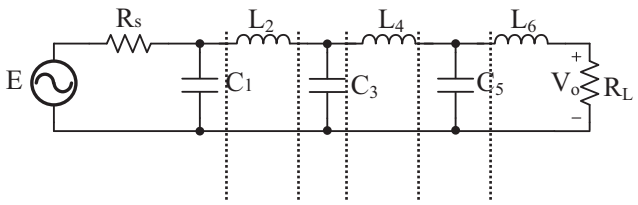

Fig. 10. The 6th-order Butterworth low-pass ladder filter.

Passive filter section circuit	Transformation matrix & transfer function	Digitally controlled DDCC-based circuit & design equation
R, C, E	$\begin{bmatrix}0 & \pm R\\ \pm 1 & 0\end{bmatrix}$ $\pm y_{21}=\frac{\pm x_{21}+E}{sRC+1}$	E, $\mp x_{21}$, Y1, Y2, X, Z, DCDDCC, Ra, Ca, $\pm y_{21}$, $R\cdot C=\frac{R_a\cdot C_a}{\alpha}$
L	$\begin{bmatrix}\pm 1 & 0\\ 0 & \pm R\end{bmatrix}\begin{bmatrix}\pm 1 & 0\\ 0 & \pm R\end{bmatrix}$ $\pm y_{1i}=\pm y_{2i}=\frac{\mp x_{2i}\pm x_{1i}}{s\frac{L}{R}}$	$\mp x_{2i}$, $\mp x_{1i}$, Y1, Y2, X, Z, DCDDCC, Ra, Ca, $\pm y_{1i}=\pm y_{2i}$, $\frac{L}{R}=\frac{R_a\cdot C_a}{\alpha}$
C	$\begin{bmatrix}0 & \pm R\\ \pm 1 & 0\end{bmatrix}\begin{bmatrix}0 & \pm R\\ \pm 1 & 0\end{bmatrix}$ $\pm y_{1i}=\pm y_{2i}=\frac{\mp x_{2i}\pm x_{1i}}{sRC}$	$\mp x_{2i}$, $\mp x_{1i}$, Y1, Y2, X, Z, DCDDCC, Ra, Ca, $\pm y_{1i}=\pm y_{2i}$, $R\cdot C=\frac{R_a\cdot C_a}{\alpha}$
L, R	$\begin{bmatrix}\pm 1 & 0\\ 0 & \pm R\end{bmatrix}$ $\pm y_{16}=\frac{\pm x_{16}}{s\frac{L}{R}+1}=V_O$	$\pm x_{16}$, Y1, Y2, X, Z, DCDDCC, Ra, Ca, $\pm y_{16}=V_O$, $\frac{L}{R}=\frac{R_a\cdot C_a}{\alpha}$

Tab. 3. The transformation blocks.

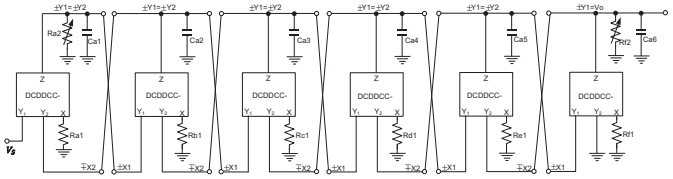

Fig. 11. A digitally controlled DDCC-based 6th-order tunable Butterworth low-pass active filter.

Then, we can cross-cascade their corresponding digitally controlled DDCC circuits to construct the filter. A 6th-order tunable Butterworth low-pass active filter using digitally controlled DDCCs, grounded resistors and grounded capacitors is presented as an example in this study. In this filter, V_{DD} = 1.8 V, $R_{a1}=R_{f1} \doteq 5.3$ kΩ, $R_{a2}=Rf2=5.3$ kΩ/α, $R_{b1}=R_{e1} \doteq 7.3$ kΩ, $R_{c1}=R_{d1} \doteq 9.9$ kΩ, $C_{a1}=C_{a6}=6$pF, and $C_{a2}=C_{a3}=C_{a4}=C_{a5}=12$ pF [15], [16]. Its configuration with six digitally controlled DDCCs is shown in Fig. 11.

CDN 8-bit SW (α)	Bandwidth	Output voltage (V_{P-P})	THD (%)
11111111 (1)	2.6 MHz	206 mV	1.09
01111111 (0.5)	1.25 MHz	218 mV	0.74
00111111 (0.25)	680 kHz	236 mV	0.69
00011111 (0.125)	363 kHz	261 mV	1.58
00001111 (0.0625)	187 kHz	225 mV	1.57
00000111 (0.03125)	93.2 kHz	235 mV	1.51
00000011 (0.015625)	48.4 kHz	265 mV	0.99
00000001 (0.0078125)	25.4 kHz	302 mV	5.35
00000000 (0.00390625)	12 kHz	326 mV	8.80

Tab. 4. The simulation results at an input voltage of 600 mV(V_{P-P}).

Filter type	Butterworth active low-pass filter
Order	6
Frequency Range	12 kHz ~ 2.6 MHz
Ripple	0 dB
THD	1.09 % @ 2.6 MHz
Voltage Supply	1.8 V
Power Consumption	3.6 mW
Chip Size	0.482×0.435 mm^2 (without PAD)
Technology	TSMC 0.18μm 1P6M mixed-mode process

Tab. 5. The specifications of the proposed filter.

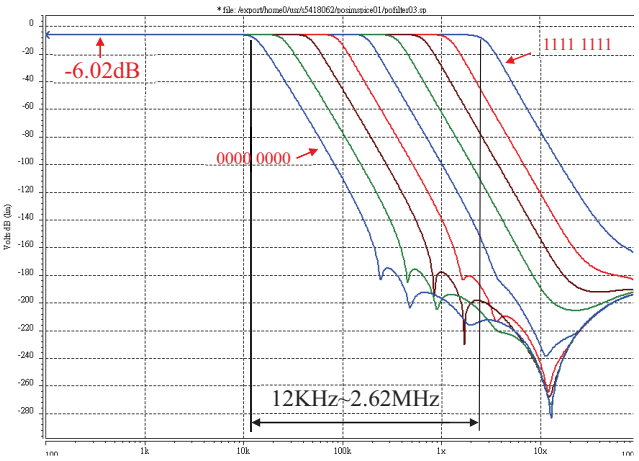

Fig. 12. The simulation frequency responses.

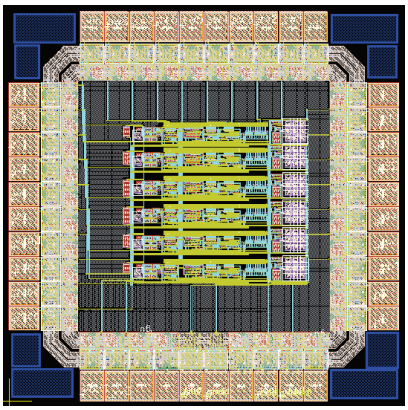

Fig. 13. The chip layout of the proposed filter.

4. Simulation Results

The proposed filter is tuned by a 8-bit CDN switch (the digital control factor α). Nine simulations with different values of α are conducted at an input voltage of 600 mV (peak-to-peak), and the range of the tuned frequencies is from 12 kHz to 2.6 MHz. The simulation results are shown in Tab. 4 and the frequency responses are shown in Fig. 12.

The filter is implemented in TSMC 0.18 μm 1P6M process with supply voltage VDD = 1.8 V. The chip layout is shown in Fig. 13, and the specifications of the filter are shown in Tab. 5. The chip area without PAD is 0.482 × 0.435 mm^2.

5. Conclusions

The design of a tunable differential difference current conveyor (DDCC) active filter using voltage-mode linear transformation (VMLT) method is presented. The bandwidth of such a filter can be tuned by the α factor (the digital value corresponding to the CDN binary switches) to adjust the output current value of the DDCC. A 6th-order tunable Butterworth low-pass active filter with digitally controlled DDCC is fabricated using 6 digitally controlled DDCCs along with 6 grounded capacitors and 8 grounded resistors. Its CDN circuits allows the bandwidth of the filter to be tuned by adjusting the α factor. The proposed filter has the following merits: easy and systematic design procedures are available, all capacitors and resistors are grounded, and the equations are simple. Furthermore, the design and circuits can be extended and applied to other applications.

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