MIDAS: Automated Approach to Design Microwave Integrated Inductors and Transformers on Silicon

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Abstract. *The design of modern radiofrequency integrated circuits on silicon operating at microwave and millimeter-waves requires the integration of several spiral inductors and transformers that are not commonly available in the process design-kits of the technologies. In this work we present an auxiliary CAD tool for Microwave Inductor (and transformer) Design Automation on Silicon (MIDAS) that exploits commercial simulators and allows the implementation of an automatic design flow, including three-dimensional layout editing and electromagnetic simulations. In detail, MIDAS allows the designer to derive a preliminary sizing of the inductor (transformer) on the bases of the design entries (specifications). It draws the inductor (transformer) layers for the specific process design kit, including vias and underpasses, with or without patterned ground shield, and launches the electromagnetic simulations, achieving effective design automation with respect to the traditional design flow for RFICs. With the present software suite the complete design time is reduced significantly (typically 1 hour on a PC based on Intel® Pentium® Dual 1.80 GHz CPU with 2-GB RAM). Afterwards both the device equivalent circuit and the layout are ready to be imported in the Cadence environment.*

Keywords

Electromagnetic simulations, electronic design automation, inductors, integrated circuits, microwaves, silicon, transformers.

1. Introduction

An accurate design of integrated inductors and transformers on silicon requires the adoption of 3D Electro-Magnetic (EM) simulators. To do this, the designer must define the process cross-section, draw the device geometry, set the boundary conditions, excitations and desired outputs, and finally launch the simulation. When the device meets the specifications, typically after a significant number of iterations including simulations and fine tuning of the geometry, the next design step is the layout drawing and S-parameters importing into the integrated circuit (IC) design environment, for schematic and post-layout simulations [1].

In spite of the commercial availability of very accurate EM simulators, the above procedure lacks of automation. Thereby, today this is an active research area characterized by a number of efforts in different directions [2], [3], [4]. In fact, in the traditional scenario, the design of integrated inductors and transformers on silicon is time consuming and entirely supported by designers' efforts [5]. Therefore, the overall time to the design completion is much longer than the time required by the 3D EM simulations. Indeed, a significant amount of time is devoted to the geometry drawing, which is very prone to mistakes inadvertently made by designers. A further difficulty is associated to the Design Rule Check (DRC) of the integrated inductor and transformer. This can be typically done only into the IC design environment according to the process design rules provided by the silicon foundry; whereas the spiral inductor and transformer are drawn by exploiting the geometry capture tools of the 3D EM simulator. Finally, a sufficiently accurate equivalent circuit model could be provided to allow the overall IC simulation in all the cases in which S-parameter descriptions may be not supported by the simulators (e.g. non-linear time-domain simulations such as transient simulations) [6].

Recently, our research group has developed a preliminary version of an auxiliary computer aided design (CAD) tool that allows the automation of microwave integrated inductor design on silicon [7], [8]. Despite this preliminary version provides a solution to the design automation of inductors, it does not provide any solution to the design automation of integrated transformers, which are today massively adopted for the design of microwave and millimeter-wave integrated circuits on silicon technology [9]. This paper addresses the need of speeding up the above design process and reports for the first type the extension of the preliminary software suite called MIDAS (Microwave Inductor Design Automation on Silicon) to the design automation of spiral transformers. In addition to the extension of the capabilities to transformers, the new developments address some important details about the inter-

nal algorithms of the scripts, which allow ad-hoc customizations of the proposed approach in support of specific needs. Moreover, we report also its application to the design of an entire inductor library SiGe-CMOS technology. Thereby, with its new developments reported hereinafter, MIDAS allows the designer to generate automatically the layout of inductor and transformer in the EM design environment, set and launch simulations. Moreover, MIDAS provides the support for the initial design of the inductor by evaluating geometric options on the basis of the performance requirements in terms of L and Q, and the equivalent circuit model of the simulated inductor.

This paper is organized as follows. Section 2 summarizes the state of art of inductor design on silicon in order to introduce the reader to the current scenario and appreciate the contribution to the design automation operated by MIDAS. Section 3 highlights the design automation operated by MIDAS, including script code descriptions, details and limitations, with emphasis on the new and original developments for transformers and script algorithms. Section 4 reports the results achieved for three representative cases of study in both CMOS and SiGe-CMOS processes. Finally, the conclusions are drawn in Section 5.

2. RFIC Design: State of the Art

The design of inductors on silicon starts from preliminary specifications derived by the RL basic model [10], as reported in EM design flow in Fig. 1.

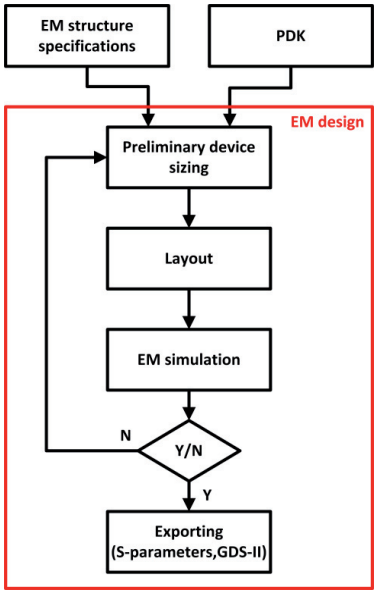


Fig. 1. Typical EM design flow on silicon.

The preliminary inductor sizing may be based on approximate closed-form analytical equations, which can provide an initial design space exploration [11]. More accurate models based on π-equivalent circuits could be used [12]-[19]. Such models are derived by numerical techniques (fitting procedures) or physical models. A deep discussion on this topic is beyond the scopes of this paper; however, a summary of effective models is reported in Tab. 1. Moreover it is worth saying that, despite of such models could be exploited to provide more accurate sizing of the preliminary inductor design, it is a common approach to skip such a task and focus the design efforts directly on full-wave EM simulations.

Therefore, assuming that 3D EM simulator is the appropriate design tool for the next step, the designer must define therein the process cross section, draw the device geometry, set the boundary conditions, excitations and desired outputs, and finally launch the simulation. When the device meets the specifications, typically after a significant number of iterations and fine tuning of the device geometry, the next design steps are the layout drawing and S-parameters exporting (for the subsequent importing into the IC design environment) and the completion of the RFIC design flow including parasitic extractions and post-layout simulations (see Fig. 1). It is worth mentioning that, in principle, the RFIC design flow could require additional fine tuning of the EM design, leading to additional refinement cycles (i.e. design, measurements and redesign). More importantly, note that these typical design phases, involving separately EM and IC design environments, lack of integration so that they are traditionally entirely supported by the designers' efforts.

Ref	Skin and prox. effects	Cap. coupling	Ind. coupling	Distributed effects	Freq. independent
[6]	yes	yes	no	no	yes
[12]	yes	yes	yes	yes	yes
[13]	yes	yes	yes	yes	yes
[14]	yes	yes	yes	no	no
[15]	yes	yes	no	no	yes
[16]	yes	yes	no	yes	yes
[17]	yes	yes	no	yes	no
[18]	yes	yes	yes	yes	yes
[19]	yes	yes	yes	yes	yes

Tab. 1. Equivalent circuit models of integrated inductor on silicon.

3. Proposed Methodology

MIDAS allows the designers to generate automatically the layout of the inductor and transformer in the EM design environment, set and launch simulations. Moreover, MIDAS provides also the support for the initial design of the inductor by evaluating geometric options on the basis of the performance requirements in terms of L and Q, and provides also the approximate equivalent π-model circuit of the inductor.

More in detail MIDAS is a software suite consisting of three tools as described hereinafter, in which each tool is independent and designed in order to support a specific design step. This current version of the suite takes into account two possible geometries for inductors: i) octagonal symmetric and ii) square. However, in principle, there are no limitations to its future extensions to other shapes and ad-hoc options for the allocation of the excitation ports. Anyway, thanks to an open access code, available on the project website [7], MIDAS can be extended by any user to meet the specific needs of the own design and simulations. The tool *First-guess Designer* allows the user to determine the geometric values that suit with the design constraints. *Layout Generator* allows the generation of the layout of the spiral inductor and transformers. *Equivalent Circuit Extractor*, based on the y-parameters computed by the full-wave simulator, extracts the π-model equivalent circuit.

3.1 First-Guess Designer

First-guess Designer offers to the designer the possibility to identify the preliminary geometric values and to achieve a rough evaluation of the inductance, series resistance and quality factor of an integrated inductor on silicon. The current version is limited to octagonal and square spirals.

Parameter	From	To
Number of turns (N)	1	3
Width (w)	1 μm	20 μm
Spacing (s)	1 μm	10 μm
Outer diameter (d_{out})	30 μm	400 μm

Tab. 2. Typical geometric values to cover the inductance range from 0.1 to 5 nH.

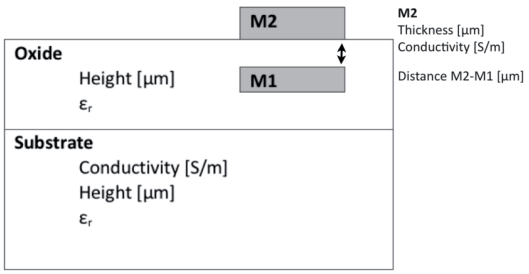


Fig. 2. Simplified cross-section of a typical commercial silicon process. Only the parameters used by the tool are highlighted. This approximation focuses on the two top metal layers and does not consider the isolation layer on top since its contribution is typically negligible, as well as the packaging (if any). If the oxide is made of layers with different dielectric constant, a simplification consists of considering a unique layer with averaged electrical properties.

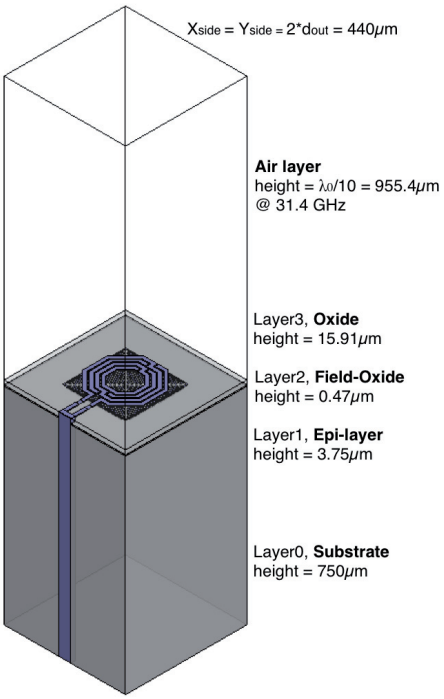
After selecting the type of shape (octagonal or square), the designer can operate through a window form interface to tune the four characteristic geometric parameters of the structure, such as the number of turns (N), width (w), spacing (s) and outer diameter (d_{out}). For typical commercial technology processes, the ranges of the geometric values shown in Tab. 2 allow the coverage of the inductances in the range from about 0.1 to 5 nH.

The designer is also required to input the operating frequency and some process dependent parameters. In particular *First-guess Designer* requires the insertion of the geometric and electrical properties of the metal layers used for the implementation of spirals, oxide layers and substrate. The notation used for the cross section geometry is reported in Fig. 2. The output data are obtained from the equations in [20], [21].

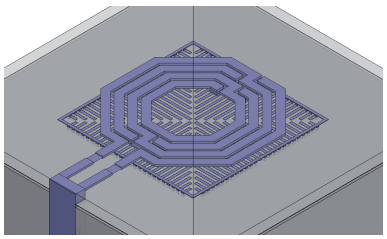
3.2 Layout Generator

The *Layout Generator* tool requires that the designer specifies the shape, i.e. square or octagonal, of the spiral inductor and if it is with or without patterned ground shield (PGS). For each selection, MIDAS launches a VBScript routine which guides the designer through the setup and execution of the EM simulation carried using High Frequency Structure Simulator (HFSS) by ANSYS [22]. However, in principle, MIDAS can be extended also to other EM commercial simulators. The *Layout Generator* draws the entire cross section of the layer stack and adds an additional layer of air on top having a thickness proportional to the frequency operation: the general settings of this tool are highlighted in Fig. 3. The ring of the PGS is also connected to the Si substrate using a number of vias (contacts). The ground ring has a square shape with characteristic size $d_{ring} = d_{out} + 2s$ in case of octagonal spirals, whereas $d_{ring} = d_{out} + 4w + 2s$ in case of square spirals. In the current version, the PGS, if required, is made of a number of strips (typically polysilicon) proportional to the dimensions of the ground ring: $N_{strips} = (d_{ring} / 2{\times}s)$-3. The width of each strip and the spacing between them is equal to s. It is worth saying that the PGS is usually realized by a much finer geometry (strip width is maybe be even 1 μm or smaller), but the proposed structure simplification represents a good tradeoff between description accuracy and computational complexity (i.e. simulation time).

The original geometry of the contacts has been simplified in order to reduce the mesh requirements. This means that, where more parallel vias are used within the same contact (i.e. multi-vias contact), then all the vias are replaced with a single via with a section area equal to the sum of each single vias area. Then, the contact is added from the ground ring to the substrate or from the ground ring to the PGS and from the PSG to the substrate (see Fig. 3c), which is assumed to be the first technology layer entered by the designer, i.e. Layer0. The other layers are then numbered progressively. There is not an upper limit to the number of layers to be drawn by MIDAS, but this number is entered by the designer.



(a)



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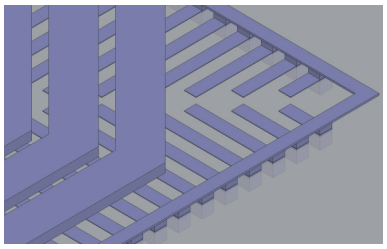


(c)

Fig. 3. General EM settings in MIDAS. Example of an octagonal spiral inductor with patterned ground shield (PGS) in a commercial 0.25μm BiCMOS process. The inductor has the following characteristic parameters: $N = 4$, $s = 4$ μm, $w = 12$ μm and $d_{out} = 220$ μm. Note that the vertical (axis z) dimension of a typical (Bi)CMOS process is dominated by the height of the Si-substrate, which is the bottom layer (tagged as Layer0 in MIDAS).

In order to illustrate the *Layout Generator* operation, the flow chart is shown in Fig. 4, which corresponds to the algorithm implemented by MIDAS to generate one of the four proposed inductor geometries.

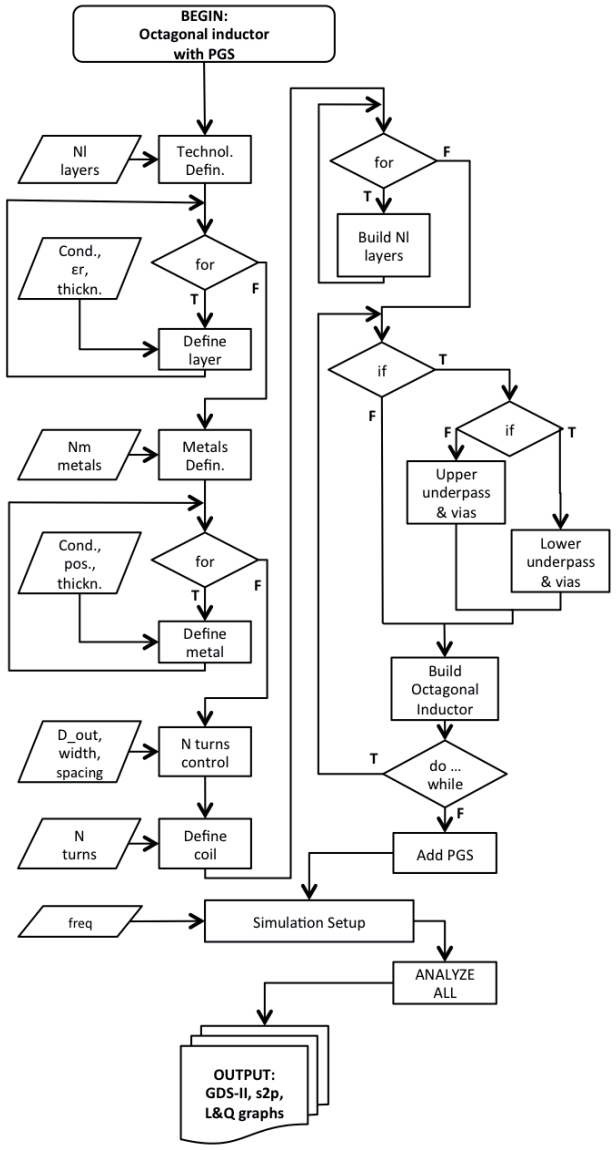


Fig. 4. Algorithm flow chart illustrating the operation of MIDAS to generate an octagonal inductor with PGS.

3.3 Equivalent Circuit Extractor

Once the full-wave simulation has been performed, the designer can automatically extract the π circuit model of the inductor by means of the *Equivalent Circuit Extractor* tool. It is required that Microsoft Excel is installed on the computer where MIDAS is running, since the output of this tool is an Excel spreadsheet containing the extracted circuit parameters. The extraction procedure performed by MIDAS adopts the method described in [6]. *Equivalent Circuit Extractor* provides the values of the π equivalent circuit model, shown in Fig. 5, as the results of the calculations derived for the equations presented in [23], [24]. Extensions to equivalent circuits for multi-port networks will be considered in future developments.

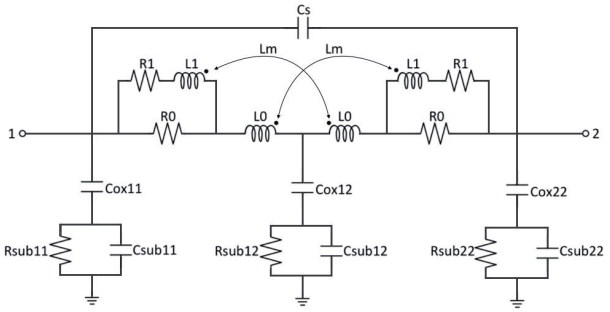


Fig. 5. π model used within Equivalent Circuit Extractor.

4. Experimental Results

In this section we report the simulation and experimental results of three relevant cases of study regarding the application of the complete MIDAS flow to the design of a square inductor. In particular, this spiral inductor has been implemented on silicon and successfully used in [25]. Moreover, we also report the application of MIDAS to the creation of an entire library of inductors and the extension of *Layout Generator* to the design of a transformer to be used in a 2.4 GHz power amplifier.

4.1 Complete MIDAS Flow

As a first case of study, we report the experimental results obtained by M. Kraemer et al. in [25]. The measured inductor (about 0.12 nH) is realized in a 65nm bulk CMOS technology by STMicroelectronics (STM) for an operating frequency close to 60 GHz. The characteristic design parameters are: $N = 1.25$, $s = 2$ µm, $w = 3$ µm and $d_{out} = 31$ µm. The parasitic effects of pads are not included in the EM problem description.

First-guess Designer ran on a Dual 1.80GHz CPU Pentium® with 2-GB RAM by Intel®. The required inductance value is 0.12 nH. One of the size sets for the square inductor sizing is given by the following set: $d_{out} = 31$, $w = 3$, $s = 2$, and $N = 1.25$, which corresponds to the geometry reported in [26].

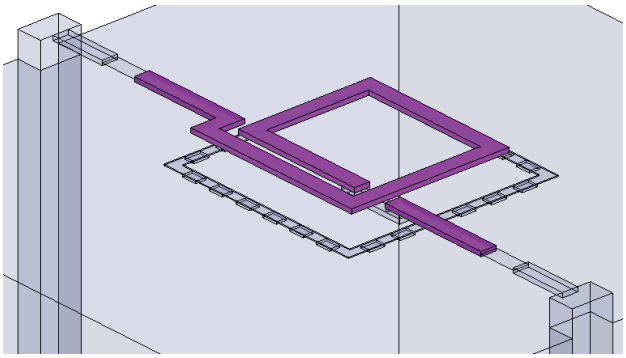
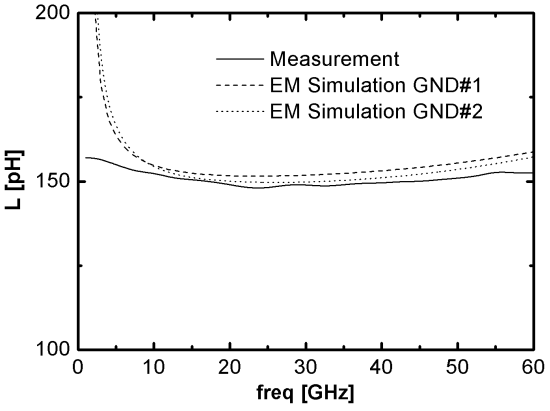


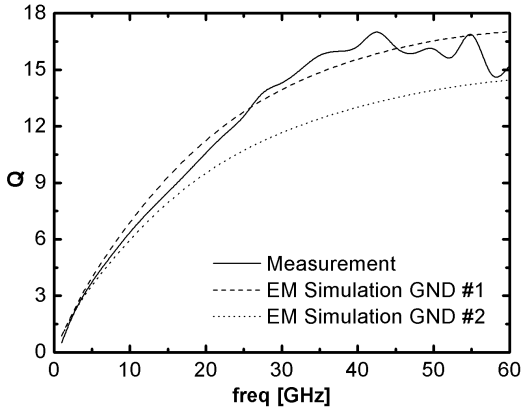
Fig. 6. HFSS layout resulting from the EM Structure Simulation tool (i.e. GND#1). The sizes are: $N = 1.25$, $s = 2$ µm, $w = 3$ µm and $d_{out} = 31$ µm.

The simulation time is approximately equal to one second on a PC based on Dual 1.80GHz CPU Pentium® with 2-GB RAM by Intel®. The tool estimates the values for L, Q and R, as follows: $L = 0.156$ nH, $Q = 13.07$, $R = 1.45$ Ω.

Figure 6 shows the output of the EM Structure Simulator resulting directly from the layout in the HFSS environment. Therein we generated a square inductor without PGS by using the set of geometric values previously above. L and Q achieved by simulations and measurements are reported in Fig. 7. The square spiral inductor has been simulated in HFSS adopting the ground structure as in Fig. 3a, hereinafter refereed as GND#2. Moreover, in order to evaluate the effectiveness of such setting of the EM simulator, we report also the EM simulation results achieved by using a different grounding structure, namely GND#1, such as reported therein [9]. GND#1 is composed by a metallic ground plate made of the bottom metal layer available in the technology process. The ground plate has 80-µm square hole centered below the inductor. GND#2 consists of a vertical PEC column connecting each port to the bottom (automatically set by HFSS as a PEC) of the substrate box.



a)



b)

Fig. 7. a) L and b) Q from measurements and EM simulations for the inductor in [25].

The results of the EM simulations of both the structures show good agreements with the measurements. The simulation results for GND#1 show a good matching with the measured Q. Moreover, on the basis of the measured results, the comparison between the results achieved for GND#1 show a higher accuracy with respect to those achieved for GND#2, which underestimates Q at higher frequencies. This is in agreement with the fact that GND#1 is very close to the grounding structure really implemented in the experimental test chip. The simulation time was about two minutes (excluding the time required for the HFSS simulation) on a PC based on a Dual 1.80GHz CPU Pentium® with 2-GB RAM by Intel®.

C_S [fF]	R_0 [Ω]	L_0 [nH]	R_1 [Ω]	L_1 [nH]	L_m [nH]
59.2	0.955	0.7	65.2	0.03	0.15
C_{ox11} [fF]		C_{ox12} [fF]		C_{ox22} [fF]	
46.6		92.4		45.8	
R_{sub11} [Ω]		R_{sub12} [Ω]		R_{sub22} [Ω]	
5063		4935		4807	
C_{sub11} [pF]		C_{sub12} [pF]		C_{sub22} [pF]	
0.11		0.23		0.11	

Tab. 3. π circuit parameters values for the inductor presented in [25].

At this stage, we achieve as the values of the equivalent π circuit of Fig. 5 by running the *Equivalent Circuit Extractor* tool. In particular, for the above structure of Fig. 6, we achieve the set of circuit components reported in Tab. 3.

4.2 Inductor Library

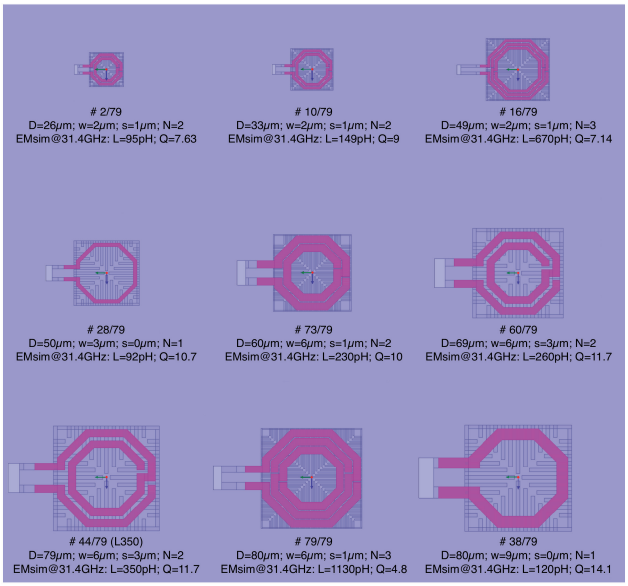


Fig. 8. Layout of the inductors. Each structure has been automatically generated in less than one minute.

For the project described in [27], [28] we needed a library of inductors operating in the Ka-band and centered at 31.4 GHz, with inductances ranging from 50 to 500 pH. By running MIDAS for a two-day simulation campaign we have achieved the goal in three different PCs based on 1.80GHz CPU Pentium® with 2-GB/4-GB RAM by Intel® Dual. The set of specifications for the inductors were:

1) $Q \geq 10$
2) $d_{out} \leq 80$ μm

We were able to achieve the goal by designing and simulating 79 inductors. Figure 8 shows nine of the 79 inductors designed in a 250-nm SiGe BiCMOS technology developed at the IHP foundry. This process allows for 3 metal layers and thick metals option on M4 and M5. The top metal layer has a thickness of 3 μm and is suitable to the implementation of spiral inductors with an adequate quality factor, and planar transmission lines. In particular, we were interested in octagonal inductors with PGS. The sizes of the developed inductor library are summarized in Tab. 4. These inductors were used for the successful design of the 36.8 GHz radiometer presented in [28].

Inductor#	d_{out} [μm]	w [μm]	s [μm]	N turns	EM sim. @ 31.4 GHz L [pH]	Q
55/79	39	5	-	1	51	10.3
30/79	55	3	-	1	104	10.8
50/79	72	3	-	1	150	10.8
76/79	59	6	2	2	197	10.7
63/79	68	6	3	2	253	11.6
62/79	73	6	3	2	297	11.8
44/79	79	6	3	2	350	11.7
58/79	75	4	3	2	400	10.8
49/79	80	4	3	2	452	10.5
43/79	80	4	2	2	500	10

Tab. 4. Library of inductor developed using MIDAS.

4.3 Transformers

The interest in integrated transformers on silicon rapidly grew over the last years [9]. They are widely exploited today in power combining techniques for the implementation of high-efficiency Power Amplifiers (PAs). In addition, heterogeneous transformers (e.g. with the primary in silicon and the secondary in a flexible substrate) have been proposed to provide contactless and low-cost interface between chip and external electronic systems [29]. A transformer is typically adopted also to implement integrated balun, e.g. in the push-pull topology. The 2:1 octagonal transformer described in [30] is a typical example for this kind of application. The primary spiral consists

of one turn with a central-tap port, whereas the secondary spiral consists of a two-turn spiral realized on the same metal plane of the primary, as represented in the schematic of Fig. 9a. Due to the symmetry of the overall structure, the primary spiral can be conveniently represented as the split into two symmetric semi-spirals L_1 with respect to the central tap.

The generation of the transformer geometry has been automated by following the same principle adopted for the design automation of inductors. However, the design of a transformer imposes new and additional challenges that require the implementation of specific and consistent new features for the design automation. In this regard, it is worth mentioning that an inductor is a two-port device, whereas a transformer is a four-port device, as shown in Fig. 9a, but to mention a few. In the specific case of the designed balun, the transformer has been simulated as a five-port device, as shown in Fig. 9b, since the central tap grounding was external to the spirals.

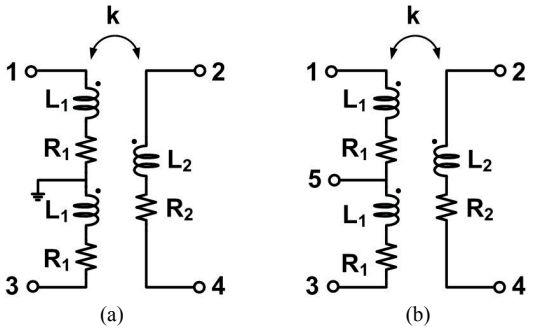


Fig. 9. Schematic of the balun as (a) four-port device and (b) five-port device. The primary spiral is split into two spirals L_1 with respect to the central tap.

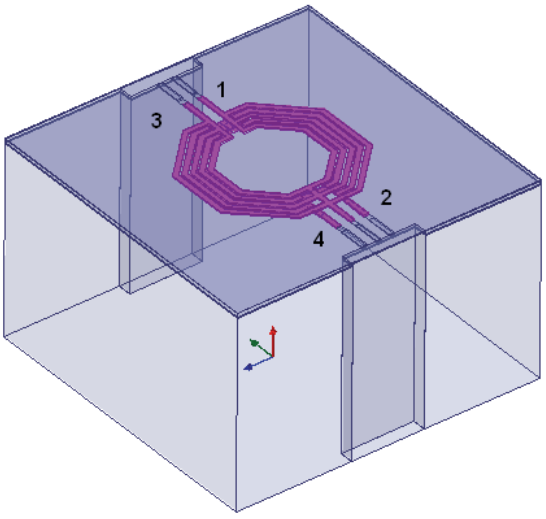


Fig. 10. Electromagnetic structure of the symmetric transformer as a five-port device. Port 5 (not labeled), corresponding to the central tap of the secondary spiral, is in between the ports 2 and 4, according to the port labels reported in the schematic of Fig. 9b.

In this important extension of the capabilities of MIDAS, the designer can draw the structure in few steps (with the own custom script) by simply entering the transformer dimensions. A technology file can be used for the definition of the chip cross-section within the EM simulator as in the previous case of the inductor design.

As an example of application, Fig. 10 shows the EM structure of the transformer designed by MIDAS through HFSS. The external and internal diameters are equal to 410 and 240 μm, respectively. The width of the metal layer is 13 μm, whereas the spacing is 5 μm. In this specific design customization, the primary spiral of the transformer consists of three tracks in parallel in order to reduce the series parasitic resistance and increase the quality factor. In addition the secondary spiral is interlaced with the primary spiral in order to increase the coupling factor *k*.

Frequency [GHz]	**Primary**			
	N turns	**L_1 [nH]**	**R_1 [Ω]**	
2,45	1	0,15	0,24	
Secondary				**k**
N turns	**L_2 [nH]**	**R_2 [Ω]**		
2	2,25	1,60	0,65	

Tab. 5. Simulation results of the octagonal transformer obtained by the EM simulations as a five-port device in which port 5 has been grounded.

The simulation of the EM structure of Fig. 10 has been carried-out considering the cross-section of a 90-nm bulk CMOS technology. The primary and secondary spirals have been implemented on metal 9, which is characterized by a 3.2 μm thickness with a conductivity of 4.5×10^7 S/m. The simulation results of the designed transformer are reported in Tab. 5; inductances and resistances have been obtained from the Z parameters according to the expressions reported hereinafter. These results have been obtained in less than one hour, including the time needed for the layout generation.

$$L_1 = \frac{\mathrm{Im}\{Z_{11\mathrm{d}}\}}{\omega}, \tag{1}$$

$$L_2 = \frac{\mathrm{Im}\{Z_{22\mathrm{d}}\}}{\omega}, \tag{2}$$

$$R_1 = \mathrm{Re}\{Z_{11\mathrm{d}}\}, \tag{3}$$

$$R_2 = \mathrm{Re}\{Z_{22\mathrm{d}}\}, \tag{4}$$

$$k = \frac{\left|\mathrm{Im}\{Z_{21\mathrm{d}}\}\right|}{\sqrt{\mathrm{Im}\{Z_{11\mathrm{d}}\}\,\mathrm{Im}\{Z_{22\mathrm{d}}\}}} \tag{5}$$

where the subscript d stands for the differential Z parameters obtained for the two-port equivalent description from the original four-port description. These can be obtained by using of the following expressions in terms of S-parameters and the well-known transformation formulas (not reported hereinafter) from S to Z parameters [31].

$$S_{11d} = \frac{1}{2}(S_{11}\text{-}S_{21}\text{-}S_{12}+S_{22}), \quad (6)$$

$$S_{12d} = \frac{1}{2}(S_{13}\text{-}S_{23}\text{-}S_{14}+S_{24}), \quad (7)$$

$$S_{21d} = \frac{1}{2}(S_{31}\text{-}S_{41}\text{-}S_{32}+S_{42}), \quad (8)$$

$$S_{22d} = \frac{1}{2}(S_{33}\text{-}S_{43}\text{-}S_{34}+S_{44}). \quad (9)$$

5. Conclusions

This paper presented an auxiliary CAD tool, namely MIDAS, allows a drastic reduction of the time required by inductor design on silicon. Based on full-wave EM simulations, MIDAS allows us to speed up the design phase by introducing automatic steps in the electromagnetic design flow. MIDAS is based on three different tools, which assist the designer from the first guess sizing to the GDS-II exporting, by means of custom software tools and contributing significantly to speed up the entire design flow. The tool settings have been presented, discussed and applied to different cases of study. In particular, this paper addressed the extension of the tool capabilities with respect to its preliminary implementation, which was limited to inductor design automation only. In particular, in its current developments reported herein, MIDAS has been significantly extended in order to support also the increasing demand of design automation of integrated transformers. The internal algorithms of the scripts have been provided in order to extend its flexibility to ad-hoc customizations of the proposed approach in support of specific needs. The tool is available to the scientific community under free common creative license. The effectiveness of the approach proposed within MIDAS has been confirmed by the experimental results on test-chips. Further extensions of the current capabilities and versatility will be considered in its future developments.

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