Novel Resistorless Mixed-Mode PID Controller with Improved Low-Frequency Performance

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Abstract. *This paper introduces a new resistorless mixed-mode proportional-integral-derivative (PID) controller. It employs six simple transconductors and only two grounded capacitors. The proposed PID controller offers several advantageous features of resistorless configuration, use of grounded capacitors, independent electronic-tuning characteristic of its parameters, and mixed-mode operation such as current, transimpedance, transadmittance, and voltage modes. The parasitic element effects of the transconductors on the proposed controller are investigated and the improved low-frequency performance of the proposed controller is then discussed. As applications, the proposed controller is demonstrated on two closed-loop systems. The PSPICE simulations with TSMC 0.18μm CMOS process and ±0.9 V supply voltage verify the theoretical analysis.*

Keywords

PID controller, grounded capacitor, resistorless, mixed-mode, electronic tunability.

1. Introduction

In analog circuit design, many researchers have been directed towards the development of voltage-mode and current-mode circuits. However, the total effectiveness of the circuitry will be increased if signal processing is performed along with voltage-current interfacing using transadmittance or transimpedance mode. Moreover, the mixed-mode circuit including voltage-mode (i.e. both input and output as voltage), current-mode (i.e. both input and output as current), transadmittance-mode (i.e. input as voltage and output as current), and transimpedance-mode (i.e. input as current and output as voltage) plays a very important role in the special applications where we need to interface a voltage-mode circuit with a current-mode circuit and vice versa. Thus, the mixed-mode circuit has challenged many researchers especially in modern microelectronic system applications [1]-[4].

A proportional-integral-derivative (PID) controller is an important controller finding application in a wide variety of control systems because of its simplicity in design, low cost, and ease in parameter tuning [5]-[7]. Several voltage-mode and current-mode PID controllers have been reported using active building blocks such as second generation current conveyors (CCIIs) [8]-[11], current differencing buffered amplifiers (CDBAs) [12], current controlled current conveyors (CCCIIs) [13], and operational transconductance amplifiers (OTAs) [14]. Most of the PID controllers employ grounded capacitors [9], [10], [11], [13], and [14]. Thus, these controllers are suitable for integrated circuit implementation. Unfortunately, most of the presented circuits require external resistors [8]-[13] and lack electronic tunability [8]-[12]. Only one of those controllers suggests resistorless structure design [14]. In [14], eight OTAs and two grounded capacitors are used. Although the resistorless PID controller of [14] offers the attractive features of electronic tuning and the use of grounded capacitors, it uses an excessive number of active elements. Furthermore, all of the existing PID controllers can be classified either as voltage-mode or current-mode. No work has been done in the domain of mixed-mode PID controller. So, it is the purpose of this paper to present such a resistorless mixed-mode PID controller.

In this paper, a new resistorless mixed-mode PID controller is presented. The proposed PID controller consists of six simple transconductors and only two grounded capacitors. The circuit exhibits several attractive features of mixed-mode operation without changing its configuration, resistorless structure, the use of grounded capacitors, and electronic tuning characteristic of proportional gain, integral time constant, and derivative time constant parameters. These parameters can be independently adjusted by bias currents of the transconductors. In addition, parasitic element effects of the transconductors on the proposed PID controller at sufficiently low frequencies are examined in detail. The PSPICE simulations are used to demonstrate the performances of the proposed mixed-mode PID controller and its applications.

2. Circuit Description

2.1 Basic Circuit Approach

A basic circuit structure of the proposed resistorless mixed-mode PID controller is shown in Fig. 1. It employs ten voltage-controlled current sources and two grounded capacitors. The current relation of node *A* produces

$$V_1 = \frac{I_1}{k_2}. \tag{1}$$

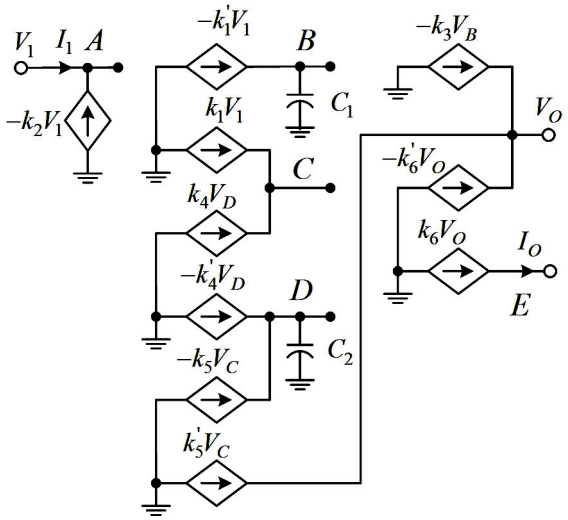

Fig. 1. Basic circuit of the proposed mixed-mode PID controller.

Setting $k_1 = k_1'$, $k_4 = k_4'$, $k_5 = k_5'$, and $k_6 = k_6'$ gives the following equations:

$$I_O = k_1(1 + \frac{k_3}{sC_1} + \frac{sC_2}{k_4})V_1, \tag{2}$$

and

$$V_O = \frac{k_1}{k_6}(1 + \frac{k_3}{sC_1} + \frac{sC_2}{k_4})V_1 \tag{3}$$

where k_i is the transconductance gain of the i^{th} voltage-controlled current source. From above equations, the current, transimpedance, transadmittance, and voltage modes of the proposed PID controller produce in the following conditions:

(i) If $I_1 = I_{IN}$, the following current-mode and transimpedance-mode transfer functions of the proposed PID controller are respectively obtained:

$$H_{I1}(s) = \frac{I_O}{I_{IN}} = \frac{k_1}{k_2}(1 + \frac{k_3}{sC_1} + \frac{sC_2}{k_4}), \tag{4}$$

and

$$H_{Z1}(s) = \frac{V_O}{I_{IN}} = \frac{k_1}{k_2 k_6}(1 + \frac{k_3}{sC_1} + \frac{sC_2}{k_4}). \tag{5}$$

(ii) If $V_1 = V_{IN}$, the following transadmittance-mode and voltage-mode transfer functions of the proposed PID controller are respectively given:

$$H_{G1}(s) = \frac{I_O}{V_{IN}} = k_1(1 + \frac{k_3}{sC_1} + \frac{sC_2}{k_4}), \tag{6}$$

and

$$H_{V1}(s) = \frac{V_O}{V_{IN}} = \frac{k_1}{k_6}(1 + \frac{k_3}{sC_1} + \frac{sC_2}{k_4}). \tag{7}$$

2.2 Proposed Mixed-Mode PID Controller

This section presents the realization of the proposed mixed-mode PID controller using transconductor-capacitor approach. Therefore, the property of the transconductor is briefly reviewed. The CMOS realization of a simple transconductor using four transistors and two current sources is shown in Fig. 2(a) [15]. It is assumed that all transistors operate in the saturation region and the substrates of these transistors are connected to their respective sources. The PMOS and the NMOS transistors are also assumed to have the same transconductance parameters. The equivalent circuit of an ideal transconductor is shown in Fig. 2(b) and the current outputs of the transconductor can be expressed as

$$I_P = -I_N = g_m(V^+ - V^-), \tag{8}$$

where g_m is the transconductance of the NMOS transistor and defined by

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_B}, \tag{9}$$

where μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area, W/L is the aspect ratio of the transistor and I_B is the bias current of the transconductor.

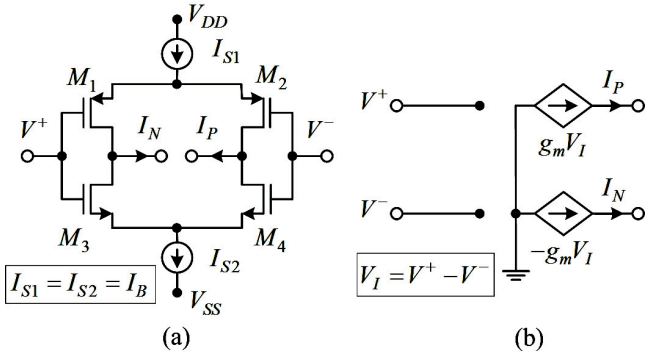

Fig. 2. (a) Simple CMOS transconductor, (b) its equivalent circuit.

When the voltage-controlled current sources of the proposed basic circuit as shown in Fig. 1 are replaced by the transconductor of Fig. 2(a), the proposed resistorless mixed-mode PID controller is shown in Fig. 3. It contains only six transconductors and two grounded capacitors. Routine analysis of this circuit produces transfer functions

which are in accordance with (4)-(7) setting $k_i = g_{mi}$, where g_{mi} is the transconductance of the i^{th} transconductor. Thus, the current-mode, transimpedance-mode, transadmittance-mode, and voltage-mode transfer functions of the proposed PID controller are respectively demonstrated:

$$H_{I2}(s) = \frac{I_O}{I_{IN}} = \frac{g_{m1}}{g_{m2}}\left(1 + \frac{g_{m3}}{sC_1} + \frac{sC_2}{g_{m4}}\right), \quad (10)$$

$$H_{Z2}(s) = \frac{V_O}{I_{IN}} = \frac{g_{m1}}{g_{m2}g_{m6}}\left(1 + \frac{g_{m3}}{sC_1} + \frac{sC_2}{g_{m4}}\right), \quad (11)$$

$$H_{G2}(s) = \frac{I_O}{V_{IN}} = g_{m1}\left(1 + \frac{g_{m3}}{sC_1} + \frac{sC_2}{g_{m4}}\right), \quad (12)$$

and

$$H_{V2}(s) = \frac{V_O}{V_{IN}} = \frac{g_{m1}}{g_{m6}}\left(1 + \frac{g_{m3}}{sC_1} + \frac{sC_2}{g_{m4}}\right). \quad (13)$$

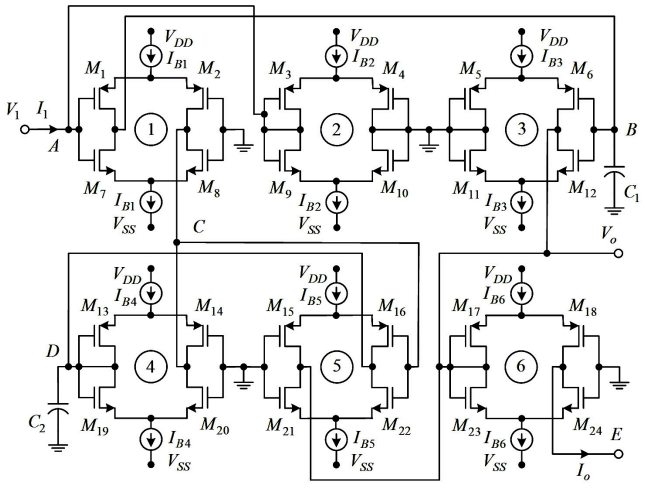

Fig. 3. The proposed resistorless mixed-mode PID controller.

The comparison of $H(s) = K_P(1 + 1/sT_I + sT_D)$ and (10)-(13) provides the proportional gain (K_P), the integral time constant (T_I), and the derivative time constant (T_D) parameters of the proposed mixed-mode PID controller in the following equations:

$$K_{PI} = \frac{g_{m1}}{g_{m2}}, \quad (14)$$

$$K_{PZ} = \frac{g_{m1}}{g_{m2}g_{m6}}, \quad (15)$$

$$K_{PG} = g_{m1}, \quad (16)$$

$$K_{PV} = \frac{g_{m1}}{g_{m6}}, \quad (17)$$

$$T_{II} = T_{IZ} = T_{IG} = T_{IV} = \frac{C_1}{g_{m3}}, \quad (18)$$

and

$$T_{DI} = T_{DZ} = T_{DG} = T_{DV} = \frac{C_2}{g_{m4}}. \quad (19)$$

From (14)-(19), these parameters can be adjusted electronically by changing the values of g_{mi} via the bias current of the i^{th} transconductor. The proportional gain, the integral time constant, and the derivative time constant parameters of the proposed resistorless PID controller can be altered independently. It should be noted that the proposed circuit is a resistorless PID controller like the previous circuit in [14], but the structure of the proposed circuit requires less number of active elements than that of the circuit of [14]. Furthermore, the circuit of [14] provides a voltage-mode PID controller while the proposed circuit offers a mixed-mode PID controller.

The sensitivities of the parameters of the proposed mixed-mode PID controller with respect to active and passive elements yield the acceptably low values as follows:

$$S_{g_{m1}}^{K_{PI}} = -S_{g_{m2}}^{K_{PI}} = 1, \quad (20)$$

$$S_{g_{m1}}^{K_{PZ}} = -S_{g_{m2}}^{K_{PZ}} = -S_{g_{m6}}^{K_{PZ}} = 1, \quad (21)$$

$$S_{g_{m1}}^{K_{PG}} = S_{g_{m1}}^{K_{PV}} = -S_{g_{m6}}^{K_{PV}} = 1, \quad (22)$$

$$S_{C_1}^{T_{II}} = -S_{g_{m3}}^{T_{II}} = S_{C_1}^{T_{IZ}} = -S_{g_{m3}}^{T_{IZ}} = 1, \quad (23)$$

$$S_{C_1}^{T_{IG}} = -S_{g_{m3}}^{T_{IG}} = S_{C_1}^{T_{IV}} = -S_{g_{m3}}^{T_{IV}} = 1, \quad (24)$$

$$S_{C_2}^{T_{DI}} = -S_{g_{m4}}^{T_{DI}} = S_{C_2}^{T_{DZ}} = -S_{g_{m4}}^{T_{DZ}} = 1, \quad (25)$$

and

$$S_{C_2}^{T_{DG}} = -S_{g_{m4}}^{T_{DG}} = S_{C_2}^{T_{DV}} = -S_{g_{m4}}^{T_{DV}} = 1. \quad (26)$$

2.3 Parasitic Element Effects

In this sub-section, the parasitic element effects of transconductor on the PID controller performance are carried out. Fig. 4 shows the equivalent circuit of the transconductor including its parasitic elements. It is shown that input terminals exhibit low-value capacitances C_{I+} and C_{I-} and output terminals exhibit low-value capacitances C_P and C_N with low-value conductances g_P and g_N, respectively.

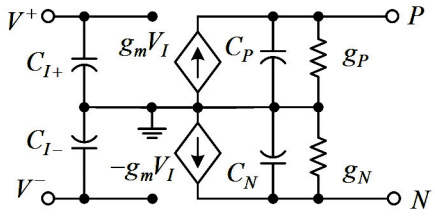

Fig. 4. The equivalent circuit of the transconductor including its parasitic elements.

Taking into account the above parasitic elements of the transconductor, routine analysis of the proposed PID controller as shown in Fig. 3 results in the following equations:

$$V_1 = \frac{I_1}{g_{m2} + y_A}, \tag{27}$$

$$V_O = \frac{g_{m1}}{g_{m6} + y_{Vo}}\left(1 + \frac{g_{m3}}{y_B} + \frac{y_D}{g_{m4}}\right)V_1 - \Delta_1, \tag{28}$$

and

$$I_O = \frac{g_{m1}}{1 + \dfrac{y_{Vo}}{g_{m6}}}\left(1 + \frac{g_{m3}}{y_B} + \frac{y_D}{g_{m4}}\right)V_1 - y_E V_E - \Delta_1 \tag{29}$$

where Δ_1 is given by

$$\Delta_1 = \left(1 + \frac{y_D}{g_{m4}}\right)\frac{y_C}{g_{m6} + y_{Vo}}V_C \tag{30}$$

where

$$y_A = g_{N2} + s(C_{I1+} + C_{I2+} + C_{N2}), \tag{31}$$

$$y_B = g_{N1} + s(C_1 + C_{N1} + C_{I3-}), \tag{32}$$

$$y_C = g_{P1} + g_{P4} + s(C_{P1} + C_{P4} + C_{I5-}), \tag{33}$$

$$y_D = g_{N4} + g_{P5} + s(C_2 + C_{I4+} + C_{N4} + C_{P5}), \tag{34}$$

$$y_E = g_{P6} + sC_{P6}, \tag{35}$$

and

$$y_{Vo} = g_{P3} + g_{N5} + g_{N6} + s(C_{P3} + C_{N5} + C_{I6+} + C_{N6}) \tag{36}$$

where C_{Ii+}, C_{Ii-}, C_{Pi}, C_{Ni}, g_{Pi} and g_{Ni} are the parasitic capacitances and the parasitic conductances of the i^{th} transconductor, respectively. Note that the terms of y_A, y_C, y_E, and y_{Vo} are effective at very high frequencies. In addition, the effects of the parasitic capacitances C_{N1}, C_{I3-}, C_{I4+}, C_{N4}, and C_{P5} are negligible because these parasitic capacitors are quite small as compared with the external capacitors ($C_1 >> C_{N1} + C_{I3-}$ and $C_2 >> C_{I4+} + C_{N4} + C_{P5}$). Also, the parasitic conductance g_{N1} in (32) affects the low-frequency performance of the proposed PID controller. To reduce the effect of the parasitic conductance, a negative grounded conductor as shown in Fig. 5 is connected in parallel to the external capacitor C_1 of the proposed PID controller as shown in Fig. 3.

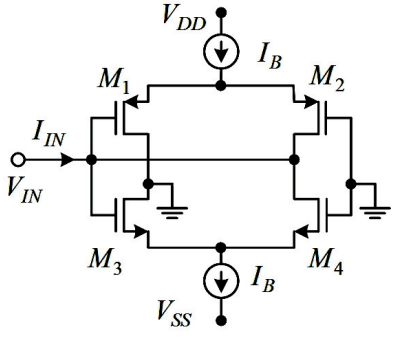

Fig. 5. A negative grounded conductor as compensated conductor.

The conductance of the negative grounded conductor can be expressed as

$$g_{COMP} = \frac{I_{IN}}{V_{IN}} = -g_m + g_P. \tag{37}$$

From (37), the conductance g_m should be selected greater than g_P to obtain a negative grounded conductor.

3. Application Examples

To illustrate the applications of the proposed mixed-mode PID controller of Fig. 3, two closed-loop systems are depicted in Fig. 6 and Fig. 7. The closed-loop system of Fig. 6 employs the proposed PID controller for current-mode and a current-mode low-pass filter as a plant. The closed-loop system of Fig. 7 consists of the proposed PID controller for transimpedance-mode and a transadmittance-mode low-pass filter as a plant. Those PID controllers are used to improve some performances of the closed-loop systems.

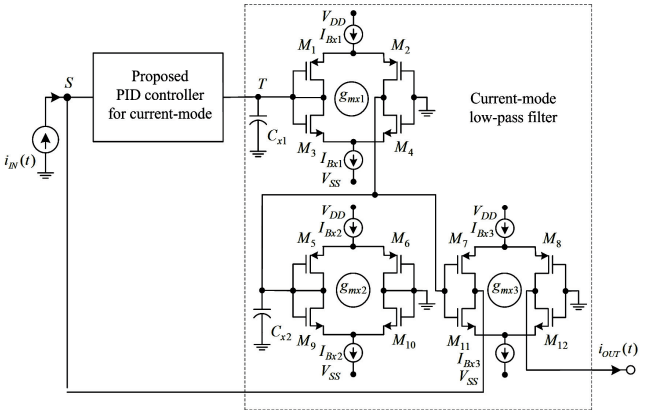

Fig. 6. Closed-loop system of the proposed PID controller for current-mode and a current-mode low-pass filter.

The transfer functions of the current-mode and transadmittance-mode low-pass filters are respectively given in the following equations:

$$P_1(s) = \frac{g_{mx1}g_{mx3}}{(g_{mx1} + sC_{x1})(g_{mx2} + sC_{x2})}, \tag{38}$$

and

$$P_2(s) = \frac{g_{my1}g_{my2}g_{my4}}{(g_{my2} + sC_{y1})(g_{my3} + sC_{y2})}. \tag{39}$$

The transfer functions of the closed-loop systems are then expressed as

$$H_{CL1}(s) = \frac{H_{I2}(s)P_1(s)}{1 + H_{I2}(s)P_1(s)}, \tag{40}$$

and

$$H_{CL2}(s) = \frac{H_{Z2}(s)P_2(s)}{1 + H_{Z2}(s)P_2(s)} \tag{41}$$

where $H_{I2}(s)$ and $H_{Z2}(s)$ are current-mode and transimpedance-mode transfer functions of the proposed mixed-

mode PID controller as shown in (10) and (11), respectively.

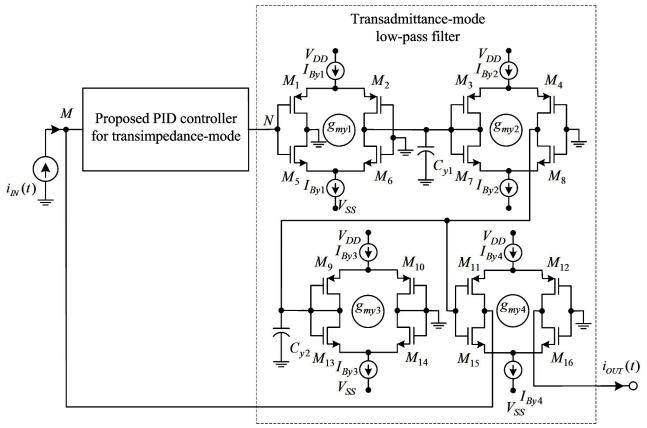

Fig. 7. Closed-loop system of the proposed PID controller for transimpedance-mode and a transadmittance-mode low-pass filter.

4. Simulation Results

In order to confirm the theoretical validity of the proposed mixed-mode PID controller, the transconductor as shown in Fig. 2(a) has been simulated using PSPICE program based BSIM3 level 7 transistor models for the TSMC 0.18 µm CMOS process available from MOSIS [16] with ±0.9 V supply voltage. To reduce the channel length modulation effect of the MOS transistor, the channel lengths of all transistors are selected as 0.54 µm [17]. The widths of the NMOS and the PMOS transistors are selected as 3.6 µm and 9 µm, respectively.

The proposed mixed-mode PID controller as shown in Fig. 3 is designed with I_{B1} = 162 µA, I_{B2} = I_{B6} = 18 µA, I_{B3} = I_{B4} = I_{B5} = 200 µA, C_1 = 20 nF, and C_2 = 0.02 nF for the PID parameters of K_{PI} = K_{PV} = 3, K_{PZ} = 18.75 kV/A, K_{PG} = 0.48 mA/V, T_{II} = T_{IV} = T_{IZ} = T_{IG} = 36.36 µs, and T_{DI} = T_{DV} = T_{DZ} = T_{DG} = 36.36 ns. The power consumption of the proposed controller is about 1.44 mW. The resulted frequency responses of the proposed PID controller for current, transimpedance, transadmittance, and voltage modes are obtained as shown in Fig. 8 to Fig. 11. The dashed and solid lines represent the ideal and simulated responses of the controller, respectively. It should be noticed that the simulated and the ideal frequency responses of the proposed PID controller are in good agreement from 40 Hz to 40 MHz. The differences of them in the low- and high-frequency regions primarily arise from the parasitic element effects of the transconductors. Moreover, the simulated frequency responses of the proposed controller are rolled off at very high frequencies because of the parasitic element effects in (28) and (29). Then, the very high-frequency noisy input can be reduced by the proposed controller.

To illustrate the frequency-domain performance of the proposed PID controller with compensated transconductor, the parasitic conductance g_{N1} is computed as g_{N1} = 5.64 µA/V. Then, the bias current of the compensated transconductor of Fig. 5 is selected as I_B = 0.484 µA. As examples, the ideal, uncompensated, and compensated frequency responses of proposed PID controller for current-mode and transimpedance-mode are shown in Fig. 12 and Fig. 13.

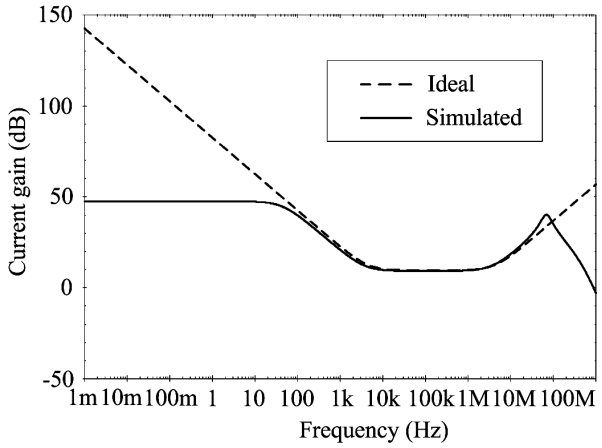

Fig. 8. Frequency responses of the proposed mixed-mode PID controller for current-mode.

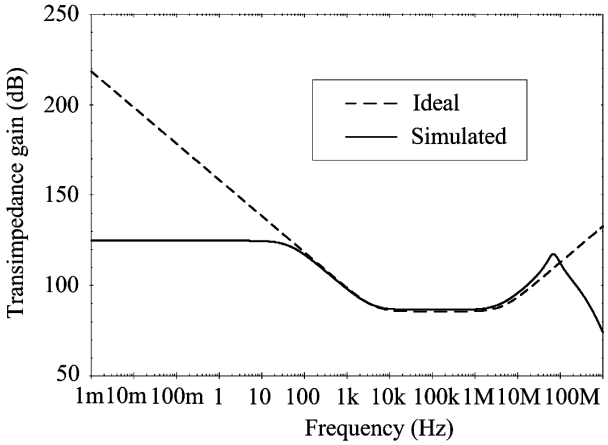

Fig. 9. Frequency responses of the proposed mixed-mode PID controller for transimpedance-mode.

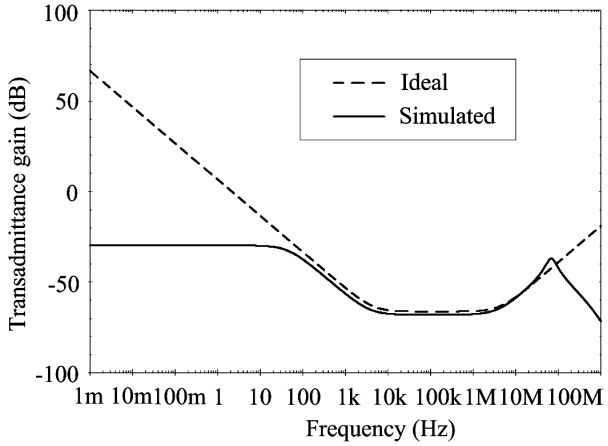

Fig. 10. Frequency responses of the proposed mixed-mode PID controller for transadmittance-mode.

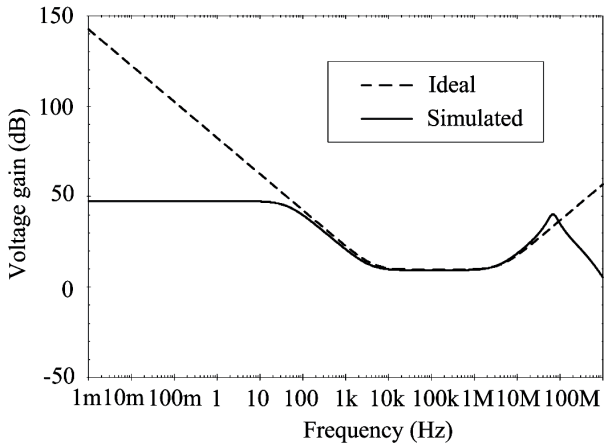

Fig. 11. Frequency responses of the proposed mixed-mode PID controller for voltage-mode.

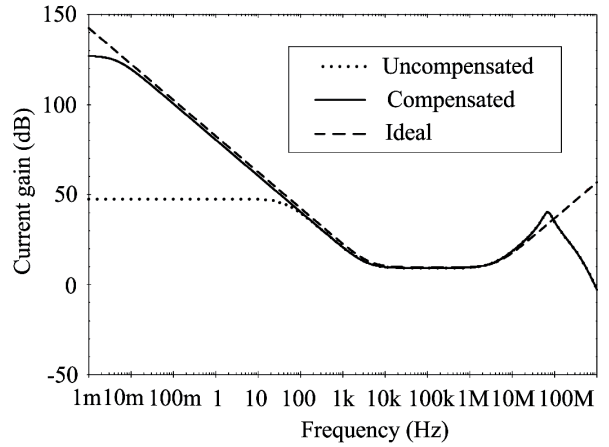

Fig. 12. Ideal, uncompensated, and compensated frequency responses of the proposed PID controller for current-mode.

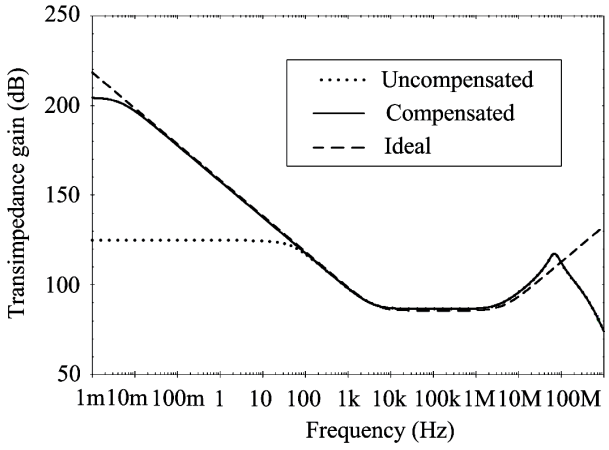

Fig. 13. Ideal, uncompensated, and compensated frequency responses of the proposed PID controller for transimpedance-mode.

It is noted that the simulated frequency responses of the compensated PID controller agree well with the ideal one from 6 mHz to 40 MHz (more than 9 decades). Consequently, the compensated PID controller exhibits better performance than the uncompensated one.

In Fig. 14 to Fig. 16, the electronic tuning feature of the proposed mixed-mode PID controller is demonstrated. The passive components of the PID controller are selected as C_1 = 20 nF and C_2 = 0.02 nF. Fig. 14 shows the proportional gain K_{PI} as in (14) versus varying bias current I_{B1} from 10 µA to 500 µA when other currents are preferred as $I_{B2} = I_{B6}$ = 18 µA and $I_{B3} = I_{B4} = I_{B5}$ = 200 µA. Fig. 15 shows the integral time constant as in (18) versus bias current I_{B3} from 10 µA to 500 µA as other currents are selected as I_{B1} = 162 µA, I_{B2} = 18 µA, $I_{B4} = I_{B5}$ = 200 µA, and I_{B6} = 18 µA. While using I_{B1} = 162 µA, I_{B2} = 18 µA, $I_{B3} = I_{B5}$ = 200 µA, and I_{B6} = 18 µA, the derivative time constant as in (19) versus bias current I_{B4} from 10 µA to 500 µA is shown in Fig. 16. It is noted that the parameters of the proposed PID controller can be electronically adjusted by control the bias currents of the transconductors.

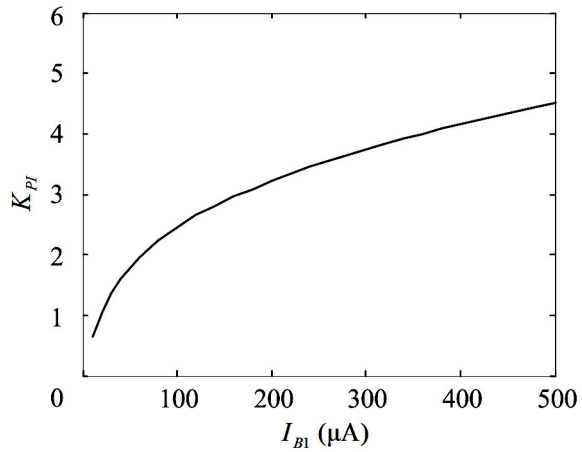

Fig. 14. Proportional gain K_{PI} of the proposed PID controller versus bias current I_{B1}.

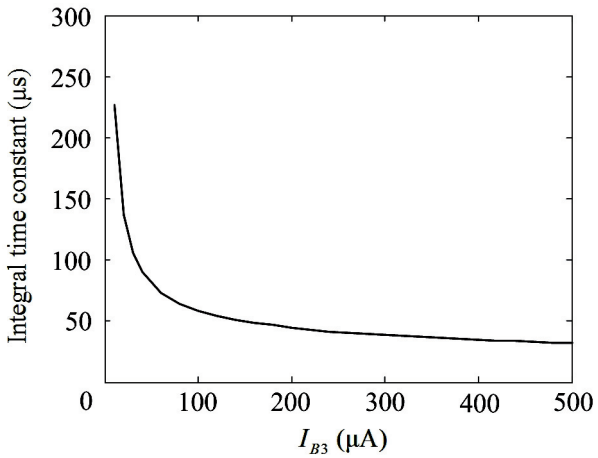

Fig. 15. Integral time constant of the proposed PID controller versus bias current I_{B3}.

In order to show the time-domain performance of the proposed PID controller, its components are set as follows: $C_1 = C_2$ = 0.1 nF, $I_{B2} = I_{B6}$ == 18 µA, $I_{B3} = I_{B4}$ = 200 µA, I_{B5} = 20 µA, and I_{B1} = 25 µA, 50 µA, and 100 µA to realize the integral time constant and the derivative time constant parameters of 0.18 µs and the proportional gain parameters

of K_{PI} = 1.19, 1.69, 2.44, and K_{PZ} = 7.44 kV/A, 10.56 kV/A, 15.25 kV/A, respectively. For examples, the simulated step responses of the proposed PID controller for current-mode and transimpedance-mode using 1 µA step input with 10 ns rise time are shown in Fig. 17 and Fig. 18.

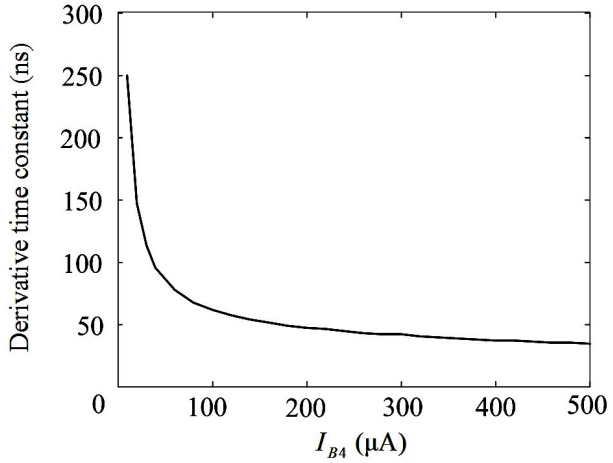

Fig. 16. Derivative time constant of the proposed PID controller versus bias current I_{B4}.

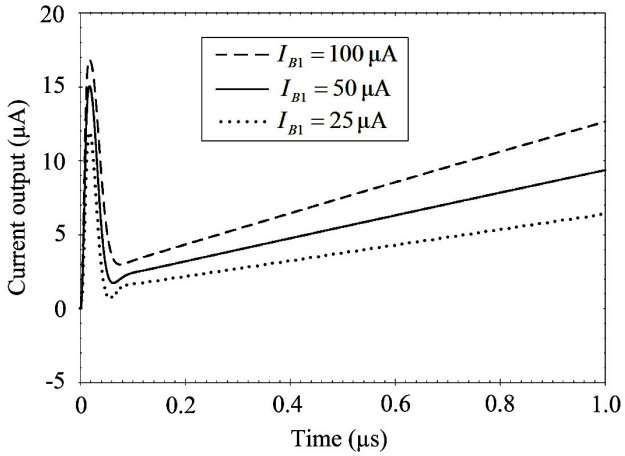

Fig. 17. Step responses of the proposed mixed-mode PID controller for current-mode.

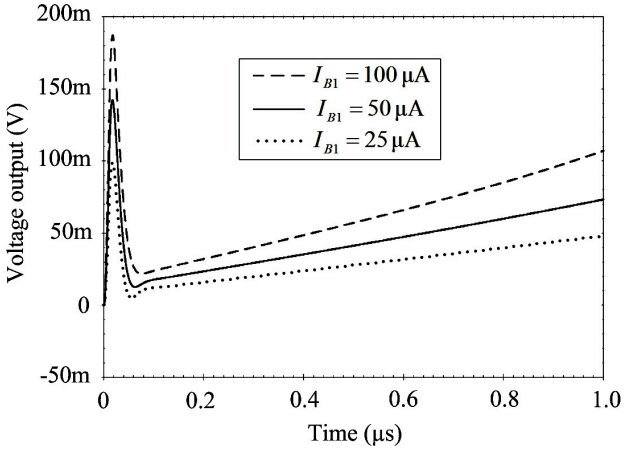

Fig. 18. Step responses of the proposed mixed-mode PID controller for transimpedance-mode.

In the closed-loop systems of Fig. 6 and Fig. 7, the current-mode low-pass filter is designed as C_{x1} = 0.3 nF, C_{x2} = 0.3 nF, and $I_{Bx1} = I_{Bx2} = I_{Bx3}$ = 100 µA and the low-pass filter of Fig. 7 is selected as C_{y1} = 0.3 nF, C_{y2} = 0.3 nF, I_{By1} = 18 µA, and $I_{By2} = I_{By3} = I_{By4}$ = 100 µA. From these plant components, the calculation of the PID parameters using Ziegler-Nichols tuning method [7] yields the proportional gains of K_{PI} = 3 and K_{PZ} = 18.75 kV/A, the integral time constant of 2.55 µs and the derivative time constant of 0.48 µs. Then, the proposed PID controller components are chosen as follows: C_1 = 1 nF, C_2 = 0.1 nF, I_{B1} = 162 µA, $I_{B2} = I_{B6}$ = 18 µA, I_{B3} = 100 µA, I_{B4} = 30 µA, and I_{B5} = 200 µA. The step responses of those closed-loop systems are tested on 7 µA step input as setpoint. The results of the systems are shown in Fig. 19 and Fig. 20.

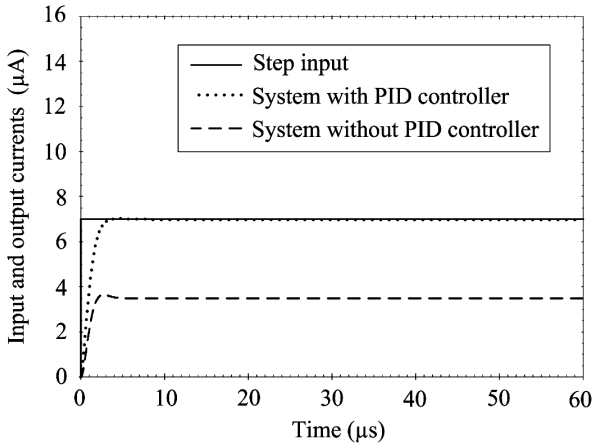

Fig. 19. Step input and outputs of the system in Fig. 6.

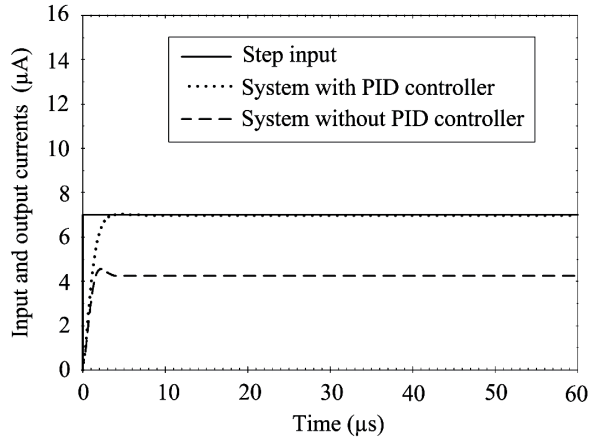

Fig. 20. Step input and outputs of the system in Fig. 7.

From those figures, the step response of the system of Fig. 6 without PID controller (node *S* and node *T* are shorted together) has the steady state error of 3.5 µA and the overshoot of 4 % and the step response of the system of Fig. 7 without PID controller (current-to-voltage converter with gain of 11.2 kV/A is used) has the steady state error of 2.4 µA and the overshoot of 6.8 % while the step responses of those systems with the proposed PID controller have the steady state error of 0.04 µA and the overshoot of 1 %.

Ref.	Components	grounded capacitors	External resistors	Electronic tuning	Operating mode	Operating Frequency range (Hz)	Supply voltage (V)
[8]	4 CCII+s 4 buffers 8 resistors 2 capacitors	No	Yes	No	Voltage	Not specified	±12
[9] Fig. 2	3 CCII+s 4 resistors 2 capacitors	Yes	Yes	No	Current	Not specified	Not specified
[9] Fig. 3	3 CCII+s 4 resistors 2 capacitors	Yes	Yes	No	Voltage	Not specified	Not specified
[10] Fig. 2	1 CCII+ 1 DO-CCII+ (22 MOS's) 3 resistors 2 capacitors	Yes	Yes	No	Voltage	Not specified	±1.5
[10] Fig. 3	1 CCII+ 1 DO-CCII+ (22 MOS's) 3 resistors 2 capacitors	Yes	Yes	No	Current	Not specified	±1.5
[11]	1 DO-CCII 1 DO-CCII- (32 MOS's) 2 resistors 2 capacitors	Yes	Yes	No	Current	Not specified	±1
[12]	4 CDBAs (80 MOS's) 8 resistors 2 capacitors	No	Yes	No	Voltage	Not specified	Not specified
[13]	8 CCCIIs (112 BJT's) 2 resistors 2 capacitors	Yes	Yes	Yes	Voltage	10 – 1M	Not specified
[14]	8 OTAs (72 MOS's) 2 capacitors	Yes	No	Yes	Voltage	Not specified	±5.0
Proposed PID controller	6 Transconductors (24 MOS's), 2 capacitors	Yes	No	Yes	Mixed	40 – 40M	±0.9

Tab. 1. Comparison of the proposed PID controller with several previous circuits.

It is obvious that the proposed PID controller can improve the steady state error and the overshoot of the closed-loop systems. A comparison of the proposed PID controller and several previous PID controllers is summarized in Tab. 1.

5. Conclusion

In this paper, a circuit configuration for realizing a mixed-mode PID controller has been presented. The proposed PID controller consists of six transconductors and only two grounded capacitors without needing any external passive resistor. It also offers the following features: mixed-mode operation without changing its topology, electronic controllability of its parameters, and low sensitivity performance. Since the compensated transconductor is used, the low-frequency performance of the proposed PID controller can be improved. The application examples of the proposed controller as two closed-loop systems are included. The results of PSPICE simulation agree well with the theoretical predictions. The uncompensated and compensated mixed-mode PID controllers have the operating frequency ranges of 40 Hz to 40 MHz and 6 mHz to 40 MHz, respectively.

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