

# Digitally Programmable High-Q Voltage-Mode Universal Filter

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**Abstract.** A new low-voltage low-power CMOS current feedback amplifier (CFA) is presented in this paper. This is used to realize a novel digitally programmable CFA (DPCFA) using transistor arrays and MOS switches. The proposed realizations nearly allow rail-to-rail swing capability at all the ports. Class-AB output stage ensures low power dissipation and high current drive capability. The proposed CFA/ DPCFA operate at supply voltage of  $\pm 0.75$  V and exhibit bandwidth better than 95 MHz. An application of the DPCFA to realize a novel voltage mode high-Q digitally programmable universal filter (UF) is given. Performances of all the proposed circuits are verified by PSPICE simulation using TSMC 0.25 $\mu$ m technology parameters.

## Keywords

Digitally programmable, universal filter, voltage mode, CFA, Q-factor.

## 1. Introduction

Programmable characteristic of analog block is an essential tool that is widely used in several applications. Analog or digital programming/tuning is employed to control the undesired parameter variation caused by temperature and process [1-14]. A common approach used for analog tuning is based on the control of parasitic resistance ( $R_x$ ) of current controlled CFA [1] and second generation current conveyor (CCII) through adjustable bias current [2]. But  $R_x$  is inherently nonlinear hence, limits the linearity. Additional disadvantage of this approach is the proportional dependence of  $R_x$  over thermal voltage, if the employed cell is implemented using BJT technology. Although analog programming is used in number of applications but the limitation on the allowable range of analog tuning voltage makes it inconvenient for low-voltage applications. Hence, in these applications, the digital control is more attractive [3-7]. Digital programming technique not only provides better accuracy in avoiding parameter race [14] but also offers additional advantages such as better noise immunity, power saving option [8] and most impor-

tantly the compatibility to modern mixed mode systems (analog/digital). Today's modern communication systems perform the signal processing mostly in digital domain. Hence, the digitally controlled analog modules are directly compatible with these systems. For example common application required in present wireless system includes channel select filter and variable gain amplifier (VGA), which are required to be digitally controlled [3-5].

Almost all the digital control techniques employ active or passive current division/summing networks (CDN) [3-13]. CDN structure consists of n-current division cells (CDC) for n-bit control. Number of CDN structure reported so far generally requires large number of transistors with additional constraint of transistor matching which makes the design complicated and area inefficient especially as the number of bits increases. CDN employed in [5], [13] is based on passive R-2R ladder technique which is not area efficient and also suffers from low output impedance. CDN structure of [3], [4] consists of n-NMOS and n-PMOS CDCs with each cell having five matched transistors for [3] and seven matched transistors for [4]. Whereas, CDCs of [9] and [10] requires eight and twelve matched transistors respectively. Although all these CDNs [3], [4], [9], [10] offer high output impedance but suffer from common drawback of using large number of matched transistors. Additional limitation of CDN structure of [4] is standby power consumption and that of [3], [9] is ability to be driven in single direction of input current. Another popular technique of digital control is based on the current division principle introduced in [15]. The current division is inherently linear and independent of MOS operating regions. CDN structure based on it is similar to R-2R ladder and requires rather lesser number of transistors but it suffers from the similar drawback of R-2R ladder i.e. low output impedance. This CDN requires  $(4n+2)$  matched transistors for n-bit control [6], [8], [12].

The digital control module used in the proposed DPCFA is analogous to the binary weighted resistor structure. It requires lesser number of transistors and also offers high output impedance [7]. An n-bit control requires only  $(4n-2)$  additional transistors in the main circuit.

Because of the higher speed, higher slew rate, simpler circuit realization, lesser component count and most im-

portantly the independence of gain and bandwidth; current feedback amplifier (CFA) has become most promising candidate for analog signal processing [1], [16-19]. Obviously if this block is equipped with the additional feature of digital control, it may find many more application in the field of mixed mode VLSI (analog/digital) systems. Thus the incorporation of digital control module in CFA not only makes the DPCFA suitable for integration but also increases its universality while preserving its simpler structure. The CFA, shown in symbolic form in Fig. 1, is a four-port network which has a describing matrix of the following form

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_Z \end{bmatrix} \quad (1)$$

Port X voltage follows port Y voltage which is independent of current injected at port X. Port Z current follows port X current. Output buffer provides voltage following action between port W and Z.

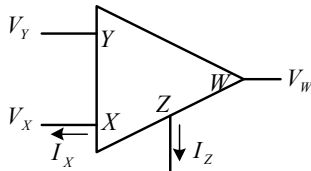


Fig. 1. Symbol of CFA.

In this paper, a new CFA derived from the low-voltage low-power CCII+ [7] is introduced. This in turn is used to realize the novel DPCFA. Both CFA/DPCFA operates at supply voltage of  $\pm 0.75$  V and nearly allows rail-to-rail voltage operation at all the ports. Class-AB output stage ensures low power dissipation and high current driving capability.

The proposed DPCFA is used to realize a novel digitally programmable four-input single-output high-Q second-order UF. It is capable of generating all the standard filter functions, namely lowpass (LP), highpass (HP), bandpass (BP), band reject (BR) and allpass (AP). All the filter parameters, namely pole frequency ( $\omega_0$ ), quality factor (Q) and gain (G) are independently programmable. The proposed UF uses four DPCFA, two digitally programmable CCIIs (DPCFAs), two grounded capacitors and few resistors. Use of only grounded capacitor makes it suitable for monolithic integration [20]. The performance and the validity of theoretical results are verified by PSPICE simulations.

This paper is organized as follows. Starting from the Introduction, Section 2 illustrates detailed description of the proposed CFA and DPCFA, Section 3 presents the realization of the proposed UF, Section 4 discusses the non-idealities and Section 5 deals with PSPICE simulation of all the proposed circuits. Finally, conclusion is drawn in Section 6.

## 2. Proposed CFA/DPCFA

The CFAs are typically built by cascading a positive current conveyor (CCII+) with a suitable voltage buffer (VB) [17], [18]. CFA realization as depicted in Fig. 2 is obtained by cascading a VB (M1a-M12a) at port Z of CCII+ [7]. VB used is the replica of buffer circuit between port X and Y of CCII+. All the transistors are assumed to be operating in saturation. Transistor M9 and M10 provide the necessary biasing current to matched PMOS (M5, M6) and matched NMOS differential pair (M1, M2) separately. The two differential pairs operate in complementary fashion and ensure rail to rail operation. Ideally for positive voltage at port Y, only NMOS pair operates and for negative voltage, only PMOS pair operates. Differential pairs perform the voltage buffering action between port Y and X. Current mirroring for these NMOS and PMOS pairs are provided by two matched current mirror pairs (M3, M4) and (M7, M8) respectively. Current following action between port X and Z is performed by either matched pair (M11, M13) or (M12, M14) depending on the input condition. Class AB push-pull output stage comprising M11-M12 provides current swing up to  $\pm 1$  mA and standby power dissipation of  $220 \mu\text{W}$ . Minimum ( $V_t + 3V_{DSsat}$ ) supply voltage is required for proper operation of circuit while class AB transistors requires ( $2V_{DSsat}$ ) voltage only.

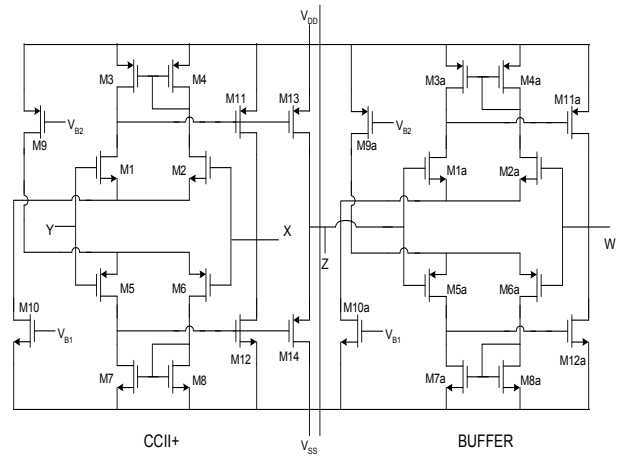


Fig. 2. CMOS implementation of CFA from CCII+ and VB.

Small signal voltage gain between port X and Y is given as

$$\frac{V_X}{V_Y} = \frac{g_{m1} + g_{m5} \frac{g_{m12}}{g_{m11}}}{g_{m2} + g_{m6} \frac{g_{m12}}{g_{m11}}} \quad (2)$$

Parameter  $g_{mi}$ , denotes the transconductance of the  $i^{\text{th}}$  transistor. It is evident from (2), that if both the differential pairs are separately matched ( $g_{m1} = g_{m2}$ ,  $g_{m5} = g_{m6}$ ), voltage gain is unity.

Assuming load at port X and Z to be negligible as compared to  $r_{oi}$  of MOS, current gain is given by

$$\frac{I_Z}{I_X} \approx \frac{g_{m11}}{g_{m13}} \approx \frac{g_{m12}}{g_{m14}}. \quad (3)$$

Obviously, unity current gain requires matched transistor set (M11, M13) and (M12, M14).

Port X and W impedance, for ( $g_{m2} = g_{m6} = g_m$ ,  $g_{m1} = g_{m5}$ ,  $r_{o1}/r_{o3} = r_{o5}/r_{o9} = r_o/2$ ) is given as

$$R_X = \frac{2}{r_o g_m (g_{m11} + g_{m12})} = R_W. \quad (4)$$

Port Z parasitic impedance is given as

$$Z_Z = \frac{r_{o13} r_{o14}}{r_{o13} + r_{o14}}. \quad (5)$$

The proposed CFA offers high impedance at port Z (1.13 M $\Omega$ ). This is useful for better high frequency response of circuit [18]. Obtained gain values of current and voltage transfer are close to unity. Apart from this the proposed CFA exhibits good temperature independence and offers reasonably better values of slew rate and settling time.

Digital programmability feature is incorporated in CFA by replacing the transistors of port X or Z by a current summing network (CSN) consisting n-transistor arrays associated with MOS switches. It modifies the current transfer ratio between port X and Z as

$$I_Z = K^m I_X \quad (6)$$

where  $K$  denotes the  $n$ -bit digital codeword given by

$$K = \sum_{j=0}^{n-1} a_j 2^j \quad (7)$$

where  $a_j$  is the digital code bit applied to the  $j^{\text{th}}$  array of CSN (described in subsequent subsection). Power integer  $m = \pm 1$  results in the two variant of DPCFA. The value of  $m = +1$  denotes the DPCFAK<sup>+</sup> block having CSN at port Z and current gain greater than or equal to unity ( $K^+$ ), while  $m = -1$  denotes the DPCFAK<sup>-</sup> block having CSN at port X and current gain less than or equal to unity ( $K^-$ ). Thus DPCFA may be represented as a five port block as shown in Fig. 3a, having digitally controlled current gain  $K^\pm$  between port X and Z through  $n$ -bit codeword ( $K$ ), while all other characteristics are same as that of conventional CFA. For ease of representation the block diagram of DPCFA of Fig. 3a is modified, as shown in Fig. 3b and will be used throughout the paper. It shows the  $i^{\text{th}}$  DPCFA block with gain  $K^+$  or  $K^-$  and applied codeword  $K_i$ .

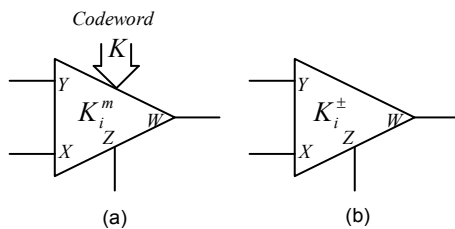


Fig. 3. (a) Symbol of DPCFA. (b) Modified symbol.

## 2.1 DPCFA with Gain $K^+$ (DPCFAK<sup>+</sup>)

CMOS implementation of 3-bit DPCFAK<sup>+</sup> is shown in Fig. 4. Port Z transistor M13-M14 of Fig. 2 is replaced by three ( $n=3$ ) arrays CSN comprised of transistors M13-M24. Each  $j^{\text{th}}$  array of CSN consists of PMOS ( $jP$ ) and NMOS ( $jN$ ) transistor pair having aspect ratio set in binary weighted order and is given as

$$\left(\frac{W}{L}\right)_{jP(\text{or } jN)} = 2^j \left(\frac{W}{L}\right)_{P(\text{or } N)} \quad j = 0, 1, \dots, n-1 \quad (8)$$

where P (N) denotes the PMOS (NMOS) transistor M11 (M12).

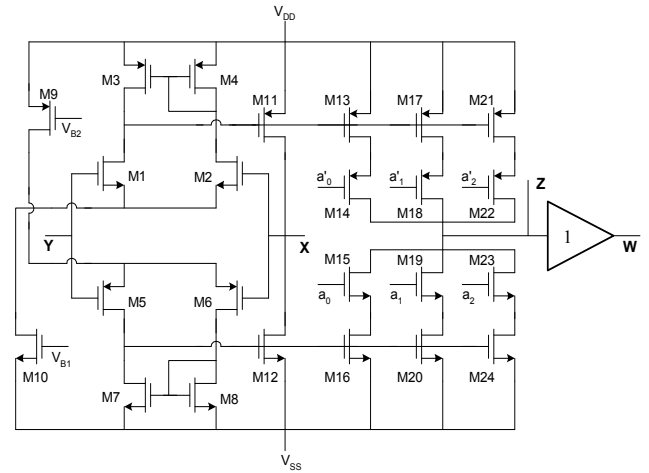


Fig. 4. DPCFAK<sup>+</sup> with gain  $K^+$ .

Thus, each array of CSN amplifies the port X current as per the weight (aspect ratio) assigned to them. Thus, port Z current, if flowing out of DPCFAK<sup>+</sup>, is given by

$$I_Z = \sum_{j=0}^{n-1} a_j 2^j (I_{M11} - I_{M12})$$

whereas port X current is given by

$$I_X = (I_{M11} - I_{M12}).$$

Hence, the current gain is given as

$$\frac{I_Z}{I_X} = \sum_{j=0}^{n-1} a_j 2^j = K = K^+. \quad (9)$$

It can be seen from (9) that current gain ( $K^+$ ) is programmable by codeword  $K$  and may have any value ranging from 1 to  $(2^n - 1)$  for  $n$ -array DPCFAK<sup>+</sup>.

## 2.2 DPCFA with Gain $K^-$ (DPCFAK<sup>-</sup>)

Following the similar approach, 3-bit DPCFAK<sup>-</sup> (Fig. 5) can be implemented by replacing port X transistors M11-M12 of Fig. 2 by same CSN as mentioned above. But in this case no current amplification is involved at port Z rather it is just equal to the smallest current of CSN flowing in the active array having least weight. Port X current, if flowing out of DPCFAK<sup>-</sup> is given as:

$$I_X = \sum_{j=0}^{n-1} a_j 2^j (I_{M11} - I_{M12})$$

whereas the port Z current is given as

$$I_Z = (I_{M11} - I_{M12}) .$$

Thus the current gain is given by

$$\frac{I_Z}{I_X} = \frac{1}{\sum_{j=0}^{n-1} a_j 2^j} = \frac{1}{K} = K^- . \tag{10}$$

It is again clear from (10) that current gain ( $K^-$ ) is programmable by codeword  $K$  and may have any value ranging from 1 to  $1/(2^n - 1)$  for  $n$ -array DPCFAK<sup>-</sup>.

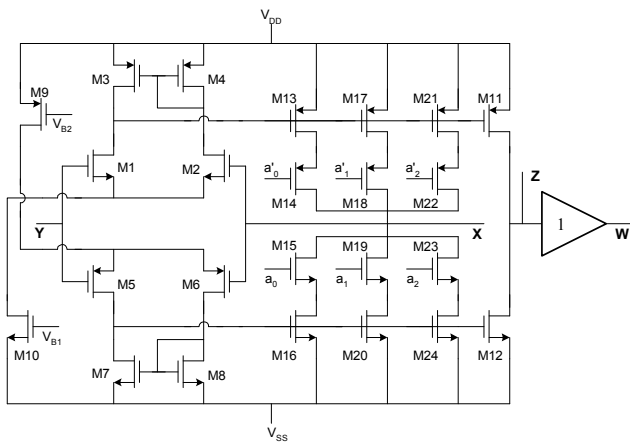


Fig. 5. DPCFAK<sup>-</sup> with gain  $K^-$ .

### 3. Proposed Universal Filter

The DPCFA discussed in the previous section is utilized for the realization of voltage mode digitally programmable four-input single-output second-order UF (Fig. 6). It uses three DPCFAK<sup>+</sup>, one DPCFAK<sup>-</sup>, two DPCCIIK<sup>-</sup>, two grounded capacitors and few resistors. DPCCIIK<sup>-</sup> may be thought of as DPCFAK<sup>-</sup> with buffer removed from port Z. Versatility of UF may be described by following desirable features:

- All the inputs are applied at high impedance ports (Y) and outputs are generated at low impedance port (W). This enables easy cascading for higher order filter realization without requiring any buffer stage.
- No constraint such as input inversion is required for various filter function realization.
- All the filter parameters ( $\omega_0$ ,  $Q$  and gain) are independently digitally programmable.
- High-Q realization for BP and BR.
- Only single circuit is used for programming all the filter functions.

In addition to this, use of only two grounded capacitor makes the proposed UF suitable for monolithic integration. A detailed comparison of the proposed UF with similar reported filters is given in next Section 5.

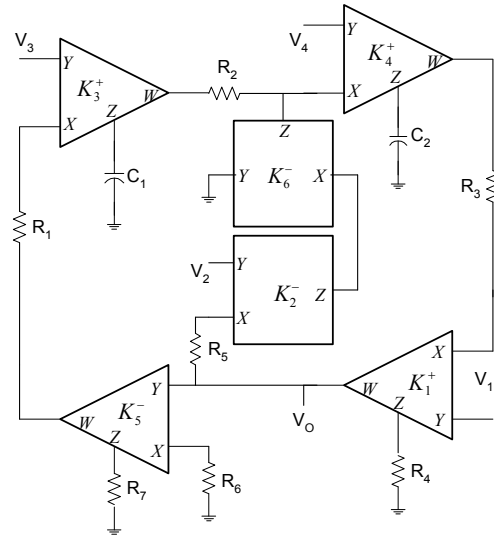


Fig. 6. The proposed UF using DPCFA and DPCCII.

Routine analysis yields the following output function:

$$V_0 = \frac{N(s)}{D(s)} \tag{11}$$

where the numerator and denominator functions are given as

$$N(s) = s^2 K_1 \frac{R_4}{R_3} V_1 + s \frac{K_1 K_4 R_4}{K_2 K_6 C_2 R_3 R_5} V_2 - s \frac{K_1 K_4 R_4}{C_2 R_2 R_3} V_4 + \frac{K_1 K_3 K_4 R_4}{C_1 C_2 R_1 R_2 R_3} V_3 \tag{12a}$$

$$D(s) = s^2 + s \frac{K_1 K_4 R_4}{K_2 K_6 C_2 R_3 R_5} + \frac{K_1 K_3 K_4 R_4 R_7}{K_5 C_1 C_2 R_1 R_2 R_3 R_6} . \tag{12b}$$

All the programming method described in this paper requires common codeword constraint,  $K_3 = K_4$  and  $K_1 = K_5$ , using this (12) reduces to:

$$N(s) = s^2 K_1 \frac{R_4}{R_3} V_1 + s \frac{K_1 K_3 R_4}{K_2 K_6 C_2 R_3 R_5} V_2 - s \frac{K_1 K_3 R_4}{C_2 R_2 R_3} V_4 + \frac{K_1 K_3^2 R_4}{C_1 C_2 R_1 R_2 R_3} V_3 \tag{13a}$$

$$D(s) = s^2 + s \frac{K_1 K_3 R_4}{K_2 K_6 C_2 R_3 R_5} + \frac{K_3^2 R_4 R_7}{C_1 C_2 R_1 R_2 R_3 R_6} . \tag{13b}$$

From (13), it can be seen that all the standard filter functions including two variants of BP, namely inverting BP (BPI) and non-inverting BP (BPN) can be generated by proper input combination as shown in Tab. 1. Only AP and BR response requires component matching constraint.

All the filter functions except BPNI have digitally programmable gain parameters.

Input Set	Filter Function	Gain (G) (V <sub>o</sub> /V <sub>i</sub> )	Constraint
V <sub>2</sub> =V <sub>3</sub> =V <sub>4</sub> =0, V <sub>1</sub> =V <sub>i</sub> *	HP	(K <sub>1</sub> R <sub>4</sub> )/R <sub>3</sub>	NO
V <sub>1</sub> =V <sub>2</sub> =V <sub>4</sub> =0, V <sub>3</sub> =V <sub>i</sub>	LP	(K <sub>1</sub> R <sub>6</sub> )/R <sub>7</sub>	NO
V <sub>1</sub> =V <sub>3</sub> =V <sub>4</sub> =0, V <sub>2</sub> =V <sub>i</sub>	BPNI	1	NO
V <sub>1</sub> =V <sub>2</sub> =V <sub>3</sub> =0, V <sub>4</sub> =V <sub>i</sub>	BPI	- (K <sub>2</sub> K <sub>6</sub> R <sub>5</sub> )/R <sub>2</sub>	NO
V <sub>2</sub> =V <sub>4</sub> =0, V <sub>1</sub> =V <sub>3</sub> =V <sub>i</sub>	BR	K <sub>1</sub>	R <sub>4</sub> /R <sub>3</sub> =R <sub>7</sub> /R <sub>6</sub> =1
V <sub>2</sub> =0, V <sub>1</sub> =V <sub>3</sub> =V <sub>4</sub> =V <sub>i</sub>	AP	K <sub>1</sub>	R <sub>4</sub> /R <sub>3</sub> =R <sub>7</sub> /R <sub>6</sub> =1 R <sub>2</sub> =R <sub>5</sub> , K <sub>1</sub> =K <sub>6</sub> , K <sub>2</sub> =1

\*V<sub>i</sub> denotes the actual applicable input.

**Tab. 1.** Filter functions of UF.

From (13b) the pole frequency ( $\omega_0$ ) and quality factor ( $Q$ ) can be expressed as:

$$\omega_0 = \left[ \frac{R_4 R_7}{C_1 C_2 R_1 R_2 R_3 R_6} \right]^{1/2} [K_3], \quad (14a)$$

$$Q = R_5 \left[ \frac{C_2 R_3 R_7}{C_1 R_1 R_2 R_4 R_6} \right]^{1/2} \left[ \frac{K_2 K_6}{K_1} \right]. \quad (14b)$$

For  $C_1 = 2C_2$  and equal resistor values, (14) reduces to

$$\omega_0 = \frac{1}{\sqrt{2}CR} [K_3] = \omega_c [K_3], \quad (15a)$$

$$Q = \left[ \frac{1}{\sqrt{2}} \right] \left[ \frac{K_2 K_6}{K_1} \right] = Q_c \left[ \frac{K_2 K_6}{K_1} \right]. \quad (15b)$$

With gain parameter given as:

$$G|_{BPNI} = 1, \quad (15c)$$

$$G|_{LP,HP,BR,AP} = [G_c][K_1], \quad (15d)$$

$$G|_{BPI} = [G_c][K_2 K_6] \quad (15e)$$

where  $\omega_c$ ,  $Q_c$  and  $G_c$  are defined as component dependent factor of pole frequency, quality factor and gain respectively and are given as:

$$\omega_c = \frac{1}{\sqrt{2}CR}, \quad (16a)$$

$$Q_c = \frac{1}{\sqrt{2}}, \quad (16b)$$

$$G_c = 1. \quad (16c)$$

Setting capacitance value  $C_1 = 2C_2$ ; results quality factor of value  $1/\sqrt{2}$  as given by (16b). It is required for maximal flat LP and HP response. Moreover, the condition of equal resistance values also satisfies the component matching constraints of BR and AP. Thus, (15), (16) effectively characterize all the responses of UF.

First set of programming requires  $K_1 = K_6$ , which modifies (15) as:

$$\omega_0 = \omega_c K_3, \quad (17a)$$

$$Q = Q_c K_2, \quad (17b)$$

$$G|_{BPNI} = 1, \quad (17c)$$

$$G|_{LP,HP,BR,AP} = [G_c][K_1], \quad (17d)$$

$$G|_{BPI} = [G_c][K_1 K_2]. \quad (17e)$$

From (17a-d), it can be seen that  $\omega_0$ , Q-factor and gain of all the filter functions except BPI are programmable independently through codeword  $K_3 (=K_4)$ ,  $K_2$  and  $K_1 (=K_5=K_6)$  respectively. Although the programming of (17) equally applies to BPI but it requires a rather different approach. First, the desired value of Q-factor is set by  $K_2$  then gain is programmed by  $K_1$ . Pole frequency is programmed in similar way through  $K_3$ . Thus by adopting programming method of (17), all the filter functions are fully programmable.

Although equation (17) governs the complete programming of UF but it does not provide  $Q$  values more than  $7Q_c$ , which is mainly required from BR and BP responses. A different codeword programming as described below not only realizes high-Q for both BP and BR but also provides additional flexibility in programming of BP combination (BPI and BPNI).

Defining new codeword programming by setting  $K_1 = 1$ , (15) reduces to:

$$\omega_0 = \omega_c K_3, \quad (18a)$$

$$Q = Q_c K_2 K_6, \quad (18b)$$

$$G|_{BPNI} = 1, \quad (18c)$$

$$G|_{LP,HP,BR,AP} = [G_c], \quad (18d)$$

$$G|_{BPI} = [G_c][K_2 K_6]. \quad (18e)$$

Following (18b-d), high Q realization for BPNI and BR can be achieved through product ( $K_2 K_6$ ) but at the cost of constant gain. Thus the Q-value ranging from  $Q_c$  to maximum  $49Q_c$  in step of one is realizable using (18b). Quality factor value higher than  $49Q_c$  can be obtained by introducing additional transistor arrays in CSN of blocks  $K_2$  or  $K_6$ . As evident from (7), the addition of only one transistor array in either of block results  $Q$  factor upto  $105Q_c (15 \times 7)$ .

For realizing high gain as well as high-Q, BPI response is preferred and programmed using (18b,e). Again the product term ( $K_2 K_6$ ) can provide any value of gain and  $Q$  with a common multiplier factor ranging from 1 to 49. Pole frequency programming from (17a, 18a) is same in all the cases.

At this point of time, it is necessary to introduce another popular approach used for high-Q realization [21], [22]. It uses cascaded AP sections in positive feedback configuration for realizing high-Q. But the Q-values using this approach are not independent of gain [22]. Thus in this aspect, the proposed circuit is more flexible as it provides both high-Q and desired gain values simultaneously.

Thus the combined programming of (17), (18) makes the UF fully programmable and realizes high-Q as well. Simulation results for all the cases are given in Section 5.

## 4. Non-ideal Analysis

This section discusses the effect of CFA non-idealities over the performance of the proposed UF. These non-idealities result from (i) small error in unity transfer gains as described by equation (1) and (ii) CFA parasitics.

Considering the first set of non-idealities, port relation of DPCFA modifies as

$$V_X = \alpha_i V_Y, \quad (19a)$$

$$I_Z = \beta_i K_i^m I_X, \quad (19b)$$

$$V_W = \gamma_i V_Z \quad (19c)$$

where,  $\alpha_i$ ,  $\beta_i$ , and  $\gamma_i$  are non-unity transfer gains of the  $i^{\text{th}}$  block resulting from the non-idealities.

Denoting the non-idealities effects by subscript 'n', the modified output function of UF using (19) is given as

$$V_{on} = \frac{N_n(s)}{D_n(s)}. \quad (20)$$

Modified numerator and denominator functions are given as

$$N_n(s) = s^2 \alpha_1 \beta_1 \gamma_1 K_1 \frac{R_4}{R_3} V_1 + s \frac{\alpha_2 \beta_1 \beta_2 \beta_4 \beta_6 \gamma_1 \gamma_4 K_1 K_4 R_4}{K_2 K_6 C_2 R_3 R_5} V_2 - s \frac{\alpha_4 \beta_1 \beta_4 \gamma_1 \gamma_4 K_1 K_4 R_4}{C_2 R_2 R_3} V_4 + \frac{\alpha_3 \beta_1 \beta_3 \beta_4 \gamma_1 \gamma_3 \gamma_4 K_1 K_3 K_4 R_4}{C_1 C_2 R_1 R_2 R_3} V_3 \quad (21a)$$

$$D_n(s) = s^2 + s \frac{\beta_1 \beta_2 \beta_4 \beta_6 \gamma_1 \gamma_4 K_1 K_4 R_4}{K_2 K_6 C_2 R_3 R_5} + \frac{\alpha_5 \beta_1 \beta_3 \beta_4 \beta_5 \gamma_1 \gamma_3 \gamma_4 \gamma_5 K_1 K_3 K_4 R_4 R_7}{K_5 C_1 C_2 R_1 R_2 R_3 R_6} \quad (21b)$$

Modified  $\omega_0$  and  $Q$  factor using (21b) are given as

$$\omega_0 = \sqrt{\frac{\alpha_5 \beta_1 \beta_3 \beta_4 \beta_5 \gamma_1 \gamma_3 \gamma_4 \gamma_5 K_1 K_3 K_4 R_4 R_7}{K_5 C_1 C_2 R_1 R_2 R_3 R_6}}, \quad (22a)$$

$$Q = \frac{K_2 K_6 R_5}{\beta_2 \beta_6} \sqrt{\frac{\alpha_5 \beta_3 \beta_5 \gamma_3 \gamma_5 K_3 C_2 R_3 R_7}{\beta_1 \beta_4 \gamma_1 \gamma_4 K_1 K_4 K_5 C_1 R_1 R_2 R_4 R_6}}. \quad (22b)$$

Thus the active and passive sensitivities of  $\omega_0$  and  $Q$  may be summarized as

$$0 \leq |S_x^{\omega_0}| \leq \frac{1}{2}, \quad (23a)$$

$$0 \leq |S_x^Q| \leq 1 \quad (23b)$$

where 'x' denotes various active and passive elements i.e.  $\alpha_i$ ,  $\beta_i$ ,  $\gamma_i$ ,  $K_i$ , resistances and capacitances. It is evident from (23) that the sensitivity figures are within reasonable limit.

The second set of non-idealities includes DPCFA parasitics. DPCFAs have high value parasitic resistance  $R_Y$  (or  $R_Z$ ) in parallel with low value parasitic capacitance  $C_Y$  (or  $C_Z$ ) at port Y (or Z), and a low valued series resistance  $R_X$  at port X. To simplify the discussion parasitic resistances at port Y and Z are not considered as these are much greater than the external resistance of circuit. Also, the parasitics at a port is ignored if the respective port is really or virtually grounded. Under these assumptions, modified output function of UF is similar to that given by (11), (12) with component values replaced by the following modified set-  $R_{1P} = R_1 + R_{X3}$ ,  $R_{3P} = R_3 + R_{X1}$ ,  $R_{6P} = R_6 + R_{X5}$ ,  $R_{5P} = R_5 + R_{X2}$ ,  $C_{1P} = C_1 + C_{Z3}$ ,  $C_{2P} = C_2 + C_{Z4}$ ,  $R_{2P} = R_2 \parallel 1/sC_{Z6}$ ,  $R_{4P} = R_4 \parallel 1/sC_{Z4}$  and  $R_{7P} = R_7 \parallel 1/sC_{Z5}$ . Subscript 'P' denotes the modified component values under the influence of parasitics. Modification in component values reveals the fact that (1) the proposed UF is completely unaffected by the port Y parasitics, (2) number of parasitics are absorbed in external components itself; hence do not create any unwanted pole and impose any frequency limitation over filter performance. On the other hand, components  $R_{2P}$ ,  $R_{4P}$  and  $R_{7P}$  restrict the circuit operation below frequencies  $1/R_2 C_{Z6}$ ,  $1/R_4 C_{Z4}$  and  $1/R_7 C_{Z5}$  respectively. Since the port Z parasitic capacitance values are of order of few picofarads only; these frequencies are very high, which can be further increased by using low value resistance at port Z.

## 5. Simulation Result

Performance of the proposed DPCFA and UF is verified by PSPICE simulations with supply voltage  $\pm 0.75$  V using level-7, 0.25  $\mu\text{m}$  TSMC CMOS technology parameters and aspect ratios listed in Tab. 2.

MOSFET	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )
M1, M2, M5, M6	5	0.25
M3, M4, M7, M8	0.5	0.5
M9, M10	0.5	0.25
M11-M16	25	0.25
M17-M20	50	0.25
M21-M24	100	0.25

Tab. 2. Aspect Ratios of MOSFETs of DPCFA.

First of all, the performance of CFA circuit (Fig. 2) is verified. Voltage tracking action of port Y-W exhibits nearly rail-to-rail linearity range from -0.6 to 0.61 V as shown in Fig. 7.

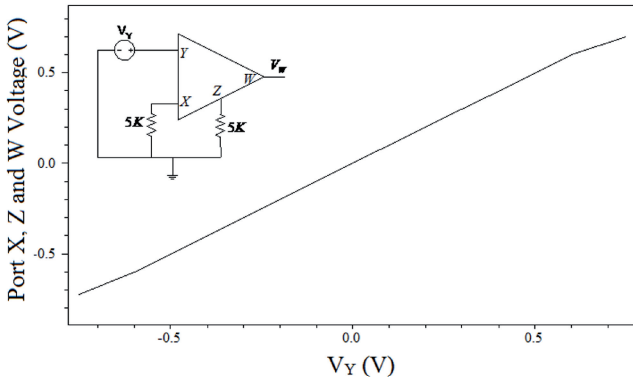


Fig. 7. Port X, Z and W voltage variation vs. port Y voltage.

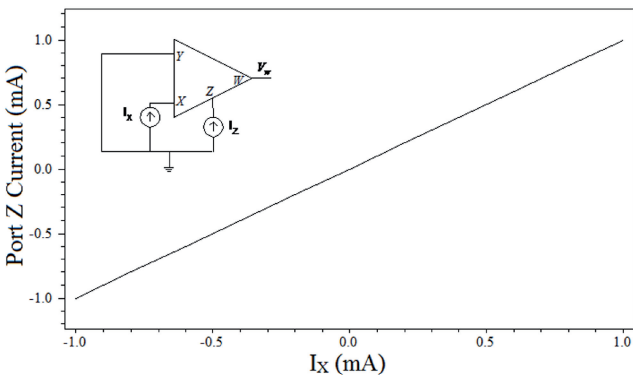


Fig. 8. Port Z current variation versus port X current.

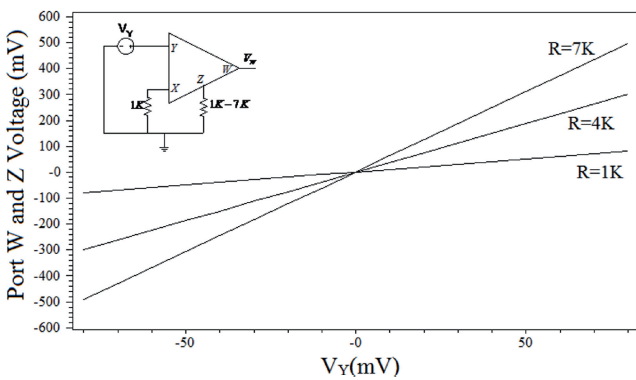


Fig. 9. Port W and Z voltage versus port Y voltage for CFA based VGA.

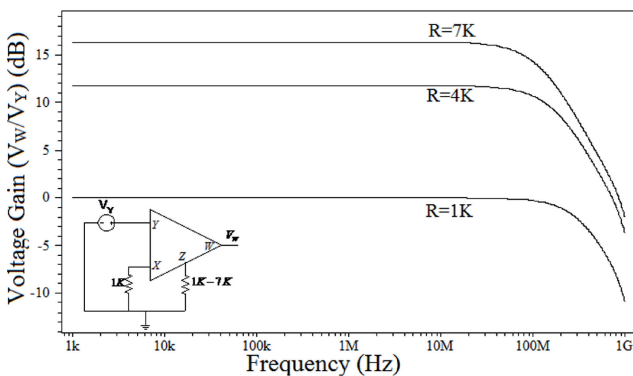


Fig. 10. Magnitude response of CFA based VGA.

Port Z current variation with respect to port X current is shown in Fig. 8. A high current drive capability of  $\pm 1$  mA is obtained.

Fig. 9 shows the output voltage swing of non-inverting CFA based VGA for gain values 1, 4 and 7. Port X is terminated with resistance 1K, while port Z resistance is scanned for values 1K, 4K and 7K. Output shows an acceptable linearity for input swing of  $\pm 80$  mV. As shown in Fig. 10, amplifier results almost constant bandwidth of 100 MHz for different gains.

Transient analysis of the unity gain CFA as depicted in Fig. 11 is performed by applying 1 MHz square wave of magnitude  $400$  mV<sub>P-P</sub> at port Y. The positive (negative) slew rate obtained is  $69$  V/ $\mu$ s ( $58$  V/ $\mu$ s). Rise time and fall time on the basis of 1% of final value is  $6.4$  ns and  $8.3$  ns respectively.

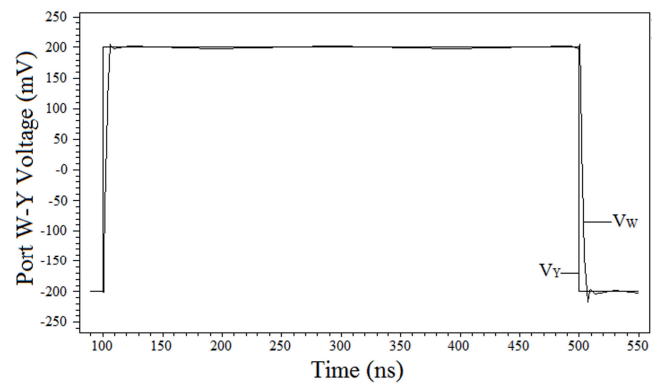


Fig. 11. Transient response of unity gain CFA.

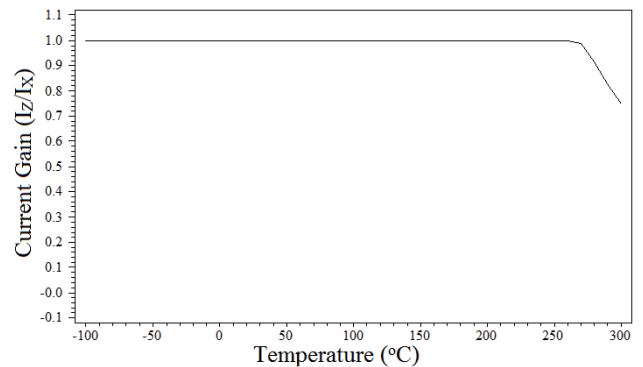


Fig. 12. Current gain variation with respect to temperature.

Ref./Parameters	CFA [16]	CFA [17]	Proposed CFA
CMOS technology ( $\mu$ m)	0.25	0.25	0.25
Power supply (V)	$\pm 0.75$	$\pm 0.75$	$\pm 0.75$
Standby power dissipation ( $\mu$ W)	NA	456	220
Standby current ( $\mu$ A)	320	304	299
Input voltage dynamic range (V)	NA	$\pm 0.65$	$\pm 0.6$
Current drive capability (mA)	NA	$\pm 1$	$\pm 1$
Bandwidth (MHz)	57-530	120	100
Slew rate (V/ $\mu$ s)	10	NA	69

Tab. 3. Performance comparison of proposed CFA.

Current gain variation with respect to temperature is shown in Fig. 12. Current gain is almost insensitive to temperature up to 250°C.

Performance comparison of the proposed CFA and the CFA reported in [16], [17] is given in Tab. 3.

In next step, the comparative performance of the two variants of 3-bit DPCFA is presented in parallel for better analysis of results. For the sake of clarity, all the simulations are performed for codeword values  $K = 1(001)$ ,  $4(100)$ ,  $7(111)$ . (Quantity written in brackets denotes the applied bit combination). Depending on the DPCFA variant used, these codewords result different values of current gain  $K^+$  and  $K^-$ .

Current transfer related to port X-Z (Fig. 13) shows an acceptable input linearity range of  $\pm 150 \mu\text{A}$ .

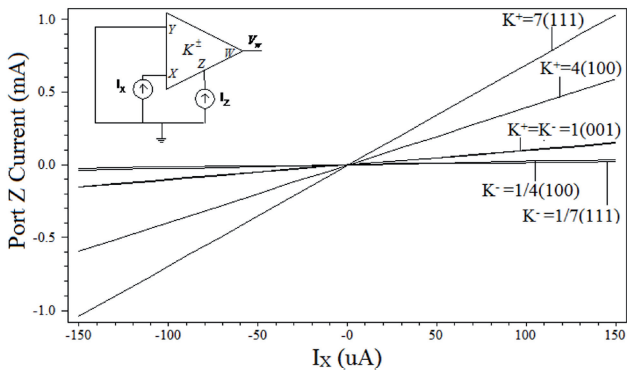


Fig. 13. Port Z current versus port X current for different gain/codewords.

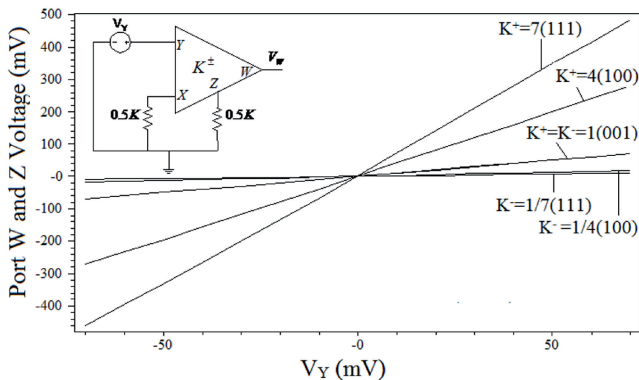


Fig. 14. Port W and Z voltage versus port Y voltage for DPCFA based VGA.

DPCFA based VGA showing the voltage amplification related to port Y-W for different gain values are depicted in Fig. 14. It shows an acceptable input linearity range of  $\pm 70 \text{ mV}$  and has almost constant bandwidth of 95 MHz as depicted in Fig. 15.

Finally, the last set of simulation is performed for the proposed UF with capacitor values  $C_1 = 2 \text{ nF}$ ,  $C_2 = 1 \text{ nF}$  and equal resistor values  $R = 2\text{K}$ . It results component dependent filter parameters as  $f_c = 1/2\sqrt{2}\pi RC = 56.27 \text{ kHz}$ ,  $Q_c = 1/\sqrt{2}$  and  $G_c = 1$ .

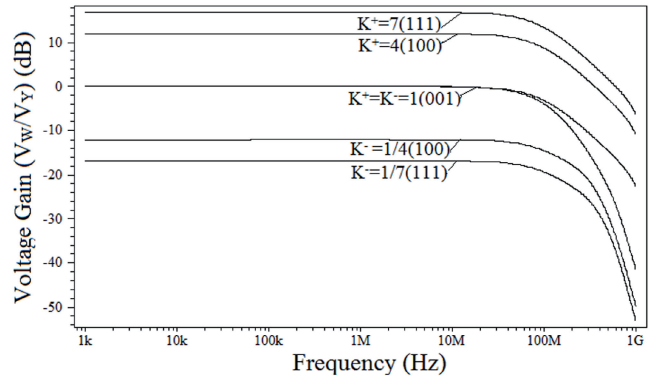


Fig. 15. Magnitude response of DPCFA based VGA.

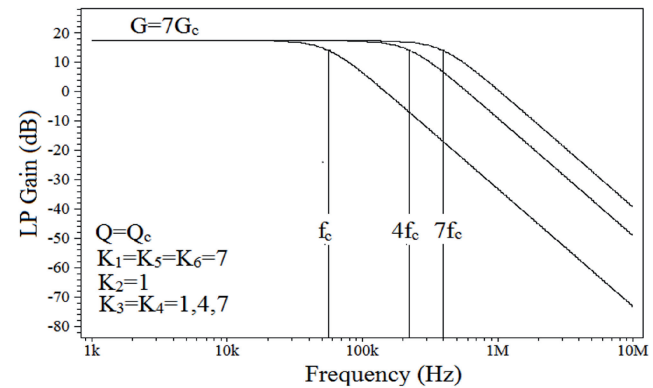


Fig. 16a. Pole frequency programming of LP filter.

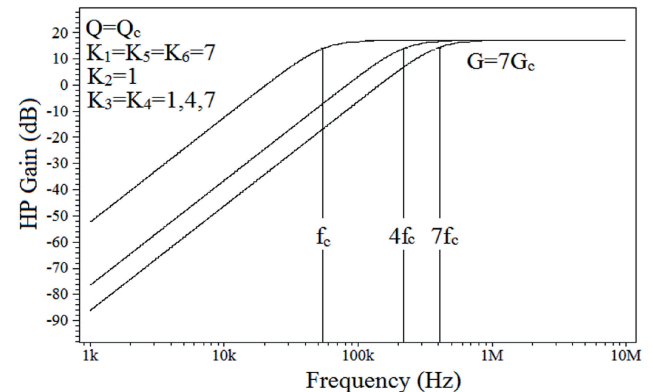


Fig. 16b. Pole frequency programming of HP filter.

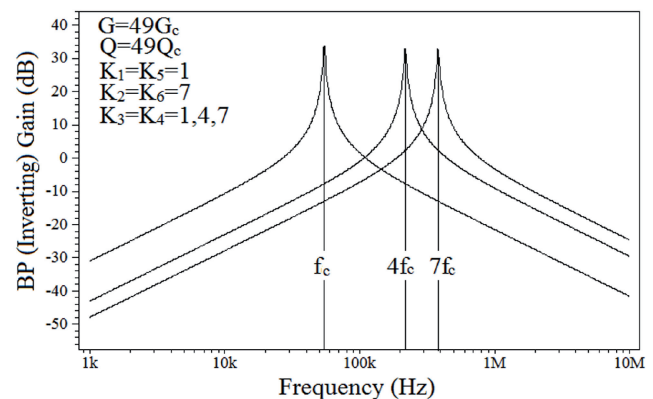


Fig. 16c. Pole frequency programming of BPI filter.



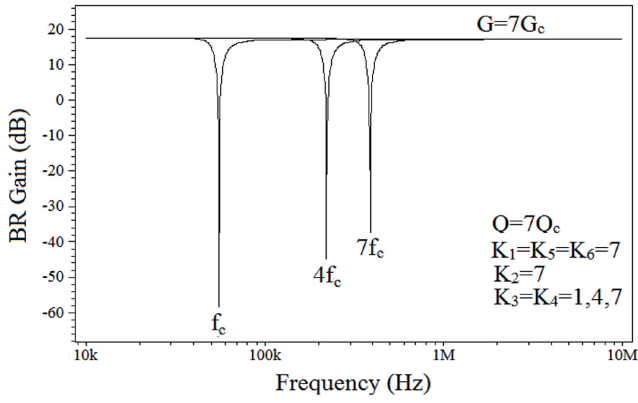


Fig. 16d. Pole frequency programming of BR filter.

As evident from (17a), (18a), pole frequency is programmed by varying  $K_3(=K_4)$ . Fig. 16 shows the  $\omega_0$  programming for various responses for different values of gain and  $Q$  factor. Parameter values and codeword programming are mentioned in figures itself. BPI programming depicted in Fig. 16c) follows the rule of (18).

As described by (17d) gain of LP, HP, BR and AP can be programmed by varying  $K_1(=K_5=K_6)$ . Fig. (17a-d) shows the same at frequency  $4f_c$ .  $Q$  values are chosen depending on the type of response. Fig. 17e shows the phase response of AP filter at frequency  $4f_c$ .

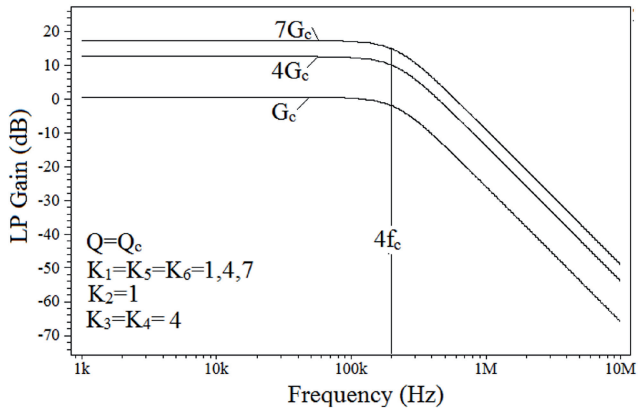


Fig. 17a. Gain programming of LP filter.

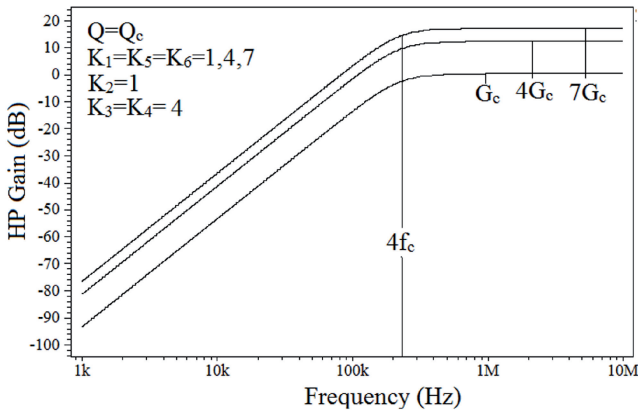


Fig. 17b. Gain programming of HP filter.

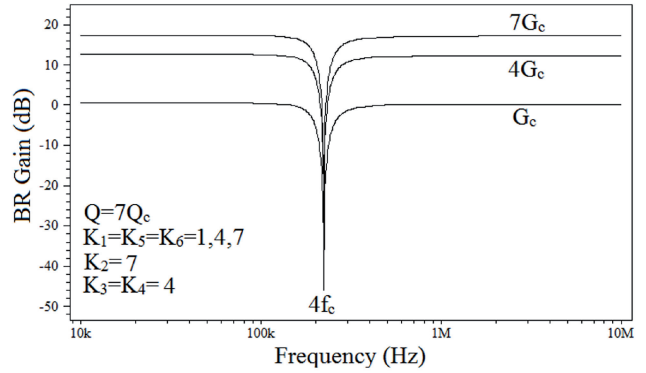


Fig. 17c. Gain programming of BR filter.

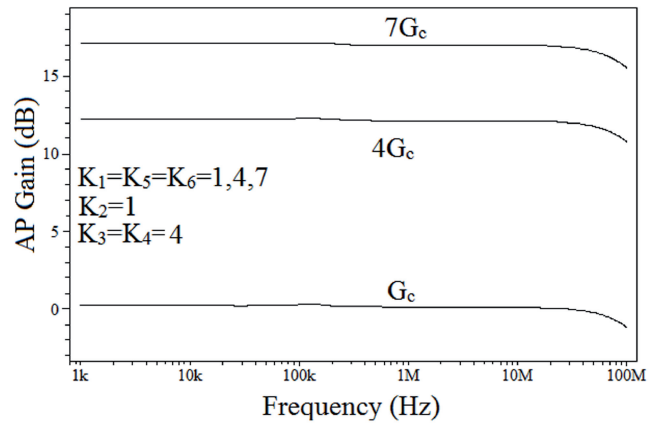


Fig. 17d. Gain programming of AP filter.

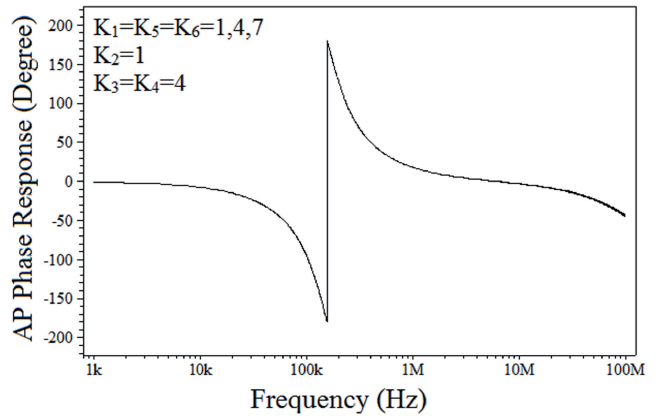


Fig. 17e. Phase response of AP filter.

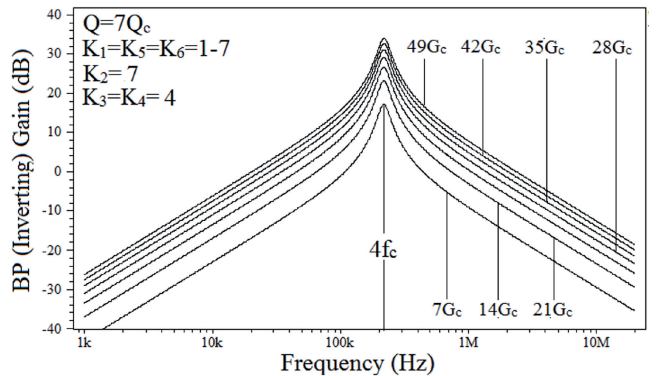


Fig. 17f. Gain programming of BPI filter. (In step of 7)

Gain programming of BPI using (17b,e) is performed by varying  $K_1(=K_5=K_6)$  at frequency  $4f_c$  with maximum quality factor of value  $7Q_c$  (Fig. 17f). It is evident that the maximum gain realizable is  $49G_c$ .

Quality factor programming through  $K_2$  as described by (17b) is shown Fig. 18 for BR filter for gain  $7G_c$ . Fig. 17f-18 clearly show the limitation of high Q (maximum  $7Q_c$ ) realization using (17).

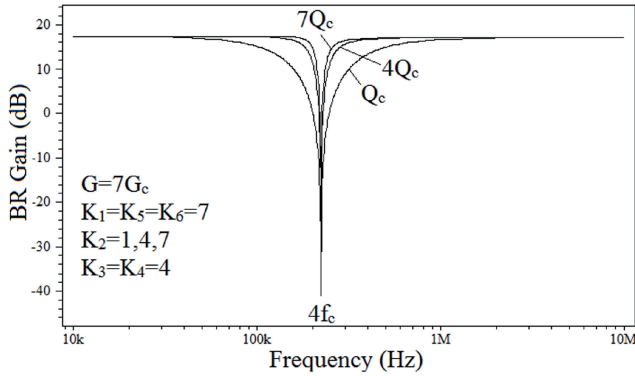


Fig. 18. Quality factor programming of BR filter.

In order to have high Q realization, programming of (18b) is adopted. Fig. 19 shows the same for BR and BPNI response by varying product term  $(K_2K_6)$ . Squared Q values shown in Fig. 19a results because  $K_2$  and  $K_6$  are set at same value. By setting different codeword values any Q value ranging from  $Q_c$  to  $49Q_c$  can be realized. As an example, Fig. 19b shows high-Q realization of BPNI in steps of seven by setting  $K_2=7$  and then varying  $K_6$  from 1 to 7.

Fig. 20 depicts the simultaneous gain and Q programming for BPI response as described by (18b,e). Decimal numbers shown on the response curve represents the common multiplier factor for both gain and Q. An example of high gain high-Q BPI filter is also shown in Fig. 16c with programmable  $f_o$ .

The performance of the proposed UF is compared in Tab. 4 with similar reported digitally programmable UFs. Comparison is based on the following important features. (1) Independently programmable pole frequency. (2) Independently programmable Q. (3) Independently program-

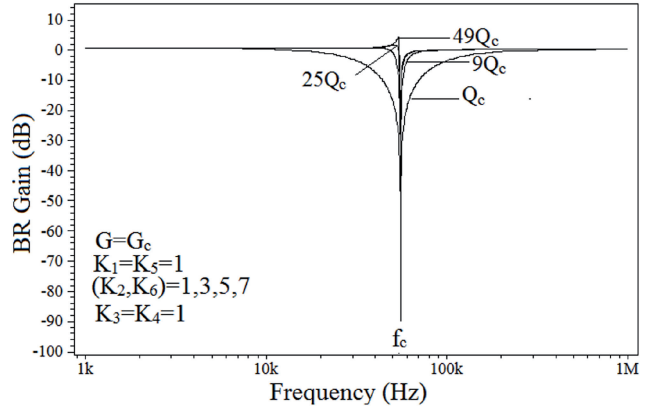


Fig. 19a. Q-factor programming of BR filter.

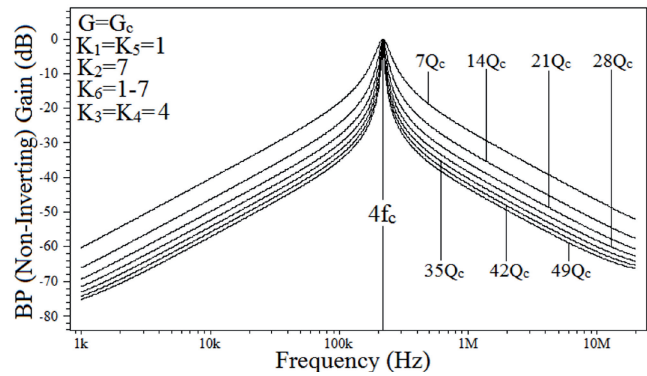


Fig. 19b. Q-factor programming of BPNI filter. (in steps of 7).

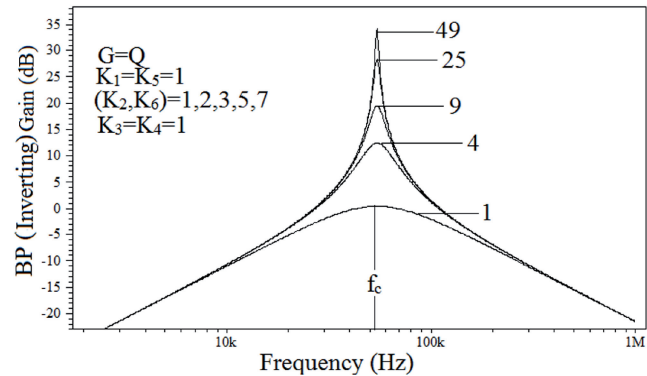


Fig. 20. Gain and quality factor programming of BPI filter.

Criteria/Ref	1	2	3	4	5	6	7	8	9	10	11	12	13	14
6 (Fig. 4b)	Y	Y	Y	Y	Y	NA	5	2	$(2^n-1)Q_c$	ALL	1	4CF+4DC-CF	CM	SIMO
10	Y	Y	Y	Y	Y	N	4	2	$(2^n-1)Q_c$	ALL	1	3DC-CDBA	CM	MISO
13	Y	Y	N	N	N	NA	5	1	$(2^n-1)Q_c$	3	1	3DC-CCII	CM	SIMO
4	Y	Y	N	Y	N	NA	16	4	$(2^n-1)Q_c$	3	1	5DC-FDCC	VM	SIMO
12 (Fig. 19)	Y	Y	Y	Y	N	NA	6	4	NA	1(LP)	1	3DC-BOTA	VM	SIMO
9	Y	Y	N	Y	N	NA	3	0	$2^n Q_c$	3	1	5DC-BOTA	VM	SIMO
7	Y	Y	Y	Y	N	NA	8	2	$*(2^n-1)^2 Q_c$	3	2	5DPCCII	VM	SIMO
Proposed	Y	Y	Y	Y	Y	N	9	2	$(2^n-1)^2 Q_c$	ALL	1	4DPCFA+2DPCCII	VM	MISO

Y-yes, N-no, NA-not applicable, \* with some constraint, DC-digitally controlled, CDBA- current differencing buffer amplifier, CF-current follower.

Tab. 4. Performance comparison of proposed filter.

mable gain. (4) Appropriate input port impedance. (5) Appropriate output port impedance. (6) Input inversion required. (7) Total number of passive components. (8) Total grounded capacitors. (9) Maximum Q attainable. (10) Number of filter functions generated. (11) Number of circuit configuration used. (12) Number of active elements used. (13) CM/VM (14) Topology.

The potential performance of the proposed UF is obvious from Tab. 4 itself. Attractive features of the proposed UF which are not available simultaneously in any of the reported configuration include full programmability, full cascadability and high-Q realization (for given  $n$ ). Though UF of [7] possess almost all these features except the fifth one (appropriate output port impedance) but its parameters are independently programmable in limited sense. Programming of one of the parameters ( $G$ ,  $\omega_0$ ,  $Q$ ) of the proposed UF do not put any constraint over remaining two parameters but the situation is quite different in [7]. Programming of one of the parameter of [7] makes either one or both of the remaining two parameters non-programmable e.g. high-Q ( $= 49Q_c$ ) realization needs constant values of gain ( $G = 7G_c$ ) and  $\omega_0$  ( $= \omega_c$ ); thus makes these parameters non-programmable. The similar constraint applies for  $\omega_0$  and  $Q$  programming of [10], [12] also. Apart from this high-Q realization of [7] needs different filter configuration while the proposed configuration needs only change in programming as described by (18). Availability of BP combination (BPNI and BPI) is another feature which is not present in any of the reported configuration.

It is evident from Tab. 4 that all the UF configurations though use lesser number of active elements but they either realize lesser number of filter functions [4], [7], [9], [12], [13] or operates in CM [6], [10], [13] which results in simplified circuit. CM UFs of [6], [10], [13] are further constrained by the need of additional circuitry for processing the input and output variables, whereas filter configuration of [6] needs three switches for AP and BR realization, [10] needs additional circuitry for providing weighted current input and [13] needs circuitry for taking current outputs available in working impedances of filter circuit. Apart from this the CDN structure used in [4], [10] increases its complexity as described in Section 1. UF of [12] though uses only three digitally controlled balanced output transconductance amplifier (DC-BOTA) but each consists of two fully differential current conveyors (FDCC) and two CDNs.

## 6. Conclusion

This paper presents a new low-voltage low-power CMOS current feedback amplifier (CFA). Using transistor arrays and MOS switches the proposed circuit is digitally controlled (DPCFA). Both the realization features high current drive capability and rail-to-rail voltage operation. As an application, DPCFA based digitally programmable multiple input single output UF is presented. The proposed

voltage mode filter offers the following advantageous features: generation of all the standard filter functions from same configuration, independently programmable filter parameters ( $\omega_0$ ,  $Q$ , gain), high-Q realization, no inverting input requirement, lesser effect of non-idealities, appropriate input/ output port impedances (high/low) making the UF cascadable. In addition to this, use of only two grounded capacitor makes it suitable for monolithic implementation. As the proposed filter is fully programmable, it may find various applications in mixed mode (analog / digital) VLSI system. All the circuits are realized and simulated using 0.25  $\mu\text{m}$  TSMC technology parameters.

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