

5 Watt GaN HEMT Power Amplifier for LTE

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Abstract. *This work presents the design and implementation of a stand-alone linear power amplifier at 2.4 GHz with high output power. A GaN HEMT transistor is selected for the design and implementation of the power amplifier. The device exhibits a gain of 11.7 dB and a drain efficiency of 39% for an output power of 36.7 dBm at 2.4 GHz for an input power of 25 dBm. The carrier to intermodulation ratio is better than 25 dB for a two tone input signal of 25 dBm of total power and a spacing of 5 MHz. The fabricated device is also tested with LTE input signals of different bandwidths (5 MHz to 20 MHz).*

Keywords

ACPR, GaN HEMT, linearity, LTE, PAPR, power amplifier.

1. Introduction

The increasing demand for radio frequency (RF) power amplifiers (PAs) in communication systems has led to enormous research efforts towards the development of reliable and low cost circuit designs with the best tradeoff between linearity and efficiency. As communication systems evolve to higher data rates the modulation schemes generate signals that are characterized by non-constant envelopes with high peak to average power ratio (PAPR). For instance, the Universal Mobile Telecommunications System (UMTS) standard reaches a PAPR of 7–10 dB while modulation schemes in Long Term Evolution (LTE) are characterized with a PAPR that exceeds 10 dB [1], [2], [3].

The high PAPR signals should be amplified linearly to avoid the signal distortion and thus the power amplifier should operate below the saturation at back off. To improve the efficiency in the back off region, several efficiency enhancement techniques have been proposed in the literature, including the envelope tracking (ET) technique [1], [4]. The ET topology consists of an RF power amplifier operating at its linear region and a dynamic power supply (DPS) that adjusts the power supply voltage provided to the amplifier according to the input power level. Several envelope tracking systems have been proposed in the literature recently [5], [6], [7], [8].

The specifications for the design of a power amplifier circuit depend on the targeted application and are significantly different for user equipment (UE) or base stations (BSs). The requirements for UE in terms of output power and linearity are modest in comparison to the base station power amplifiers due to the high power that is involved on the BS operation [3], [9]. The tight requirements for the design of high output power amplifiers result in a decreased efficiency [3], [9]. Thus, efficiency enhancement techniques have been applied for the design of linear power amplifiers for base station applications in the literature [10], [11].

Among the candidates for envelope tracking base stations power amplifiers stands the design of gallium nitride (GaN) high electron mobility transistor (HEMT) RF power amplifiers because of the inherent advantages of high breakdown voltage, high efficiency, high power density and large bandwidth (BW) [12], [13], [14].

This work presents the design of a 5 Watts stand-alone GaN HEMT linear power amplifier operating at 2.4 GHz that can have successful application in envelope tracking systems. The proposed circuit is manufactured and its performance is evaluated in terms of linearity, output power and efficiency. Various input signals, such as single carrier, two-tone and LTE signals have been used for the characterization of the power amplifier.

This work is organized as follows. Section 2 presents the design and implementation of the GaN HEMT power amplifier. The device is designed and optimized for optimum tradeoff between linearity and efficiency at 2.4 GHz. This section also includes the experimental characterization of the power amplifier in terms of power gain, power added efficiency (PAE) and drain efficiency (DE). Section 3 presents additional measurements to evaluate the linearity of the amplifier, such as two-tone IMD and ACPR. Section 4 summarizes the conclusions of the presented work.

2. Design and Implementation of GaN HEMT Power Amplifier

The design of the power amplifier starts with the set of specifications and the selection of the proper device. A gallium nitride high electron mobility transistor from Cree (CGH40006P) is chosen. The selected device operates

up to a frequency of 6 GHz [15]. According to its datasheet [15], the transistor is able to provide a drain efficiency of 43% and a gain of 11 dB at 2.4 GHz, for a $V_{DD} = 28$ V and an output power of 37 dBm. It also exhibits a third order intermodulation distortion of -26 dBc (26 dB below carrier) under these operating conditions.

The power amplifier is designed using the harmonic balance (HB) analysis in Agilent Advanced Design System software. The schematic of the designed power amplifier is shown in Fig. 1(a). The drain and gate bias networks are implemented as quarter wavelength bias lines with some decoupling capacitances, including chip capacitances and a radial stub with width = 0.415 mm, length = 19 mm and angle = 70°. DC-blocking capacitances are placed in the input (C_1, C_2) and output (C_3) matching networks.

The topology of the power amplifier includes three resistances (R_1, R_2 and R_3) that contribute to the global stabilization of the power amplifier for all the expected operation conditions in terms of bias voltage and input power level. Stability considerations should always be taken into account in the design of nonlinear devices in order to eliminate oscillation problems especially at RF and microwave frequency bands [16]. Large signal S-parameter (LSSP) analysis is used to perform the stability analysis of the device.

The input and output matching networks are designed and optimized to match the power amplifier to 50 Ohm. Small S-parameters and large signal scattering parameter (LSSP) analysis is also used to impose constraints on the impedance matching of the nonlinear device at the operating frequency band. The matching network parameters are optimized to match the instantaneous output impedance of the transistor at the fundamental frequency. The final circuit parameters are shown in Tab. 1.

Fig. 2 demonstrates a comparison among the simulated and measured small signal S-parameters performance over the frequency range of 0.5 GHz to 3 GHz showing good agreement between simulation and measurements. Design specifications for the linearity of the device are taken into account during the design of the power amplifier. Initially, the intermodulation distortion (IMD) sweet spots are examined to minimize the level of the nonlinear distortion [16], [17], [18]. The IMD sweet spots are particular points of operation that lead to high IMD ratio and

depend on the bias of the device, as well as the input power level.

The proposed system is simulated using Agilent Advanced Design System software (ADS) and is excited with a two tone input signal at f_1 GHz and f_2 GHz, with equal input power levels ($P_{in[f1]} = P_{in[f2]}$), where $f_2 > f_1$. The

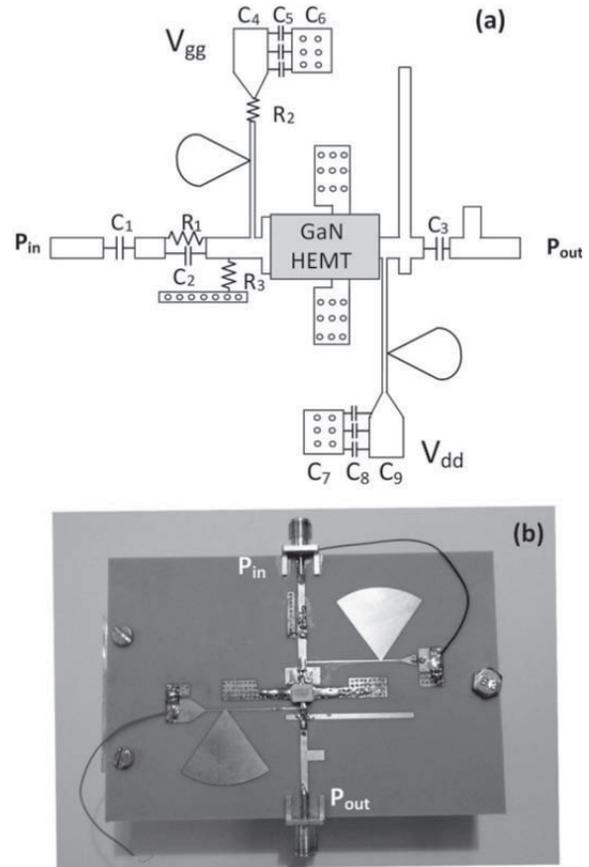


Fig. 1. 2.4 GHz GaN HEMT power amplifier: a) Simulated circuit topology and b) fabricated prototype.

Component	Value	Component	Value
C_1	1 pF	C_4	6.8 nF
C_2	0.5 pF	C_5	22 nF
C_3	3.3 pF	C_6	47 nF
R_1	5 Ohm	C_7	6.8 nF
R_2	52 Ohm	C_8	22 nF
R_3	390 Ohm	C_9	47 nF

Tab. 1. Power amplifier circuit component values.

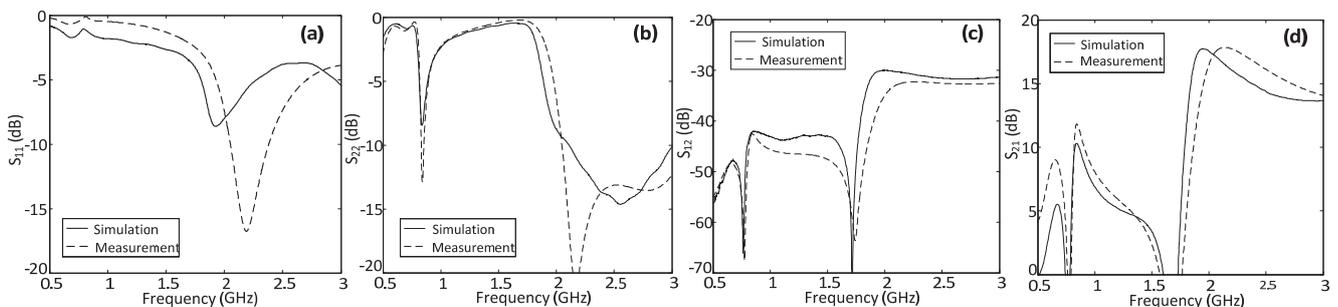


Fig. 2. Comparison of simulated (solid line) and measured (dashed line) small signal S-parameters performance over the frequency range of 0.5 GHz to 3 GHz: a) S_{11} , b) S_{22} , c) S_{12} , and d) S_{21} .

goal of the optimization process is to minimize the output power of the third order components, at $2f_1 - f_2$ GHz ($P_{out[2f_1-f_2]}$) and at $2f_2 - f_1$ GHz ($P_{out[2f_2-f_1]}$). High linearity should be met at high output power levels close to 1 dB compression point. The selected operating frequencies are $f_1 = 2.395$ GHz and $f_2 = 2.405$ GHz and the input power level is $P_{in[f_1]} = P_{in[f_2]} = 22$ dBm.

The optimum intermodulation ratio is predicted from the nonlinear simulation when the device is biased with a drain voltage (V_{ds}) of 35 V and a gate voltage (V_{gs}) of -3.5 V. A comparison of the carrier to intermodulation ratio is shown in Fig. 3 demonstrating that the optimum IMD behavior is achieved for $V_{gs} = -3.5$ V in Fig. 3.

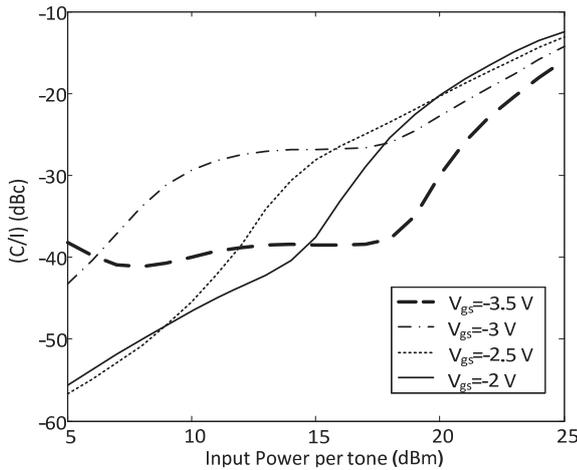


Fig. 3. Simulated carrier to intermodulation ratio versus input power level for $V_{gs} = -3.5$ V, $V_{gs} = -3$ V, $V_{gs} = -2.5$ V and $V_{gs} = -2$ V. The selected operating frequencies are $f_1 = 2.395$ GHz and $f_2 = 2.405$ GHz. The results are obtained when the device is biased with a drain bias of 35 V.

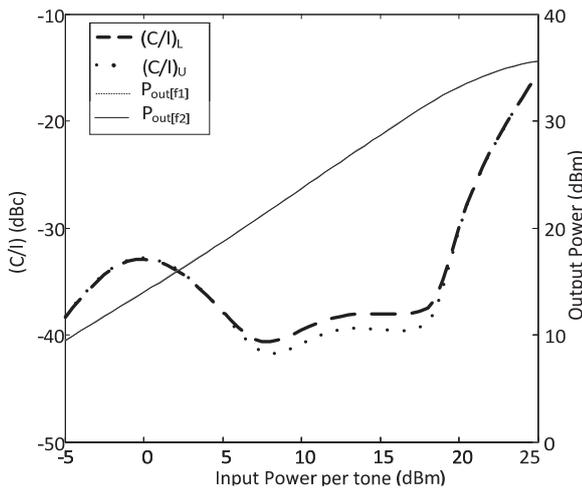


Fig. 4. Simulated output power and carrier to intermodulation ratio versus input power level of one of the tones. The selected operating frequencies are $f_1 = 2.395$ GHz and $f_2 = 2.405$ GHz. The results are obtained for $V_{ds} = 35$ V and $V_{gs} = -3.5$ V.

The simulation results show a high linearity level for a wide input power range when the device operates in its linear region for the selected bias conditions.

Fig. 4 depicts the simulated output power and the carrier to intermodulation ratio of the power amplifier when excited by a two-tone signal around 2.4 GHz ($f_1 = 2.395$ GHz and $f_2 = 2.405$ GHz). The x-axis corresponds to the total power of one of the tones, which means the total input power at the amplifier is 3 dB higher.

The output power at the operating frequencies ($P_{out[f_1]}$ and $P_{out[f_2]}$) is shown in the plot, along with the upper and lower carrier to intermodulation ratios (C/I_U and C/I_L). Details about the calculation of the carrier to intermodulation ratio are given in Section 3. A reduced IMD is noticed when the power amplifier operates with total input power from 8 dBm (5 dBm each tone) to 23 dBm (20 dBm each tone) for the selected bias.

The potential use of the device as the RF power amplifier of an envelope tracking topology is examined by varying the drain voltage of the device. The performance of the device is compared when the power amplifier operates with an input signal at 2.4 GHz and for $V_{gs} = -3.5$ V. The simulated performance of the power amplifier over a wide range of output power levels is shown in Fig. 5 and Fig. 6.

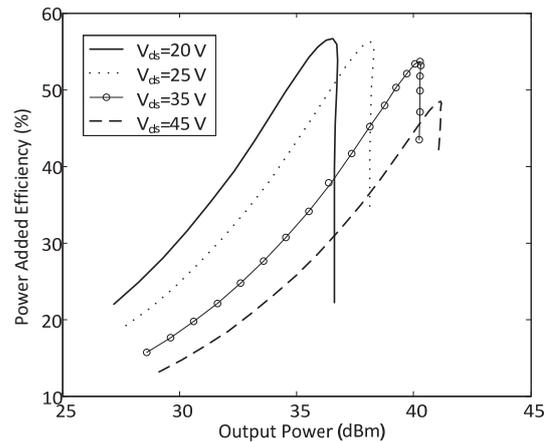


Fig. 5. Simulated power added efficiency versus output power for $V_{ds} = 20$ V, $V_{ds} = 25$ V, $V_{ds} = 35$ V and $V_{ds} = 45$ V. The power amplifier operates at 2.4 GHz and the selected gate voltage is -3.5 V.

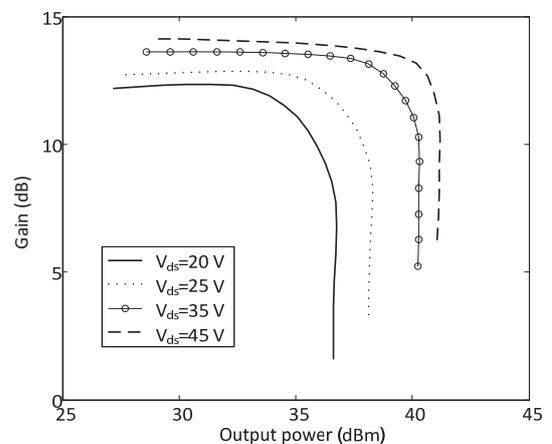


Fig. 6. Simulated gain of the power amplifier for different drain voltages ($V_{ds} = 20$ V, $V_{ds} = 25$ V, $V_{ds} = 35$ V and $V_{ds} = 45$ V) and output power levels.

It can be observed that different efficiency levels are achieved for various drain voltage and input power values. Thus, the proposed device could be potentially used in an envelope tracking topology in order to improve the average efficiency of the device when operating with high PAPR input signals and time varying envelopes, such as LTE.

The implemented power amplifier circuit is shown in Fig. 1(b) and has a total size of 6 cm x10 cm. The device is fabricated in Arlon 25N substrate with dielectric constant of 3.38, loss tangent of 0.0027 and thickness of 0.5 mm.

Initially, the fabricated prototype is characterized with a single tone input signal using a signal generator and a spectrum analyzer from Agilent. The device is characterized in terms of its output power level (P_{out}), gain (G), drain efficiency (DE) and power added efficiency (PAE).

The drain efficiency is given by the ratio of the output power and the dissipated power (P_{dc}) [4]:

$$DE = \frac{P_{out}}{P_{dc}} \quad (1)$$

The power added efficiency takes into account the RF input power and is defined as [4], [16]:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \quad (2)$$

Tab.2 shows a comparison of the simulated and measured performance of the fabricated power amplifier for the frequency band of interest (2.4 GHz - 2.45 GHz). The device demonstrates a measured gain of 11.7 dB and a drain efficiency of 39% for an input power of 25 dBm at 2.4 GHz.

	Simulated Performance at 2.4 GHz -2.45 GHz	Measured Performance at 2.4 GHz -2.45 GHz
P_{out}	38.1 dBm – 37.9 dBm	36.7 dBm – 37.7 dBm
G	13.1 dB – 12.9 dB	11.7 dB – 12.7 dB
DE	47.2 % – 45.4 %	39 % – 43.3 %
PAE	44.9 % – 43.1 %	37 % – 41 %

Tab. 2. Measured and simulated output power, gain, drain efficiency and power added efficiency of the power amplifier for a fixed input power of 25 dBm. The device is biased with 35 V drain and -3.5 V gate voltage.

3. Linearity and ACPR Characteristics

The performance of the power amplifier in terms of linearity is evaluated with different input signals. Initially, the power amplifier is tested with a single carrier input signal and thus the 1 dB compression point is defined. A two tone input signal is used in order to evaluate the linearity of the power amplifier by calculating the carrier to intermodulation (C/I) ratio. The device is also tested in an LTE environment using an LTE input signal.

3.1 Single Carrier Input Signal

The performance of the amplifier is evaluated for different input power levels. The measured output power and gain when the input varies from 0 to 27 dBm are shown in

Fig. 7. As the input power increases, the device is driven into saturation. It is observed that the maximum linear output of the stand-alone power amplifier is 24 dBm and corresponds to an input power of 10 dBm and a gain of 14 dB at 2.4 GHz. The measured value of the 1 dB (P_{1dB}) compression point for one tone input signal is observed at 22 dBm of input power.

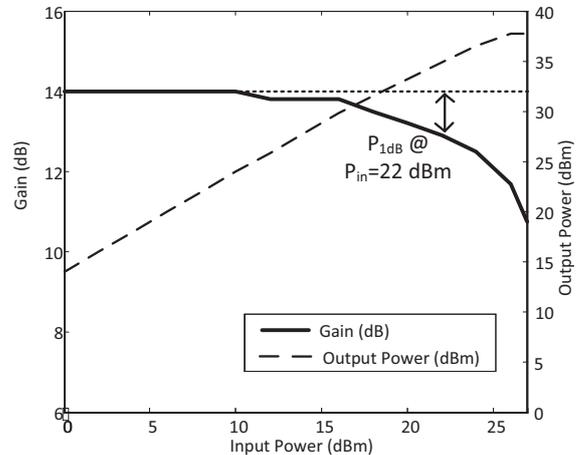


Fig. 7. Measured output power and gain for a 2.4 GHz input signal as a function of the input power level. The measurements are for $V_{ds} = 35$ V and $V_{gs} = -3.5$ V.

3.2 Two-tone Input Signal

One of the most widely used nonlinear distortion metrics is the carrier-to intermodulation ratio (C/I). The C/I is defined as the ratio between the carrier output power (P_{out}) and the intermodulation product output power ($P_{out[2f_1-f_2]}$ or $P_{out[2f_2-f_1]}$). Many factors including memory effects contribute to C/I asymmetries at the output power spectrum, such as unequal output power in the intermodulation products [16], [17], [18], [19], [20]. Thus, due to asymmetry in the upper and lower bands of the intermodulation products, the C/I is defined as lower (C/I_L) and upper C/I (C/I_U), where C/I_L is calculated as $P_{out[f_1]}/P_{out[2f_1-f_2]}$ and C/I_U as $P_{out[f_2]}/P_{out[2f_2-f_1]}$.

The C/I ratio is measured using a two-tone input signal. The two tones have equal amplitude and they are centered around 2.4 GHz. The C/I is calculated for different frequency spacings ($\Delta f = f_2 - f_1$) between the two tones (5 MHz, 10 MHz, 15 MHz, 20 MHz). Each of the tones has a power of $P_{in[f_1]} = P_{in[f_2]} = 22$ dBm. The measurement set up is depicted in Fig. 8.

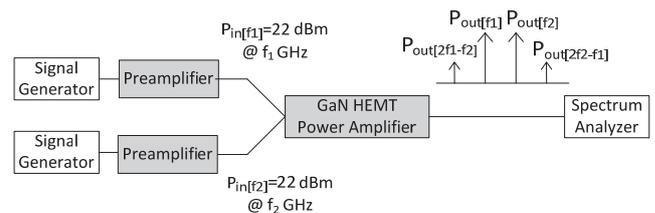


Fig. 8. Measurement set up for a two tone characterization of the power amplifier. The device is tested for different frequency spacing at a center frequency of 2.4 GHz.

Two preamplifiers are used as the signal generators are not able to give such a high output power. The preamplifiers are adjusted to provide an input signal of 22 dBm to the fabricated power amplifier at the selected frequencies.

The output spectrum of the power amplifier when excited with a two tone 22 dBm input signal at 2.395 GHz and 2.405 GHz ($\Delta f = 10$ MHz) is shown in Fig. 9. The power amplifier operates at the compression region and the obtained lower and upper carrier to intermodulation ratios are 24.3 dB and 24.6 dB, respectively.

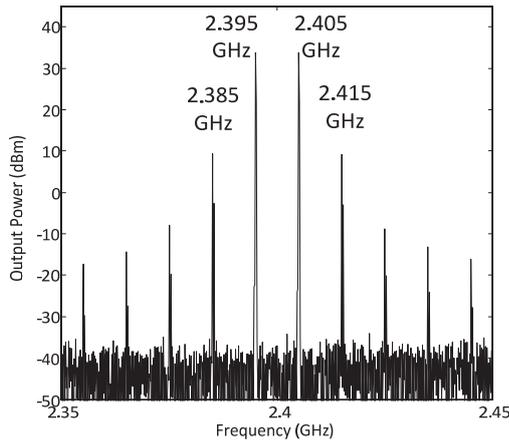


Fig. 9. Output spectrum when the power amplifier is excited with a two tone input signal (22 dBm each of them) of a center frequency of 2.4 GHz and spacing of 10 MHz.

$(C/I)_L$ and $(C/I)_U$ for different frequency spacing are shown in Tab. 3 demonstrating a good performance even though the device is not operating at its linear region. It is shown that for a spacing of 5 MHz the power amplifier demonstrates a carrier to intermodulation ratio better than 25 dB. The asymmetry between the lower and upper carrier to intermodulation ratios is attributed to the measurement setup.

Δf	$(C/I)_L$	$(C/I)_U$
5 MHz	25.4 dB	32 dB
10 MHz	24.3 dB	24.6 dB
15 MHz	23.4 dB	25.4 dB
20 MHz	24.9 dB	22.3 dB

Tab. 3. Lower and upper carrier to intermodulation ratios for different frequency spacing at 2.4 GHz. The measurements are made for a two-tone input signal of 22 dBm power each.

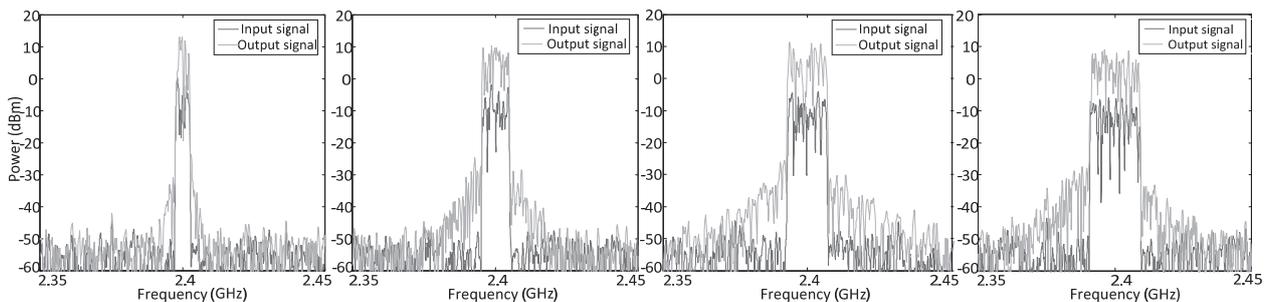


Fig. 11. Measured output spectrum for an LTE 2.4 GHz input signal for a variety of different bandwidths: a) 5 MHz, b) 10 MHz, c) 15 MHz and d) 20 MHz. The input signal has an input power of 5 dBm.

3.3 LTE Input Signal

The linearity of the proposed topology is also tested using an LTE input signal. LTE supports different channel bandwidths ranging from 1.4 MHz to 20 MHz (1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz and 20 MHz) to deploy more spectrum flexibility than the previous systems. The wider channel bandwidths of 10 MHz, 15 MHz and 20 MHz target to improve the system performance as users may perceive that they have a wide bandwidth connection while sharing the bandwidth with individual users [3].

One concern in the design of a linear power amplifier is its behavior at the adjacent channels. One of the metrics that are used for the protection of the adjacent channel is the adjacent channel power ratio (ACPR) [3]. An LTE signal is used as the input signal of the device for the calculation of the ACPR. The measured complementary cumulative distribution function (CCDF) of the envelope of the LTE input signal is depicted in Fig. 10.

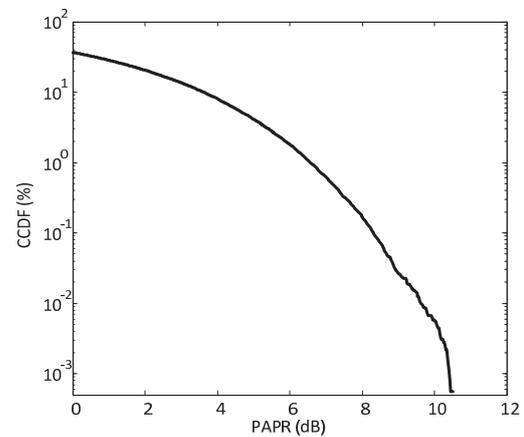


Fig. 10. Measured complementary cumulative distribution function of the envelope of a downlink LTE signal (BW = 10 MHz).

Fig. 11 shows the measured output spectrum of the fabricated power amplifier for an input LTE signal with total power of 5 dBm and a bandwidth of 10 MHz. Measurements with a higher input power level is not possible as the available instrumentation in the laboratory is not able to give more output power. As it can be observed from Fig. 12, two unequal adjacent channels exist and therefore different metrics are defined: the lower ACPR and the upper ACPR.

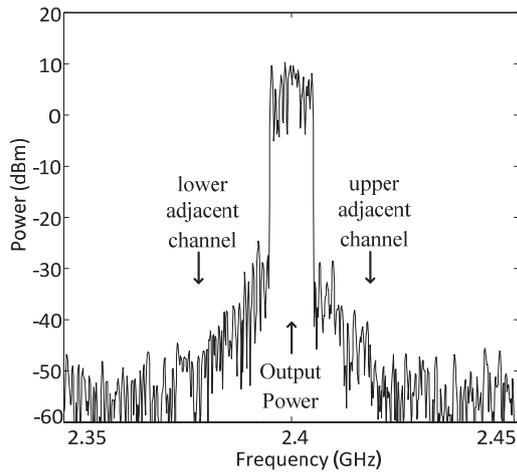


Fig. 12. Output spectrum of the power amplifier when excited with an LTE signal. The input power level is 5 dBm and the bandwidth 10 MHz.

The lower adjacent channel power ratio ($ACPR_L$) is defined as the ratio between the total output power measured in the fundamental zone around the carrier, P_{out} , and the total power in the lower adjacent-channel power ($P_{out,L}$). The same applies for the upper $ACPR$ ($ACPR_U$) which is defined as the ratio of the P_{out} and the upper adjacent-channel power ($P_{out,U}$).

The nonlinear distortion of the output signal is shown in Tab. 4. It can be noted that the $ACPR_L$ and $ACPR_U$ are higher than 40 dB for an input power of 5 dBm. The power amplifier has almost the same ACPR performance regardless of the LTE input signal bandwidth. The overall performance of the power amplifier is summarized in Tab. 5.

Bandwidth	$ACPR_L$	$ACPR_U$
5 MHz	43.2 dB	44.2 dB
10 MHz	40.7 dB	43 dB
15 MHz	41 dB	43.75 dB
20 MHz	40 dB	43.4 dB

Tab. 4. Measured adjacent channel power ratio of the power amplifier for various bandwidths (5 MHz, 10 MHz, 15 MHz and 20 MHz).

Drain Voltage	35 V
Gate Voltage	-3.5 V
Output Power @ Pin=25 dBm	36.7 dBm
Gain @ Pin=25 dBm	11.7 dB
Drain Efficiency @ Pin=25 dBm	39 %
C/I ($\Delta f = 10$ MHz) @ Pin=25 dBm	(C/I) _L =24.3 dB (C/I) _U =24.8 dB
ACPR for a 5 dBm LTE signal (BW=10 MHz)	$ACPR_L$ =40.7 dB $ACPR_U$ =43 dB

Tab. 5. Summarized performance of the power amplifier at 2.4 GHz.

4. Conclusions

A 5 Watts GaN HEMT power amplifier operating at 2.4 GHz is designed and characterized. The power amplifier demonstrates a DE of 39% and 11.7 dB of gain for an input signal level of 25 dBm. The device achieves a carrier

to intermodulation ratio as good as 25 dB for a two tone input signal of 25 dBm of total power when it is not operating at its linear region.

The fabricated power amplifier is also tested with LTE input signals with different input signal bandwidths (5 MHz to 20 MHz). The power amplifier despite its simple design achieves high linearity close to 1 dB compression point. Finally, the proposed design, taking advantage of the device linearity sweet spots can have successful application in envelope tracking systems.

Acknowledgements

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