Fully CMOS Memristor Based Chaotic Circuit

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Abstract. *This paper demonstrates the design of a fully CMOS chaotic circuit consisting of only DDCC based memristor and inductance simulator. Our design is composed of these active blocks using CMOS 0.18 μm process technology with symmetric ±1.25 V supply voltages. A new single DDCC+ based topology is used as the inductance simulator. Simulation results verify that the design proposed satisfies both memristor properties and the chaotic behavior of the circuit. Simulations performed illustrate the success of the proposed design for the realization of CMOS based chaotic applications.*

Keywords

Memristor, CMOS design, DDCC, Chua's circuit, chaotic oscillators.

1. Introduction

In 1971, Leon Chua theoretically claimed that the memristor is the fourth circuit element besides the three well-known circuit elements; namely, resistor, capacitor and inductor [1]. For a long time, it remained just as a theoretical element and rarely appeared in the literature because of having no simple and practical realization. In 2008, a group of researchers from HP laboratories announced the fabrication of a physical implementation behaving as a memristor [2]. Its prototype is based on a TiO_2 thin film containing doped and un-doped regions between two metal contacts at nanometer scale. This implementation, realized by HP researchers, has attracted significant attention.

It is expected that memristors can be applied and provide new additional features to analog circuits. Various analog and chaotic applications of memristor to analog, chaotic and synaptic circuits are studied in the literature [3]-[11]. Despite large-scale interest on memristor and emerging many studies, no commercially available memristor exists yet. In this sense, a proper physical implementation representing the memristor behavior is of great importance from the point of view of real-world circuit design.

SPICE macromodels and memristor emulators exhibiting memristor-like behavior are presented in the literature [12]-[22]. SPICE models are useful for modeling characteristics of the memristor, but they have not been an alternative in practical realizations. Emulators can represent the behavior of memristor in a restricted extent and they can be applicable on some real applications.

Some inductorless implementations of Chua's circuit have been presented in the literature [23], [24]. Implementation approach of CMOS memristor employing Differential Difference Current Conveyor (DDCC) based blocks is presented previously [8].

In this paper, we propose a fully CMOS DDCC based scheme to realize memristor. It is pointed out that, this is an appropriate design for circuit. Also physical charge-flux characteristic of memristor. Memristor is constructed to behave convenient to the cubic memristor definition. Beyond our prior work, in this implementation appropriate chaotic behavior is obtained by using fully CMOS DDCC based a new CMOS based inductance simulator is used. Along with that, supply voltages and process technology is selected properly to current CMOS processes.

The paper is structured as follows: Section 2, which follows this introduction, summarizes the nonlinear cubic modeling of memristor. Section 3 includes the memristor-based Chua's circuit along with its dynamics with MATLAB simulations. In Section 4 we present the detailed design steps of our DDCC memristor-based chaotic circuit. Also in this section DDCC based inductance simulator is introduced. In Section 5 we present characteristics of memristor-based Chua's circuit. This section is devoted to the demonstrations of SPICE simulations based on the proposed design. Finally, the conclusions of this work are given in the sixth section.

2. Modeling of Memristor with Cubic Nonlinearity

Memristor can be defined with two types of nonlinear constitute relation between the device voltage and current:

$$v = M(q)\,i\,, \tag{1}$$

$$i = W(\varphi)\,v \tag{2}$$

where $M(q)$ and $W(\varphi)$ are nonlinear functions which are

called memristance and memductance respectively and they are defined by:

$$M(q)=\frac{d\varphi(q)}{dq}, \tag{3}$$

$$W(\varphi)=\frac{dq(\varphi)}{d\varphi}. \tag{4}$$

The memristor designed in this work is a flux controlled memristor described by the relation in (2). The relation between the terminal voltage $v(t)$ and the terminal current $i(t)$ of the memristor is obtained by:

$$i(t)=\frac{dq}{dt}=\frac{dq}{d\varphi}\frac{d\varphi}{dt}=\frac{dq}{d\varphi}v(t)=W\left(\varphi(t)\right)v(t). \tag{5}$$

Nonlinear resistor in Chua's circuit is defined by Zhong with cubic nonlinearity. It has been revealed that, all features of the circuit are captured correctly by this definition [25]. The $q(t)$ - $\varphi(t)$ function of memristor with cubic nonlinearity is used for implementation of chaotic circuits [26]. The cubic polynomial definition of memristor is defined as follows:

$$q(\varphi)=\alpha\varphi+\beta\varphi^3. \tag{6}$$

Thus, the memductance function is given by:

$$W(\varphi)=\frac{dq}{d\varphi}=\alpha+3\beta\varphi^2. \tag{7}$$

Considering (7) and the flux-voltage relation, we get (8). Our definition in this work, is based this relation.

$$i(t)=\left[\alpha+3\beta\left(\int v(t)\,dt\right)^2\right]v(t). \tag{8}$$

The memristor circuit introduced employs only DDCC based sub blocks such as mainly integrator, squarer, multiplier and summer. Designs of these active blocks are given in the following sections.

3. Chaos in Memristor-Based Chua's Circuit

Memristor-based Chua's circuit used in this work is shown in Fig. 1.

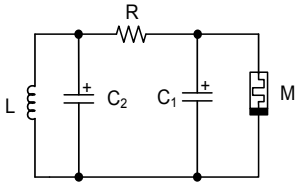

Fig. 1. Memristor-based Chua's circuit.

Note that mathematical background of the memristor-based Chua's circuit illustrated in Fig. 1 is studied earlier in [26]. We apply the DDCC based CMOS circuit proposed in our work to the realization of the Chua's circuit.

The dynamical state equations of memristor-based Chua's circuit can be described by

$$\begin{aligned}
\frac{d\grave{\varphi}(t)}{dt}&=\grave{v}_{C_1}(t)\\
L\frac{d\grave{i}_L}{dt}&=\grave{v}_{C_2}(t)\\
C_1\frac{d\grave{v}_{C_1}(t)}{dt}&=\frac{1}{R}\left(\grave{v}_{C_2}(t)-\grave{v}_{C_1}(t)\right)-W\left(\grave{\varphi}(t)\right)\grave{v}_{C_1}(t)\\
C_2\frac{d\grave{v}_{C_2}(t)}{dt}&=\frac{1}{R}\left(\grave{v}_{C_1}(t)-\grave{v}_{C_2}(t)\right)-\grave{i}_L(t)
\end{aligned} \tag{9}$$

where $W(\varphi(t))$ is memristor memductance and is defined by (7). By considering α, β and other circuit parameter values from [25], [26] this unscaled system gives unrealistic currents (up to hundred amps) and voltages (above kilo volts). In traditional op-amp based implementations currents and voltages are scaled about at mA and ten-volt levels [25], [26]. For our CMOS design we need to reduce much lower than these levels. Rescaled current and voltages are defined as:

$$\begin{aligned}
\varphi(t)&=\frac{1}{\delta}\grave{\varphi}(t)\\
v_{C_1}(t)&=\frac{1}{\delta}\frac{1}{\gamma}\grave{v}_{C_1}(t)\\
v_{C_2}(t)&=\frac{1}{\delta}\frac{1}{\gamma}\grave{v}_{C_2}(t)\\
i_L(t)&=\frac{1}{\delta}\frac{1}{\gamma}\grave{i}_L(t)
\end{aligned} \tag{10}$$

The following set of equations is obtained as our rescaled system.

$$\begin{aligned}
\frac{d\varphi(t)}{dt}&=\frac{v_{C_1}(t)}{\delta}\\
\frac{di_L(t)}{dt}&=\frac{v_{C_2}(t)}{L}\\
\frac{dv_{C_1}(t)}{dt}&=\frac{1}{C_1}\left(\frac{v_{C_2}(t)-v_{C_1}(t)}{R}\right)-\left(\alpha+3\beta\varphi^2(t)\right)v_{C_1}(t)\\
\frac{dv_{C_2}(t)}{dt}&=\frac{1}{C_2}\left(\frac{v_{C_1}(t)-v_{C_2}(t)}{R}\right)-i_L(t)
\end{aligned} \tag{11}$$

where β is also rescaled with

$$\beta=\grave{\beta}\frac{1}{\gamma^2} \tag{12}$$

Let $\delta = 1.6\ \text{k}\Omega \times 47\ \text{nF} = 7.52\times10^{-5}$, $C_1 = 7.2$ nF, $C_2 = 70$ nF, $L = 18$ mH, $R = 1.97$ kΩ. $\alpha = -0.662 \times 10^{-3}$ and $\beta = 18.75 \times 10^{-3}$. Initial values are $\varphi(0) = 0$, $i_L(0) = 0$, $v_{C1}(0) = 0.01$, $v_{C2}(0) = 0.01$. This parameter set will be used as design basis synthesizing of the CMOS circuit.

The bifurcation diagram of the system with respect to R is shown in Fig. 2. R is very important to create the chaotic behavior. Time domain waveforms and chaotic

phase portraits from MATLAB simulations are shown in Fig. 3 and Fig. 4, respectively.

In a recent work, it has been shown that the type of singularities may be an indication of chaos [27]. Following up in this direction, it may be useful to note that the system in (11) has a single singularity on the origin, i.e. $v_{C1} = v_{C2} = i_L = 0$ unlike conventional Chua's system; thus we think that a detailed study of the system from the perspective introduced in [27] would be useful, while being beyond this paper's scope.

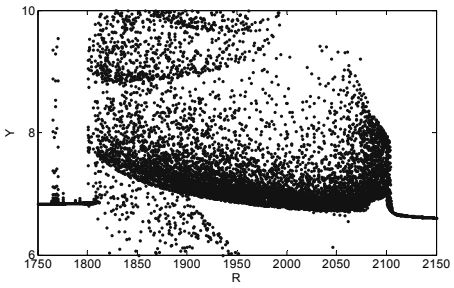

Fig. 2. The bifurcation diagram with respect to R.

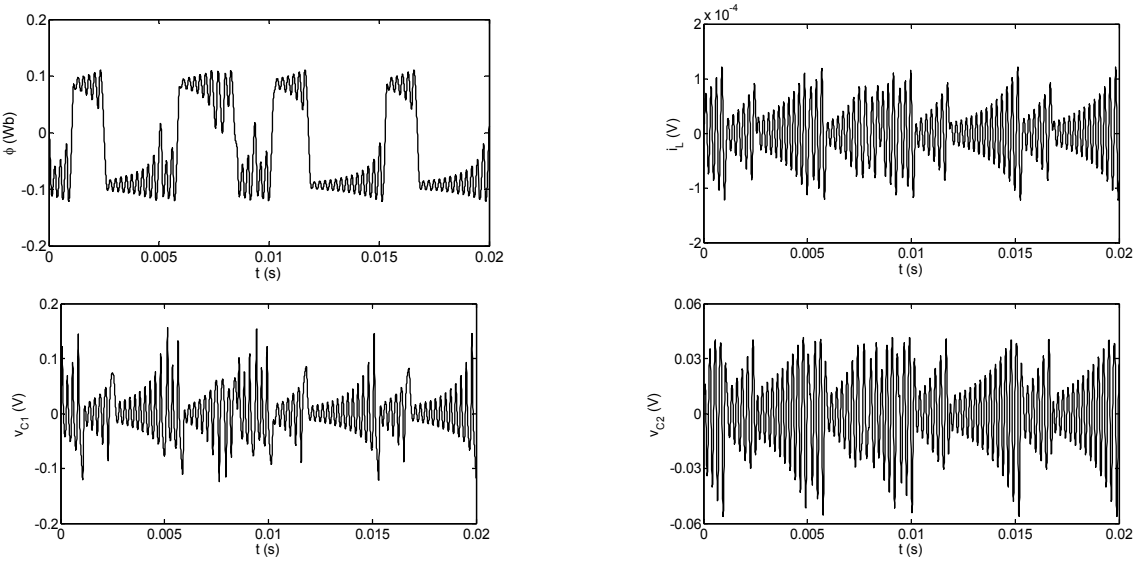

Fig. 3. Time domain waveforms of chaotic signals from MATLAB simulations.

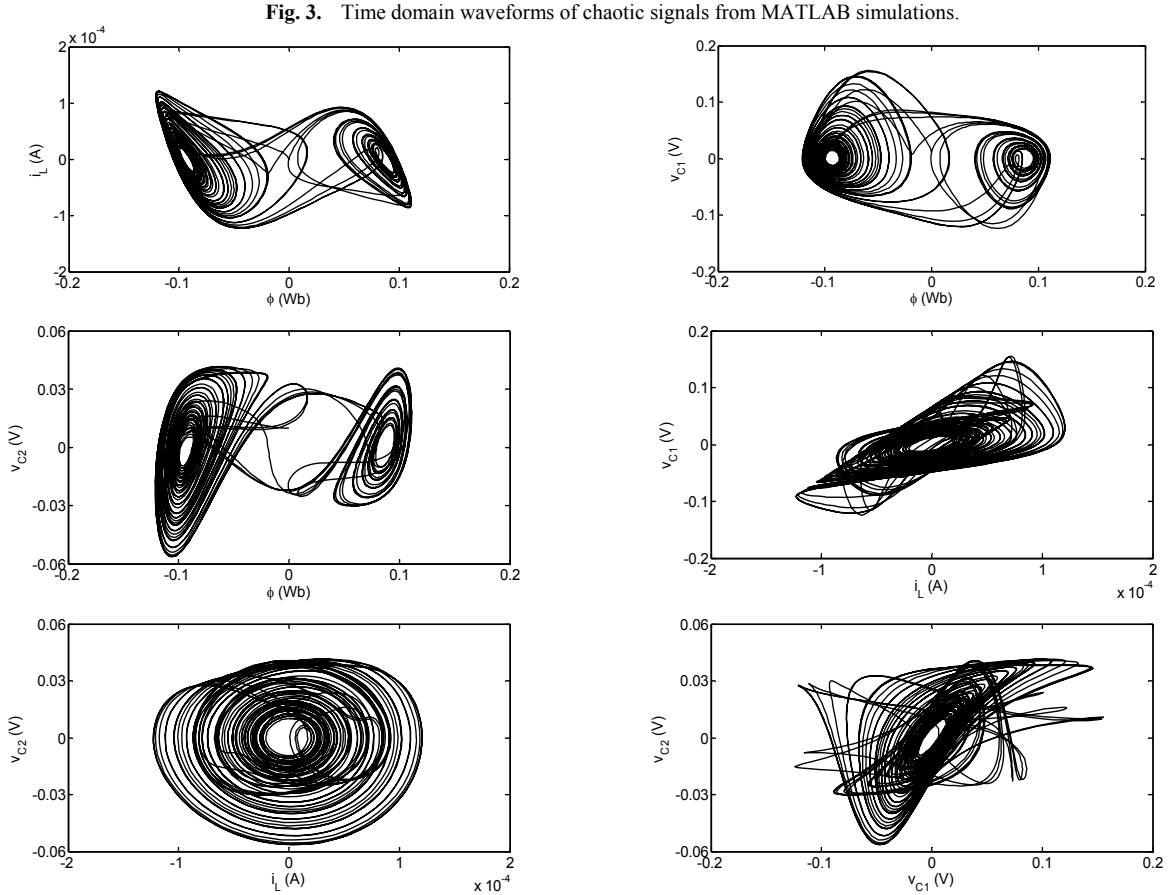

Fig. 4. Phase portraits from the MATLAB simulations.

4. Design of Fully CMOS Memristor-Based Chaotic Circuit

4.1 DDCC

DDCC is a 5-terminal active circuit block. Circuit symbol of DDCC is given in Fig. 5. Its terminal characteristics can be defined by a hybrid matrix giving the output of the five ports in terms of their corresponding inputs as shown in (13) [28].

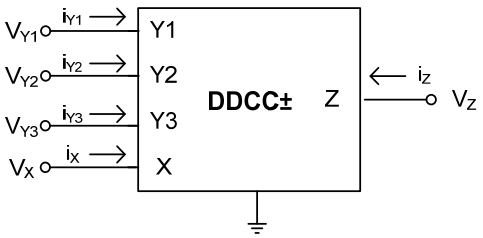

Fig. 5. Circuit symbol of DDCC.

$$\begin{bmatrix} i_{Y1} \\ i_{Y2} \\ i_{Y3} \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_{Y1} \\ v_{Y2} \\ v_{Y3} \\ i_X \\ i_Z \end{bmatrix} \tag{13}$$

Here ± (plus or minus) sign indicates whether DDCC is non-inverting or inverting type denoted as DDCC+ or DDCC- respectively.

4.2 Block Diagram of Proposed DDCC Based Memristor

The proposed principle block diagram of memristor constructed employing only CMOS DDCC based sub blocks is shown in Fig. 6.

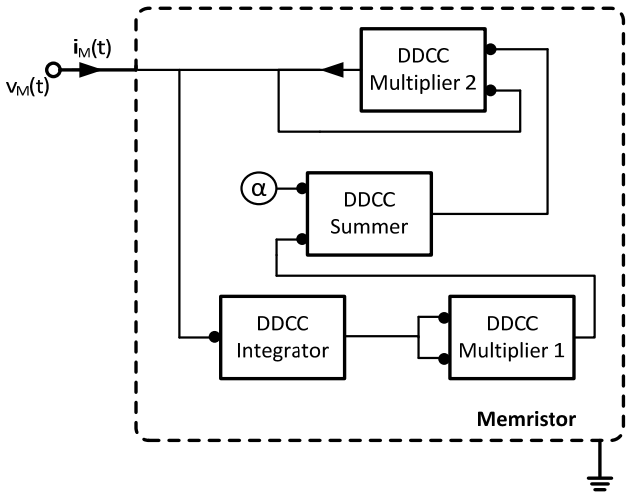

Fig. 6. Principle block diagram of proposed memristor implementation.

Four main CMOS stages are used in our memristor design. The first block works as an integrator. Also this block behaves as a buffer and it is used to avoid loading effect and insulate the current from the other stages. The output of the first block is connected both of the inputs of the multiplier and here it is the square of the voltage. The next block is summing block which also incorporates coefficients defined in (8) to the process. This block also makes current-voltage conversion in order to produce the inputs of the multiplier in voltages form. Finally, the current of our active memristor is generated after the output of this last multiplier block.

4.3 Sub-blocks of Memristor

4.3.1 Integrator

DDCC based integrator is shown in Fig. 7. For $R_X = \infty$ the output characteristics of the circuit can be derived as follows:

$$V_O = \frac{V_1 - V_2 + V_3}{sRC}. \tag{14}$$

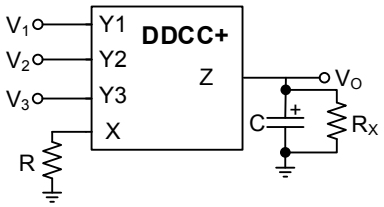

Fig. 7. DDCC based integrator.

Only C is used at the output of the integrator. Its parameters are defined as R = 1.6 kΩ and C = 47 nF.

4.3.2 Multiplier

In order to obtain DDCC based multiplier, the combination of two DDCC differential squarer is used [28]. The schematic of differential squarer is given in Fig. 8.

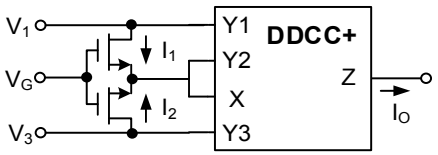

Fig. 8. DDCC based differential squarer.

In triode region, drain current of a MOS transistor can be expressed as follows:

$$I_D = K\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right], \tag{15}$$

$$K = \frac{1}{2}\mu C_{ox}\frac{W}{L}. \tag{16}$$

Considering the voltage relation of DDCC between X-Y inputs and supposing the transistors are well matched, the output current I_O can be derived as

$$
\begin{aligned}
I_O &= -(I_1 - I_2) \\
&= -K\left[2\left(V_G - \frac{V_1+V_3}{2} - V_T\right)\left(V_1 - \frac{V_1+V_3}{2}\right) - \left(V_1 - \frac{V_1+V_3}{2}\right)^2\right] \\
&-K\left[2\left(V_G - \frac{V_1+V_3}{2} - V_T\right)\left(V_3 - \frac{V_1+V_3}{2}\right) - \left(V_3 - \frac{V_1+V_3}{2}\right)^2\right] \\
&= \frac{K}{2}(V_1 - V_3)^2 = K_s(V_1 - V_3)^2
\end{aligned}
\tag{17}
$$

If a DDCC- is used here, the output current would be obtained as follows

$$I_O = -\frac{K}{2}(V_1 - V_3)^2 = -K_s(V_1 - V_3)^2 . \tag{18}$$

DDCC based multiplier [28] can be realized employing two squarers as shown in Fig. 9. Summing the outputs of both squarers, the output characteristics of the multiplier is obtained as given in (19).

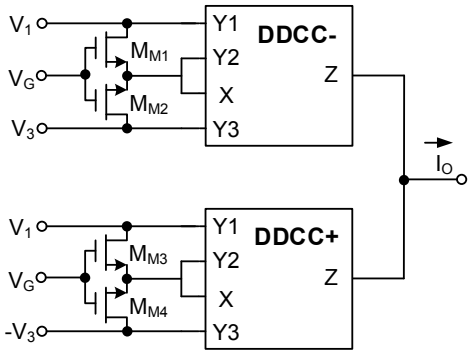

Fig. 9. DDCC multiplier.

$$I_O = \left[\frac{K}{2}(V_1 + V_3)^2 - \frac{K}{2}(V_1 - V_3)^2\right] = 2KV_1V_3 = K_M V_1 V_3 \tag{19}$$

where K_M is the multiplying coefficient of the multiplier. Aspect ratios of MOS transistor used at inputs of the multiplier stage are $W/L = 40\ \mu m / 1\ \mu m$ and $W/L = 10\ \mu m / 1\ \mu m$ for multiplier 1 and multiplier 2, respectively. Gate voltages of these transistors are defined as $V_G = 0.75$ V and drain currents are decreased as soon as possible preserving required multiplying situation. It is clear from Fig. 9 that the outputs of multipliers are current. The output current of multiplier 2 corresponds current of memristor. However current at the output of memristor 1 will be converted to voltage as stated in description of the summer block.

4.3.3 Buffer

DDCC has buffered inputs with very high gate impedances. Normally there is no need to additional buffer stages. However, DDCC multipliers have additional drain-input MOS transistors. So, DDCC based buffers are used at the input stages of these multipliers as shown in Fig. 10.

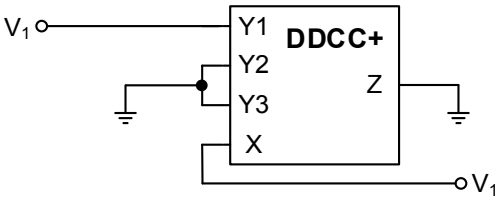

Fig. 10. DDCC based buffer.

4.3.4 Inverter

As can be seen from Fig. 9 we need an inverter at one of the inputs of the each DDCC multiplier. To obtain an inverter employing DDCC, simply it can be obtained by using the Y2 terminal as input and Z terminal as output. However, this topology is proper if the following stage has buffered input(s). Otherwise, an additional buffer will be needed. As a simpler form, DDCC based inverting buffer shown in Fig. 11 is used in our design.

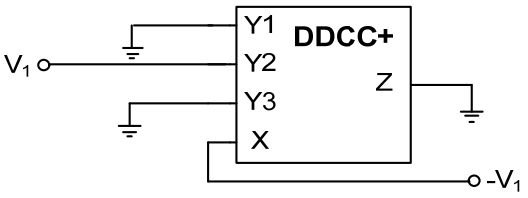

Fig. 11. DDCC based inverting buffer.

4.3.5 Summer

A DDCC is a kind of differential summer circuit due to its characteristic. As the DDCC based summing circuit in Fig. 6, two-input DDCC based topology is used as shown in Fig. 12. In this scheme, by considering differentiated inputs which are applied to Y1 and Y2, the output voltage of the circuit is as follows:

$$V_O = \frac{R_Z}{R_X}(V_1 - V_2) . \tag{20}$$

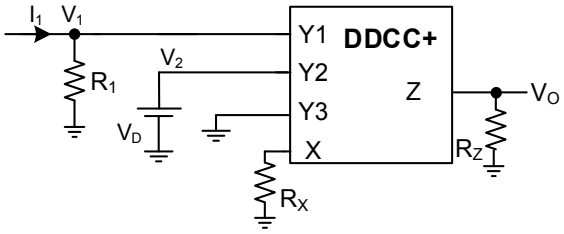

Fig. 12. DDCC based summer topology used in the memristor design.

V_1 corresponds produced voltage from the output current of the previous multiplier with resistor $R_1 = 1.6$ kΩ. V_2 is a DC voltage with the value of $V_D = 135$ mV. It stands for α with scaled a constant. For weighted summation, R_X and R_Z is used with values $R_X = 1$ kΩ and $R_Z = 2.5$ kΩ.

4.4 Single DDCC+ Based Inductance Simulator

Inductors are undesired elements in circuits because of their drawbacks such as in the usage of space, cost and adjustability. They cannot be implemented inside a chip. Actively simulating of the inductors offers appropriate design possibilities and in this sense it is more preferable.

A single CCII+ based inductance simulator was presented by Cicekoglu and Kuntman [30]. Based on this implementation, we have constructed a DDCC+ based new inductance simulator as shown in Fig. 13.

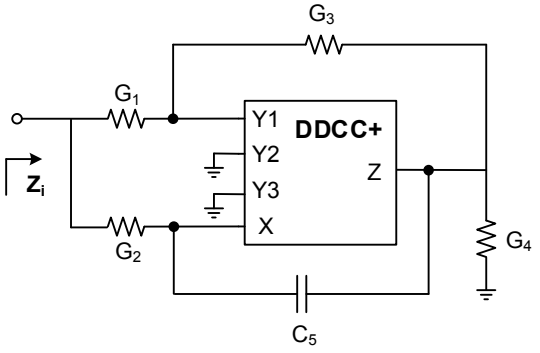

Fig. 13. DDCC based inductance simulator.

By using this topology it is either possible to realize an inductor with series resistance or a lossless inductor. For the grounded inductor with series resistance, equivalent inductance and resistance are defined by

$$L_{eq} = \frac{G_1\left(G_3+G_4\right)+G_3\left(G_4-G_2\right)+2sG_1C_5}{G_3G_4\left(G_1+G_8\right)}, \quad (21)$$

$$R_{eq} = \frac{G_1\left(G_3+G_4\right)+G_3\left(G_4-G_2\right)}{G_3G_4\left(G_1+G_8\right)}. \quad (22)$$

To utilize a lossless inductor, in matching constraint given in (23) the impedance value is obtained as in (24).

$$G_1\left(G_3+G_4\right)=G_3\left(G_2-G_4\right), \quad (23)$$

$$L_{eq} = \frac{2sG_1C_5}{G_3G_4\left(G_1+G_2\right)}. \quad (24)$$

Parameters of inductance simulator are selected as $R_1 = 1.35$ kΩ, $R_3 = 1.35$ kΩ, $R_4 = 1.35$ kΩ, $R_2 = 450$ Ω.

4.5 CMOS Design of DDCC

CMOS design of DDCC± used in this work is shown in Fig. 14. Our DDCC± is constructed based on implementations given in [28], [30]. In the circuit, M1, M2 and M3, M4 are two differential stages. High gain stage is obtained by a current mirror and the differential current is converted to a single-ended output current with the transistors M13, M14, M15. The positive output terminal Z+ is composed with a current source and duplicating elements of the current of the transistor M15 (M8, M9, M16 and M17). At the negative output terminal Z-, the current mirror shaped and the direction of the current is changed by transistors M10, M11, M12 and M18. Offset issue is critical for the multiplier stages in our design. A small DC current has come up at the output of multipliers. It would be solved for multiplier 1 by defining the value of V_D in Fig. 12. However, to systematically get rid of this constant DC current offset, M19 is used.

The supply voltages V_{CC} and V_{SS} are +1.25 V and -1.25 V, respectively. Bias voltages are taken as V_{b1} = -0.34 V and $V_{b2} = 0$. Aspect ratios of all NMOS and PMOS transistors except M19 are $W_N/L_N = 4$ µm / 0.8 µm and $W_P/L_P = 8$ µm / 0.8 µm, respectively. Dimensions of M19 are defined as $W_{M19}/L_{M19} = 20$ µm / 9 µm.

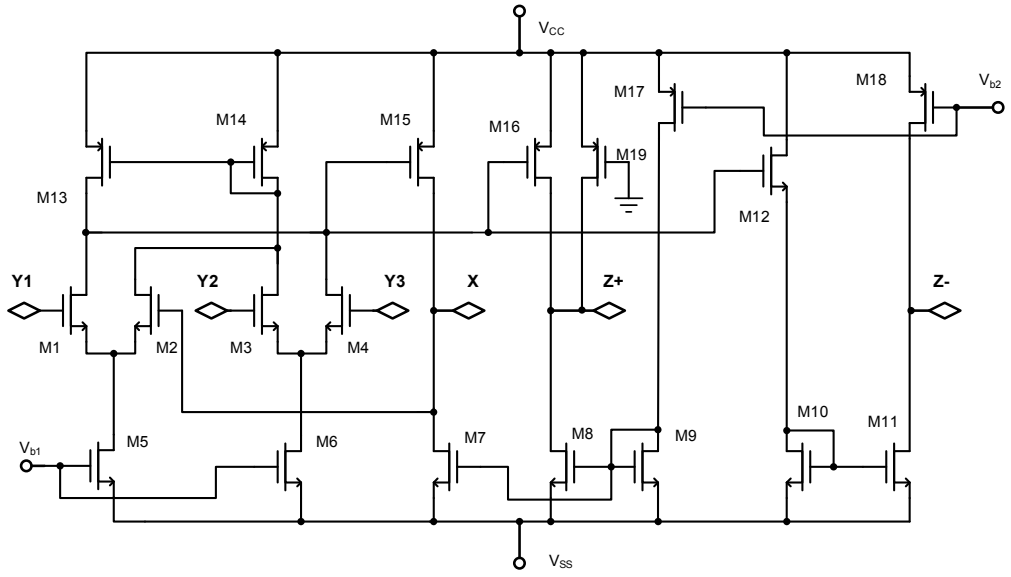

Fig. 14. CMOS circuit schematic of DDCC.

5. Simulation Results

In this section PSPICE simulations of the fully CMOS memristor-based circuit are performed and results are shown. Resistance R in Fig. 1 is still a parameter. It is taken the same as in MATLAB simulations: $R = 1.97$ kΩ. Setting of parameters properly has emerged as a critical issue. In addition to defining of parameters according to the calculations and design constraints, additional adjustments have been carried out by considering characteristics of the whole system.

Time and corresponding frequency domain waveforms and chaotic phase portraits are shown in Fig. 15 and Fig. 16, respectively. Note that the time domain and phase portrait plots obtained from the CMOS circuit exhibit very good visual agreement with corresponding plot in the MATLAB simulations.

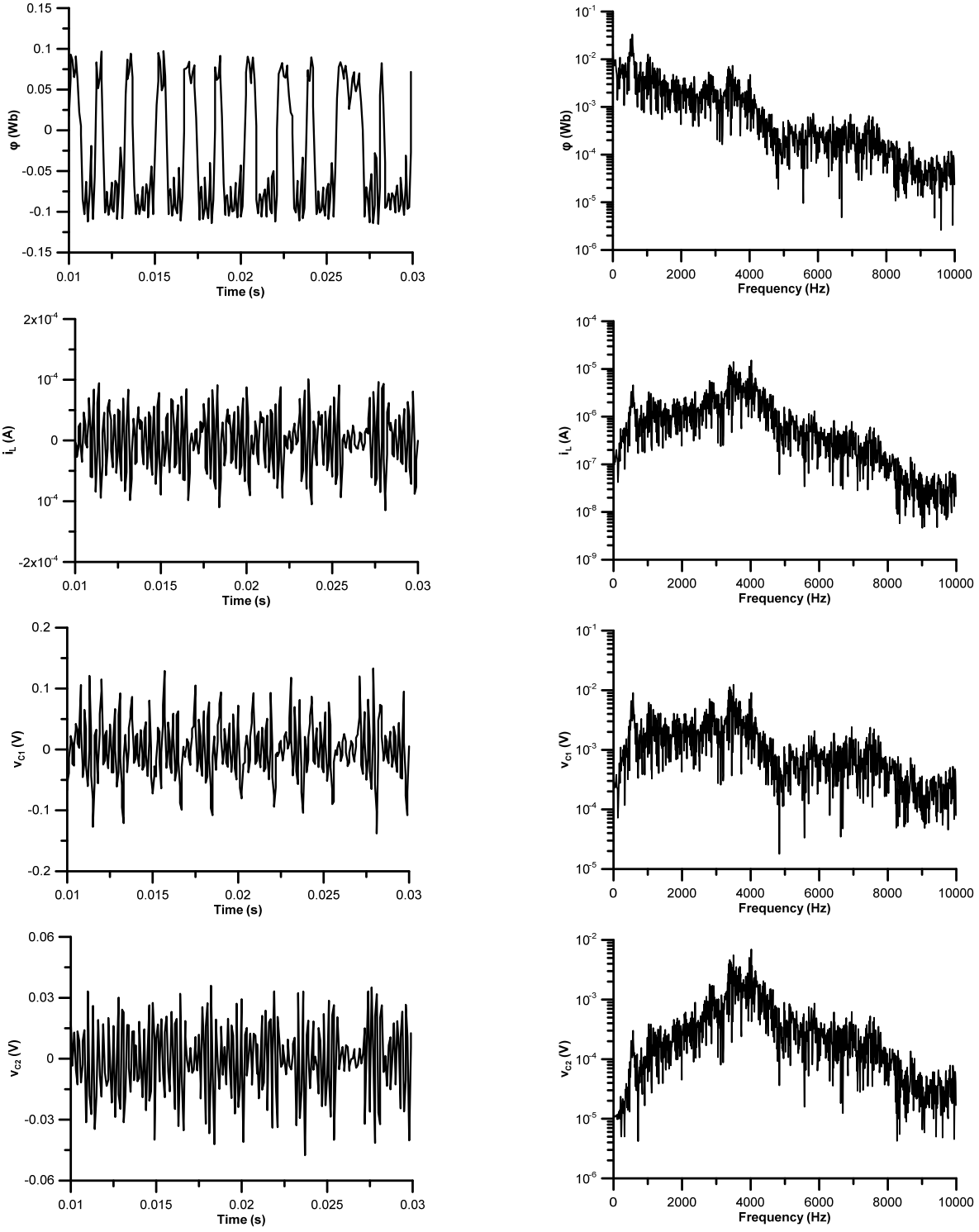

Fig. 15. Time domain waveforms of chaotic signals from SPICE simulations.

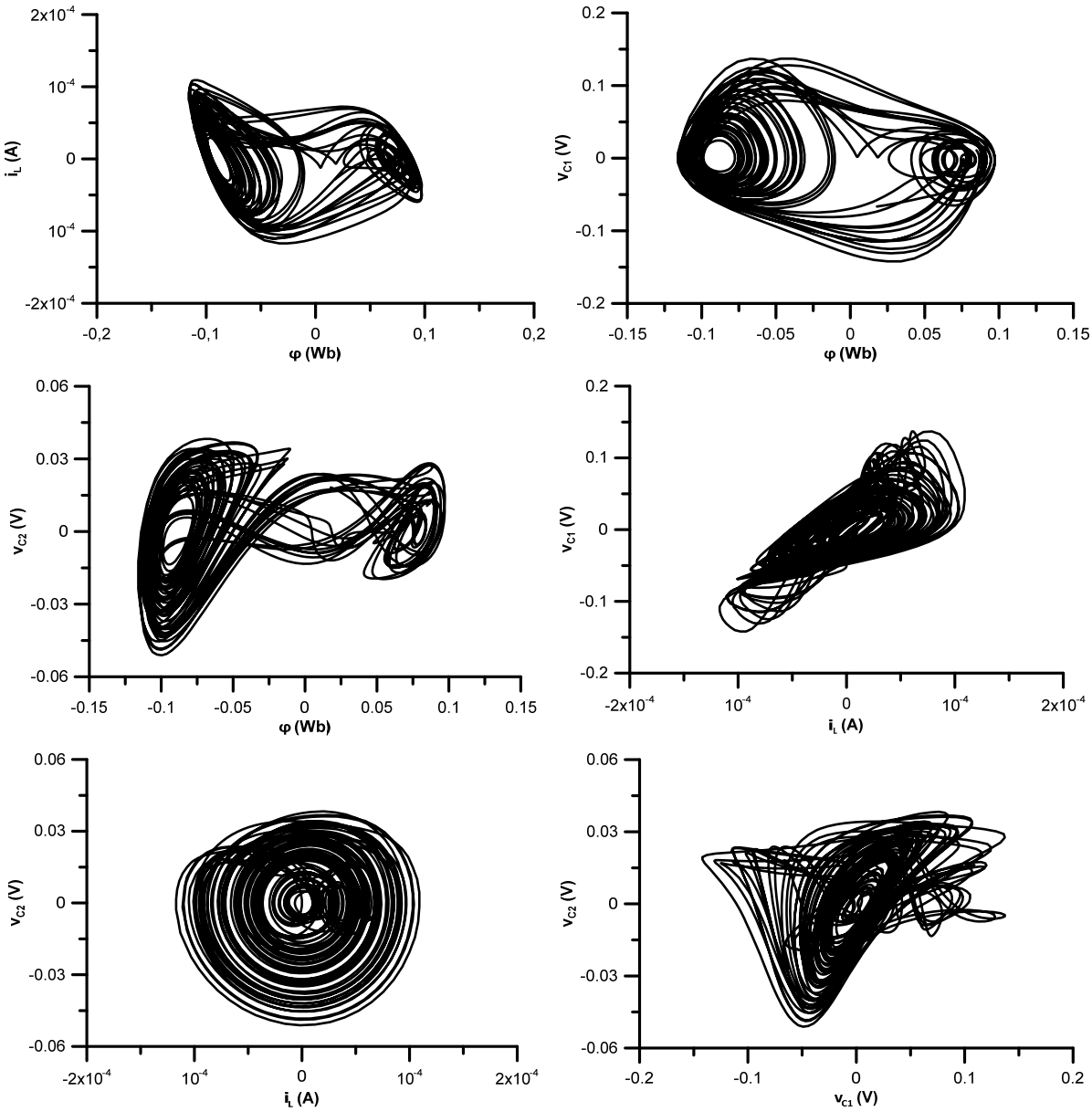

Fig. 16. Phase portraits from the SPICE simulations.

Flux-charge cubic characteristics of the memristor is shown in Fig. 17. Theoretical plot is obtained by using predetermined α and β at the beginning of our design. Experimental characteristics are obtained from CMOS chaotic circuit. From the SPICE simulations, the memductance parameters given in (8), are experimentally redetermined as $\alpha = -0.698 \times 10^{-3}$ and $\beta = 16.987 \times 10^{-3}$.

The total power consumption of the system is determined as 3.2 mW. This indicates a very low level comparing of other traditional op-amp based realizations.

Beyond the prior works and traditional op-amp based implementations, our design is entirely CMOS based and implementable only on a chip. From this perspective, it is obvious that it requires much less area. Along with the current process technology, it promises a considerable reduction in terms of the total number of transistors used in

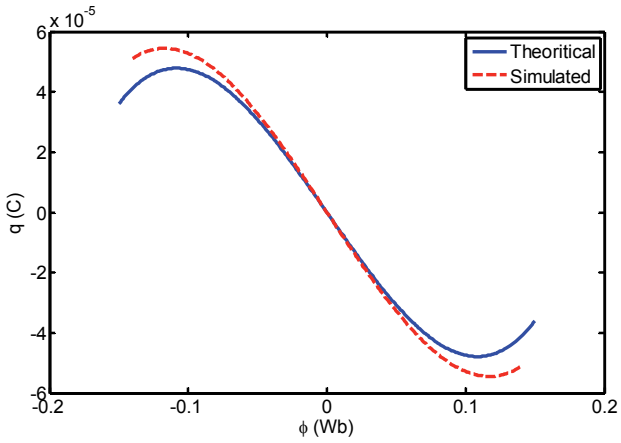

Fig. 17. Theoretical and experimental memristor cubic characteristic curve.

the design even except inductor [8], [26]. Unlike the op-amp based implementations, the proposed circuit can operate over a wide range of frequencies from Hz to MHz levels.

6. Conclusions

In this study, a new fully CMOS memristor-based chaotic Chua's circuit is presented. Memristor is implemented employing only CMOS DDCCs based blocks and therefore suitable to current VLSI processes. In the frame of the work performed, besides a systematically realizable DDCC-only realization approach to a CMOS-only memristor, a new CMOS-only chaotic oscillator is also presented. This design consumes less power and requires less area comparing other traditional realizations.

Simulations performed show that with the memristor model proposed, both memristor characteristics and chaotic behavior of the system is provided accurately. Memristor promises some new features such as reduction in the area used for the same function, lower power consumption etc. Furthermore it can be observed clearly that new possibilities and advantages will be added thanks to its natural non-volatile and non-linear structure. Since there is no physical sample yet, physically based correct modeling and design of the memristor is important. Proper implementations can be used in practical applications. It is possible to use a real physical memristor in this system when it is available.

Memristor can be easily applied to chaotic circuits thanks to its natural nonlinear behavior. It seems reasonable to compose memristor-based chaotic synchronization and chaotic communication applications. In addition it is known that memristors can mimic the behavior of biological synapses. We believe that our implementation and its application to chaotic circuits would benefit the memristor-based chaotic circuits, memristor-based analog signal processing applications.

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