Enhanced Model of Nonlinear Spiral High Voltage Divider

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Abstract. *This paper deals with the enhanced accurate DC and RF model of nonlinear spiral polysilicon voltage divider. The high resistance polysilicon divider is a sensing part of the high voltage start-up MOSFET transistor that can operate up to 700 V. This paper presents the structure of a proposed model, implemented voltage, frequency and temperature dependency, and scalability. A special attention is paid to the ability of the created model to cover the mismatch and influence of a variation of process parameters on the device characteristics. Finally, the comparison of measured data vs. simulation is presented in order to confirm the model validity and a typical application is demonstrated.*

Keywords

High voltage start-up MOSFET, pinch-off, high voltage spiral divider, statistical modeling

1. Introduction

Nowadays, the power consumption is one of the most important integrated circuit parameters. High voltage power start-up MOSFET transistor described in this paper is used to minimize the power consumption [1, 2]. It is designed to provide initial current directly from the high voltage source. This MOSFET transistor charges up the regulator voltage on an external capacitor to about 14 V. The main goal is to minimize power consumption of the circuit that is directly connected to the rectified DC high voltage source. This high voltage can be up to 400 V for a 230 V AC supply and 700 V for switcher applications using power factor correction.

The HV start-up MOSFET is fabricated in an analog 1 μm CMOS technology. The simplified structure of this MOSFET is depicted in Fig. 2. The source and drain are formed from a low-doped Nwell and are contacted by N+ diffusion. The drain drift area contains a floating P doped resurf diffusion (ptop) fabricated before field oxide. The MOSFET channel is created from Pwell not isolated from the P-substrate and it is covered by polysilicon gate. This drain-gate-source structure is rotary symmetrical around vertical axis in the center of the drain. It means that the drain is created in the shape of a circle and the gate and the source in the shape of an annulus.

The drain is located in the center of the device and contains rounded bonding pad. A drain bonding wire is connected directly to this bonding pad and this is only one possible way how the drain can be connected. The oxide breakdown is much lower (about 100 V) than maximum allowed drain voltage. The drain can be biased up to 700 V and this makes integrated direct sensing of the high drain voltage impossible. Hence, the high resistance polysilicon spiral voltage divider is used for sensing of high drain voltage. The spiral is connected to the drain and continues spirally toward the gate. How the polysilicon spiral divider is connected to other device components is depicted in the schematic symbol of HV MOSFET in the Fig. 1 (terminals d, tap1, tap2).

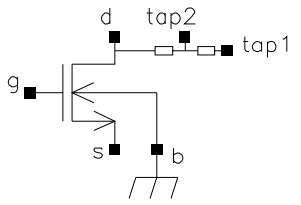

Fig. 1. Schematic symbol of HV start-up MOSFET.

The spiral divider is designed to have the electric field distribution as much similar as possible as the drain drift area under it. This ensures the voltage between divider and silicon does not exceed oxide breakdown voltage. The polysilicon spiral divider has a big impact on a distribution of electric field in low doped drain drift area. And on the contrary, the strong electric field in low doped drain drift area causes a lot of parasitic effects that have a big influence on DC and RF device characteristics. These attributes make the modeling of this start-up MOSFET complicated, especially the divider ratio voltage and frequency dependency. The divider is usually modeled by the simple RC network, but there exist the operation areas where such simple model is not sufficient.

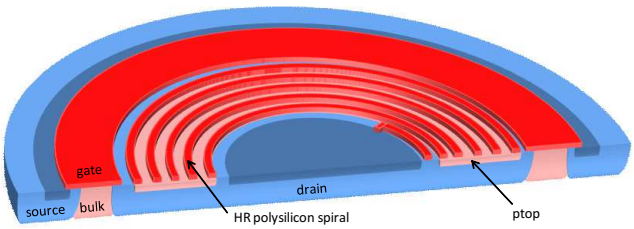

Fig. 2. The simplified 3D structure of HV start-up MOSFET transistor.

2. Spiral Divider Modeling

For the purpose of the equivalent lumped element circuit creation the polysilicon spiral is divided into several separate spiral elements. This division is shown in Fig. 3(a) where each spiral element has a different color. For better lucidity only the first four turns are depicted in this figure. The equivalent 3D circuit in Fig. 3(b) is obtained if these spiral elements are uncoiled to parallel plains. The 3D equivalent circuit in Fig. 3(b) can be redrawn for better lucidity to the 2D equivalent circuit, which is depicted in Fig. 4.

2.1 Spiral Element Length

The spiral divider of the HV MOSFET transistor is a special case of the Archimedes spiral [3]. The radius r of the spiral is increased in one turn by a radius increment Δr. The basic equation defined in polar coordinates for the radius is

$$r = r_0 + \varphi\frac{\Delta r}{2\pi} \tag{1}$$

where r_0 is an initial radius of the spiral and φ is an actual angle circumscribed by the spiral.

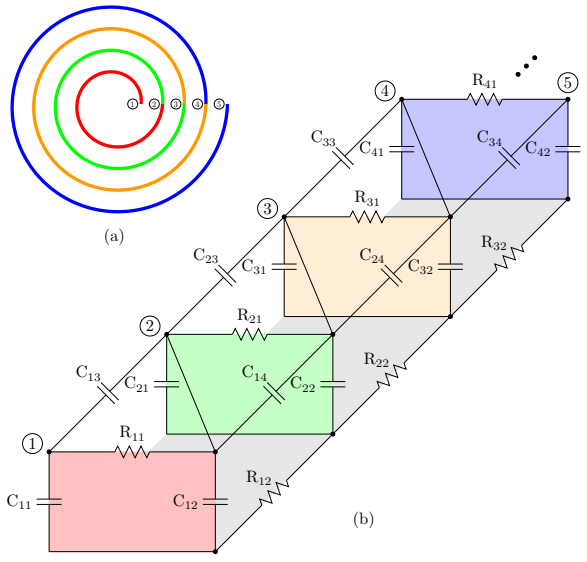

Fig. 3. Equivalent lumped 3D circuit of first four spiral poly subsegments and ptop: (a) colored spiral subsegment, (b) equivalent circuit. Colors from (a) match (b).

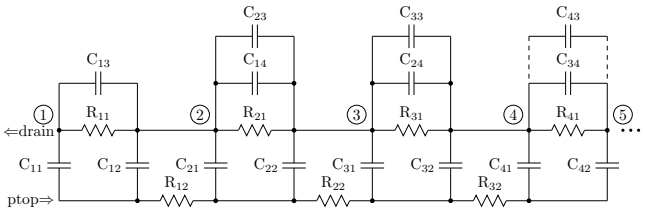

Fig. 4. Equivalent lumped 2D circuit of first four spiral poly subsegments and ptop.

The curve length can be calculated in the following way. If $f(\phi)$ is the function of the curve in polar coordinates (ϕ is an angle) then the length L of the curve is defined as

$$L = \int_0^{\varphi} \sqrt{[f(\phi)]^2 + \left(\frac{\mathrm{d}f(\phi)}{\mathrm{d}\phi}\right)^2}\,\mathrm{d}\phi. \tag{2}$$

For the spiral defined in polar coordinates by (1) the spiral length L is obtained by substituting the equation (1) into (2), and by solving this integral the spiral length is

$$\begin{aligned} L = {} & \frac{\Delta r}{4\pi}\ln\left(\frac{r_0 + \varphi\frac{\Delta r}{2\pi} + \sqrt{\left(r_0 + \varphi\frac{\Delta r}{2\pi}\right)^2 + \frac{\Delta r^2}{4\pi^2}}}{r_0 + \sqrt{r_0^2 + \frac{\Delta r^2}{4\pi^2}}}\right) + \\ & + \left(\frac{r_0\pi}{\Delta r} + \frac{\varphi}{2}\right)\sqrt{\left(r_0 + \varphi\frac{\Delta r}{2\pi}\right)^2 + \frac{\Delta r^2}{4\pi^2}} - \\ & - \frac{r_0\pi}{\Delta r}\sqrt{r_0^2 + \frac{\Delta r^2}{4\pi^2}}. \end{aligned} \tag{3}$$

When $\Delta r << r_0$ then equation (3) can be simplified to

$$L = r_0\varphi + \frac{\Delta r}{4\pi}\varphi^2. \tag{4}$$

2.2 Divider Ratio Modeling

Model of a similar device has been published in [4] but without ratio scalability and statistical modeling. These two important model abilities have been developed and implemented into the new model that is introduced in this paper. The divider ratio is dependent on the drain and source voltage V_D and V_S. The voltage dependency caused by depletion effects in the ptop and nwell layers is modeled by Verilog-A code using nonlinear functions. The increasing of the drain voltage causes the depletion of the ptop and nwell and when the ptop is fully depleted under the spiral polysilicon divider then it causes a change of the ratio voltage dependency slope as is depicted in Fig. 5. The geometrical ratio is based on (4) and can be expressed as

$$\begin{aligned} ratio_{geom} = \frac{L_1 + L_2}{L_2} = \\ = \frac{4\pi r_0(\varphi_{tap1} - \varphi_D) + \Delta r(\varphi_{tap1}^2 - \varphi_D^2)}{4\pi r_0(\varphi_{tap1} - \varphi_{tap2}) + \Delta r(\varphi_{tap1}^2 - \varphi_{tap2}^2)} \end{aligned} \tag{5}$$

where φ_D, φ_{tap1} and φ_{tap2} are drain, tap1 and tap2 angles on the spiral, L_1 and L_2 are long and sensing part of the spiral.

The normalized ratio is modeled as

$$ratio_{norm} = \frac{ratio_{el}}{ratio_{geom}} = \frac{V_D/V_{tap2}}{(L_1+L_2)/L_2} = \\ = \begin{cases} 1+(\beta_{D1}+\beta_{D2})V_D+\beta_S V_S & \text{for } V_D \le V_P \\ 1+\beta_{D2}V_D+\beta_S V_S & \text{for } V_D > V_P \end{cases} \quad (6)$$

where $ratio_{el}$ is electrical ratio, β_{D1}, β_{D2} and β_S are drain and source voltage dependency model parameters, V_D, V_S and V_{tap2} are voltages on pins drain, source and tap2, and V_P is ptop pinch-off voltage. The voltage dependency coefficient β_{D2} is temperature dependent and can be expressed as

$$\beta_{D2} = \beta_{D2Tnom}\left[1+\alpha_D(T-T_{nom})\right] \quad (7)$$

where T is temperature, model parameter β_{D2Tnom} represents value of β_{D2} at nominal temperature T_{nom} and α_D is temperature coefficient.

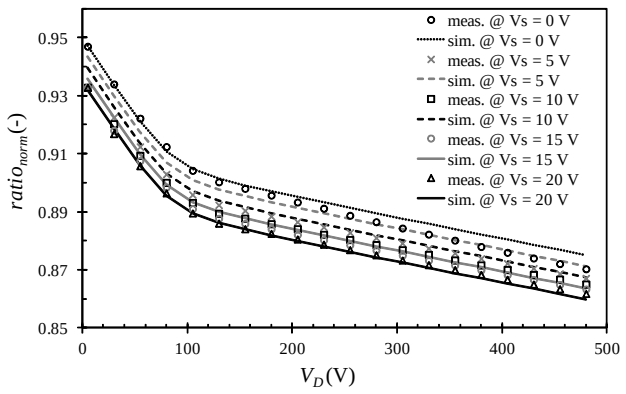

Fig. 5. Drain and source voltage dependency of normalized ratio.

The model is scalable by an editable model argument $ratio_{geom}$ that is refined to

$$ratio'_{geom} = \left(ratio_{mult}\, ratio_{geom} - ratio_{\Delta}\right)\delta_{ratio} \quad (8)$$

where $ratio_{mult}$ and $ratio_{\Delta}$ are model fitting parameters for ratio scalability and δ_{ratio} is relative statistical mismatch model parameter.

2.3 Divider Dynamical Modeling

The AC response is modeled by a distributed RC network. The magnitude and phase of the normalized ratio are depicted in Figs. 6 and 7. The AC measurement setup is described in Appendix. The full macromodel circuit of HV start-up MOSFET is shown in Fig. 12.

The high resistance polysilicon spiral segments are modeled by the Verilog-A code. Each resistor segment is modeled as

$$R_{seg} = \frac{R_{tot}}{N_{seg}}\left(1-\frac{1}{ratio_{norm}\, ratio'_{geom}}\right) \quad (9)$$

where N_{seg} is number of divider segments (excluding sense segment), R_{tot} is total spiral divider resistance and is calculated as

$$R_{tot} = \frac{R_{SH}\, L_{tot}\left(1+\alpha_{p1}\Delta_T+\alpha_{p2}\Delta_T^2\right)}{W+\delta_W} \quad (10)$$

where R_{SH} is polysilicon spiral sheet resistance, L_{tot} is a total spiral divider length, $\Delta_T = T - T_{nom}$, W is spiral segment width, δ_W is absolute statistical process model parameter, α_{p1} and α_{p2} are temperature coefficients dependent on R_{SH}

$$\begin{aligned} \alpha_{p1} &= \alpha_{rsh1}R_{SH}+\alpha_{rp1} \\ \alpha_{p2} &= \alpha_{rsh2}R_{SH}+\alpha_{rp2} \end{aligned} \quad (11)$$

where α_{rsh1}, α_{rsh2}, α_{rp1}, and α_{rp2} are polysilicon temperature coefficients. The resistance of the sense segment is

$$R_{sense} = \frac{R_{tot}}{ratio_{norm}\, ratio'_{geom}}. \quad (12)$$

The capacitances are modeled by the Verilog-A code and are voltage dependent similarly as resistances. The voltage dependency is caused by depleting effects of very low doped drift drain area due to the high electric field. Each capacitor segment is modeled [4] as

$$C_{seg} = \frac{C_{tot}}{N_{seg}}\left(\frac{1}{\pi}\arctan\left(\frac{V_P-V_D}{2}\right)+c_P\right) \quad (13)$$

where c_P is the pinch-off capacitance coefficient model parameter and C_{tot} is total spiral divider capacitance and is calculated as

$$C_{tot} = L_{tot}(W+\delta_W)C_{pa}+2L_{tot}C_{fr}+C_c \quad (14)$$

where C_{pa} is polysilicon (field oxide) capacitance per unit area, C_{fr} is fringe capacitance per length and C_c is capacitance model fitting parameter.

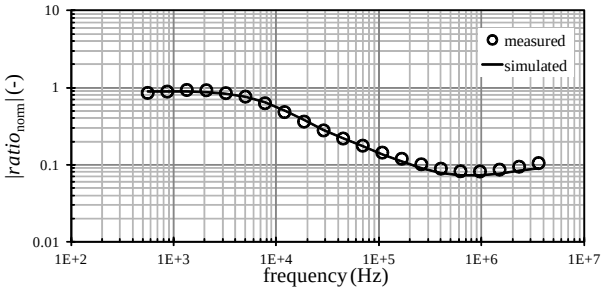

Fig. 6. Magnitude of normalized divider ratio.

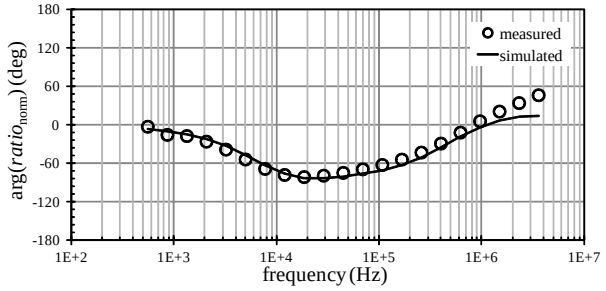

Fig. 7. Phase of normalized divider ratio.

2.4 Divider Statistical Modeling

This HV start-up MOSFET was placed on process control monitoring test chip where this device is measured on each fabricated wafer in a standard production. Data from this test chip are used for statistical process control and also for statistical modeling.

The mismatch modeling [5], [6] is implemented only to the divider ratio. The parameter δ_{ratio} is relative statistical mismatch model parameter and is defined as

$$\delta_{ratio} = 1 + \sigma_{ratio} \cdot VAR_{MATCH\_RATIO} \tag{15}$$

where σ_{ratio} is relative standard deviation of the divider ratio and VAR_{MATCH_RATIO} is random variable of mean 0 and standard deviation 1 that represents the normalized Gaussian distribution for modeling the stochastic variations. The histogram of measured and simulated voltage V_{tap2} and box plot are depicted in Figs. 8 and 9 (one lot typically contains from 20 to 30 wafers and one wafer typically contains 5 test chips). The number of measured devices was 3825. The standard deviation σ_{ratio} is equal to the standard deviation of measured electrical parameter V_{tap2} at $V_D = 100\,\mathrm{V}$, $V_S = V_G = V_{tap1} = 0\,\mathrm{V}$.

The influence of process parameters variation on the device parameters is implemented through master variables by using mapping equations:

$$R_{SH} = R_{SH\_nominal} + \sigma_{RSH} \cdot VAR_{RSH}, \tag{16}$$

$$\delta_W = \delta_{W\_nominal} + \sigma_{DW} \cdot VAR_{DW}, \tag{17}$$

$$C_{pa} = C_{pa\_nominal} + \sigma_{CPA} \cdot VAR_{CPA}, \tag{18}$$

$$C_{fr} = C_{fr\_nominal} + \sigma_{CFR} \cdot VAR_{CFR}, \tag{19}$$

where $R_{SH\_nominal}$, $\delta_{W\_nominal}$, $C_{pa\_nominal}$ and $C_{fr\_nominal}$ are nominal values, σ_{RSH}, σ_{DW}, σ_{CPA} and σ_{CFR} are the standard deviations, and VAR_{RSH}, VAR_{DW}, VAR_{CPA} and VAR_{CFR} are master random variables of mean 0 and standard deviation 1 that represents the normalized Gaussian distribution for modeling the stochastic variations.

As an example, the histogram of measured and simulated electrical process parameter DW is depicted in Fig. 10 and the box plot in Fig. 11. The number of measured devices was 29257. The standard deviations of device parameters σ_{RSH}, σ_{DW}, σ_{CPA} and σ_{CFR} can be calculated from the standard deviations of these measured electrical process parameters by using forward and backward propagation of variances [7].

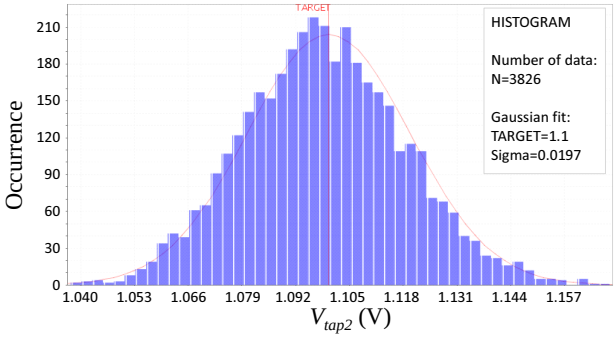

Fig. 8. The histogram of measured and simulated electrical parameter V_{tap2}. The red curve represents modeled Gaussian distribution.

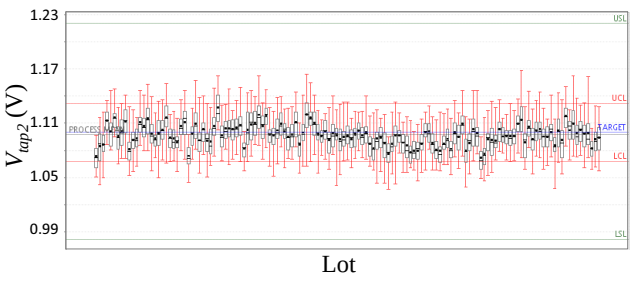

Fig. 9. The boxplot of measured electrical parameter V_{tap2}. The green lines define upper and lower specification limit (USL and LSL) while the red lines define upper and lower control limit (UCL and LCL).

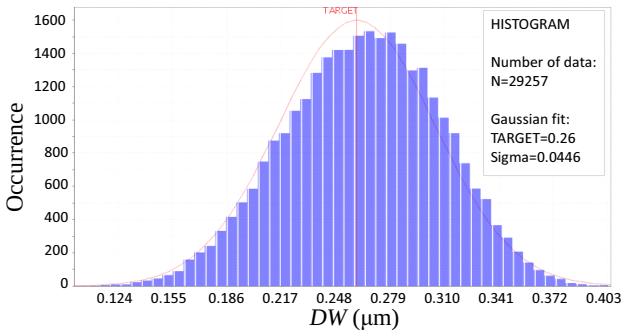

Fig. 10. The histogram of measured and simulated electrical process parameter DW. The red curve represents modeled Gaussian distribution.

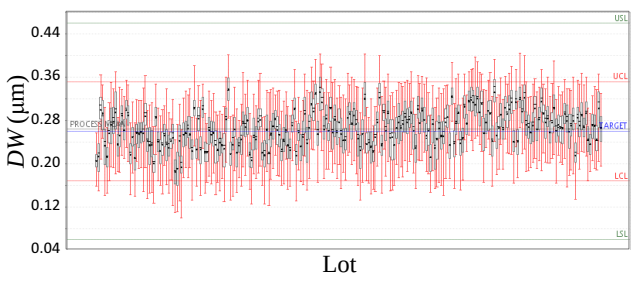

Fig. 11. The boxplot of measured electrical process parameter DW. The green lines define upper and lower specification limit (USL and LSL) while the red lines define upper and lower control limit (UCL and LCL).

3. HV Start-Up MOSFET Application

The AC/DC convertor has been selected as an example of typical application of HV start-up MOSFET with polysilicon spiral divider. The simplified AC/DC convertor circuit is depicted in Fig. 13. The HV start-up MOSFET subblock is modeled by the circuit in Fig. 12 and by the equations introduced in this paper.

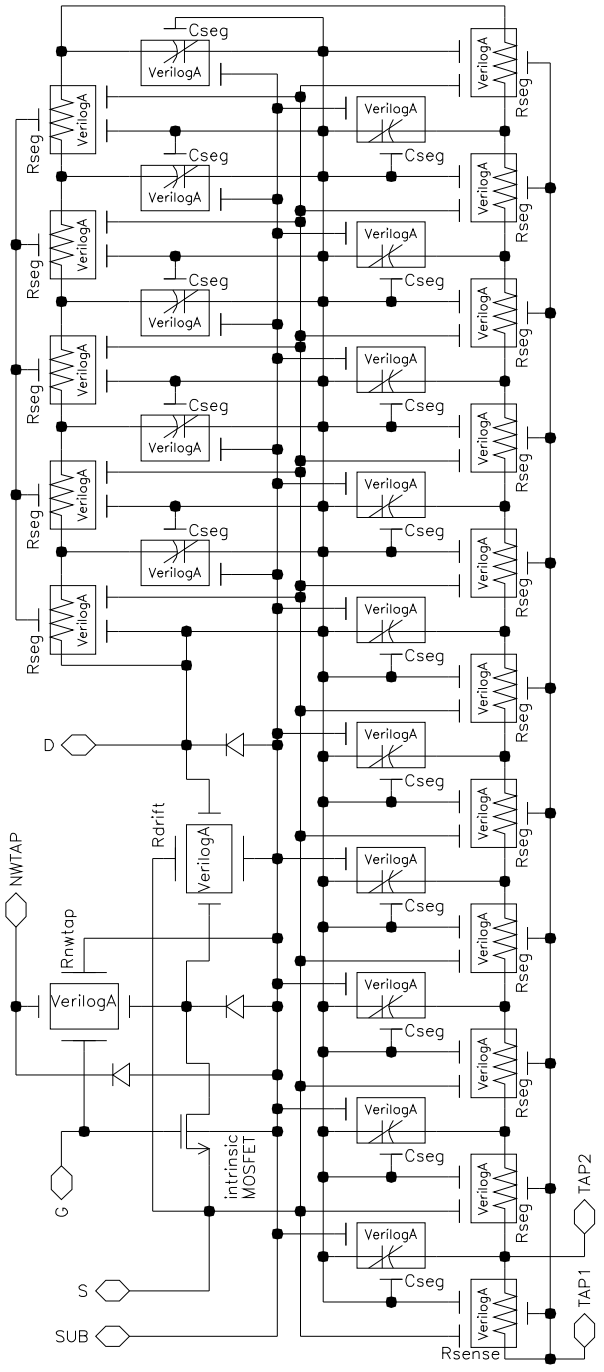

Fig. 12. The full macromodel circuit of HV start-up MOSFET with polysilicon spiral divider.

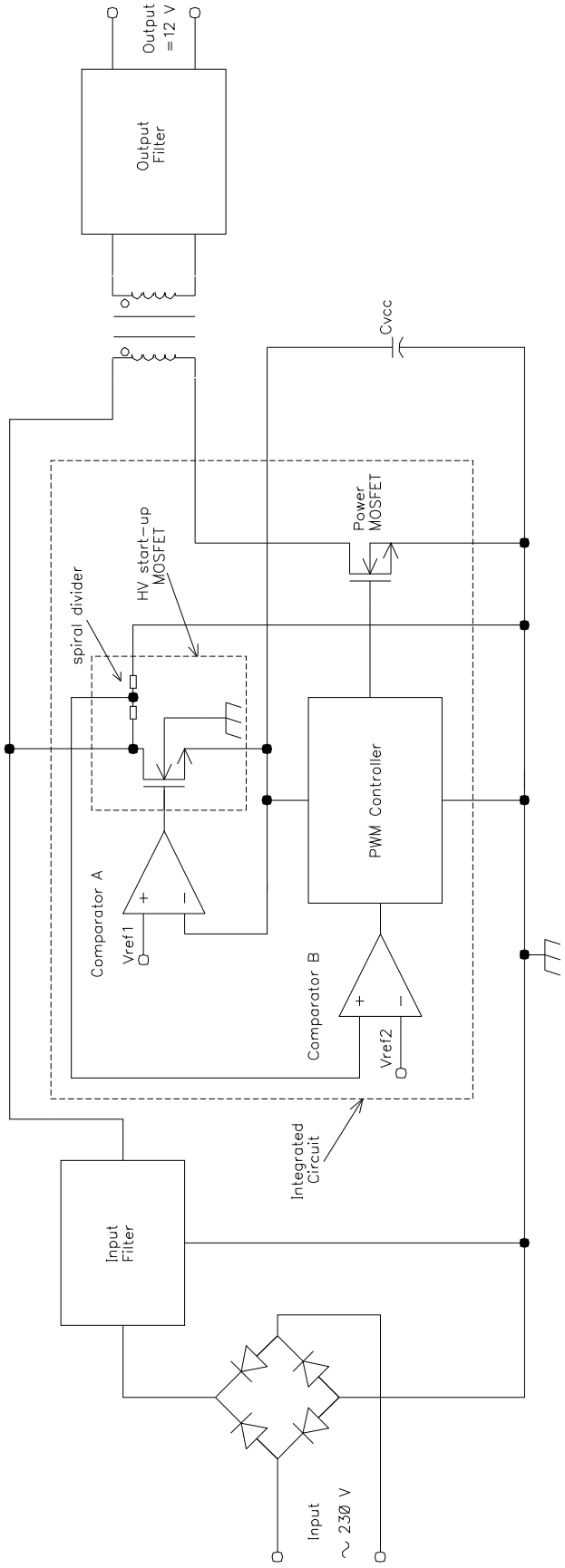

Fig. 13. The simplified circuit of AC/DC convertor. The HV start-up MOSFET subblock is modeled by the circuit in Fig. 12.

The voltage reference V_{ref1} determines the voltage (in Comparator A) to which the external capacitor C_{vcc} is charged up and basically determines the voltage at which the HV start-up MOSFET is switched off. This solution decreases the power consumption in comparison with older solution where the external capacitor C_{vcc} was permanently charged through an external resistor. The solution with HV spiral divider enables to switch off the charging in case the external capacitor C_{vcc} is charged up enough. The voltage reference V_{ref2} determines when the whole AC/DC convertor is switched on based on direct sensing of high voltage by the spiral divider described in this paper. The high input voltage is divided by the spiral divider and compared in Comparator B with the voltage reference V_{ref2}. It means that AC/DC convertor is turned off if the input high voltage is lower than defined value (depends on product specification, e.g. 112 V). See [12] or [13] for more applications.

The circuits that use HV start-up MOSFET with spiral divider allow designing applications with many features such as:

- The dynamic self-supply,
- No need of auxiliary winding [13],
- Low standby-power,
- High voltage sensing,
- Brown-out protection [12],
- Line overvoltage protection [12].

4. Conclusions

The enhanced accurate DC and RF model of nonlinear spiral polysilicon voltage divider in high voltage start-up MOSFET transistor has been created and is presented in this paper. The modeling results are compared with measured data and the maximal relative model error of divider ratio is less than 1.1 %. The intrinsic MOSFET is modeled by the standard BSIM3v3 model described in [8, 9, 10, 11].

A special attention is paid to the ability of the created model to cover the influence of a variation of process parameters on the device characteristics. The statistical process variation model is created based on measurement about 30000 devices and mismatch model is based on measurement about 3000 devices. It has to be pointed out that Monte Carlo simulations represent the most powerful tool to verify the robustness of a designed circuit over natural process and mismatch variations.

The big advantage of this model are smooth derivatives of simulated characteristics. The simulation speed is acceptable and any convergency issue was not observed during the verification realized on several real designs.

Appendix

The AC measurement setup is depicted in Fig. 14. The drain is biased to DC 50, 100, 300, and 400 V and through C_{bias} to AC source. Pin tap1 of the spiral is connected to the ground and pin tap2 is measured output. Gate, source and bulk are connected to the ground.

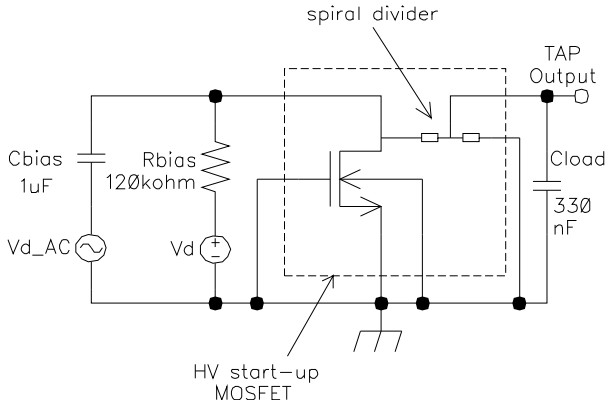

Fig. 14. The AC measurement setup.

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Václav PAŇKO was born in Czech Republic in 1979. He received his bachelor's degree in Electronics and Communications in 2006 and master's degree in Radioelectronics in 2008, both at the Czech Technical University in Prague, where he currently works toward the Ph.D. degree in Radioelectronics. In 2000, he joined ON Semiconductor, where he is presently a Senior Modeling and Characterization Engineer. His main interests include device modeling and parameter extraction, behavioral models development, parasitic effects modeling, and modeling and test chip design tools development.

Stanislav BANÁŠ was born in 1970. He received his M.Sc. degree in Electrical Engineering from the Technical University in Brno in 1994. Last year of his study he spent in scholarship in CNRS institute in Grenoble, where he was interested in optoelectronic properties of hydrogenated amorphous silicon. From 1996 he works as a modeling and characterization engineer in Motorola Czech Design Center in Roznov, later transferred to ON Semiconductor SCG Czech Design Center in Roznov. From 2012 he studies for Ph.D. in Technical University in Prague. His research interests include the modeling of high-voltage semiconductor components.

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