A Wilkinson Power Divider with Harmonic Suppression and Size Reduction using High-low Impedance Resonator Cells

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Abstract. *A miniaturized Wilkinson power divider using high-low impedance resonator cells is designed and fabricated. The proposed power divider occupies 23.7 % of the conventional structure circuit area at the operating frequency of 0.9 GHz and it is also able to suppress harmonics. According to the measured results at 0.9 GHz, the insertion-losses of output ports are 3.087 dB, the return-losses at all ports are more than 30 dB, and the isolation between output ports is better than 35 dB. Also, 2nd to 10th spurious frequencies are suppressed. According to the measured S_{11}, when it is less than -15 dB (from 0.65 GHz to 1.1 GHz) the fractional bandwidth of the proposed structure is 50 %. Good agreement between simulation and measured results is achieved.*

Keywords

Harmonic suppression, high-low impedance resonator, miniaturized Wilkinson power divider

1. Introduction

The power dividers are extremely important devices in microwave and millimeter-wave systems such as mixers, frequency multipliers, and the feeding network for an antenna array. There are several approaches for size reduction and harmonic suppression in the process of designing power dividers. The reported Wilkinson power divider with conventional quarter-wavelength transmission-line (TLIN) in [1], occupies a large area (especially at low operating frequencies) and it is not capable of suppressing spurious frequencies. In order to overcome these disadvantages several methods are used to reduce overall circuit size and suppress unwanted harmonics in the Wilkinson power dividers [2–7]. For instance, for size reduction and harmonic suppression, a kind of Wilkinson power divider based on standard printed-circuit-board (PCB) etching processes is reported in [2]. This structure is designed considering slow-wave loading and reduced the occupied area to 36.5% of the conventional structure at its operating frequency. In [3] and [4], microstrip electromagnetic band-gap (EBG) structure has been applied to the conventional power divider design, which led to the miniaturization and harmonic rejection in the conventional Wilkinson power divider.

Utilizing defected ground structure (DGS) can reject unwanted harmonics and decrease the occupied area in power dividers as it has been reported in [5] and [6]. Since, (DGS) and (EBG) need etching process, so their fabrication process is complex and these methods are not useable on a metal surface. The use of π-equivalent shunt-stub-based artificial transmission lines can effectively decrease the circuit size of conventional power divider [7]. This structure occupies 14.7% of the conventional power divider, but it is not capable for harmonic rejection at its operating frequency of 0.9 GHz.

In this paper, a Wilkinson power divider with harmonic suppression and size reduction is proposed. In order to reduce the circuit size of the conventional Wilkinson power divider, transmission lines with high-low impedance resonators are used instead of conventional quarter-wavelength TLIN sections. This technique not only reduces the occupied area to 23.7% of conventional one at operating frequency of 0.9 GHz, but also suppresses the second up to tenth harmonics.

2. Power Divider Design

2.1 The Procedure of Designing and the Effect of High-low Impedance Resonator on Size Reduction and Harmonic Suppression

Utilizing traditional TLIN in the structure of power dividers results in a large occupied area. Furthermore, this kind of transmission line is not able to suppress spurious frequencies. Using transmission line with loaded capacitance instead of quarter-wavelength transmission-line not only reduces the circuit size, but also can suppress unwanted harmonics. In the first step, a conventional Wilkinson power divider with an operating frequency at 0.9 GHz

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is designed as it is shown in Fig. 1a. In order to make capacitor loading on each $\lambda/4$ TLIN, four resonators with primary dimensions of W1 = W2 = 0.1 mm, L1 = L2 = 0.1 mm, W3 = 0.1 mm and L3 = 0.1 mm are added inside the free area of the conventional structure. These values are selected to control the effects of changing dimensions on frequency response and determine the operating frequency. The locations of the added resonators are determined with a, b, c and d in Fig. 1b. By increasing the values of W1, W2, L1 and L2 as low impedance TLINs a large loaded capacitance can be obtained. In order to reduce the occupied area of the power divider, the length of the main TLIN can decrease simultaneously, with increasing the dimensions of low impedance TLINs. Note that changing the values of variables does not have to shift the desired operating frequency, i.e. 0.9 GHz. Furthermore, adding these resonators makes a lowpass filter on the each main transmission line of the designed circuit. It appears in the insertion loss (S21), because of high order harmonics suppression in the frequency response.

The proposed power divider at 0.9 GHz and its equivalent circuit using lumped components are shown in Fig. 2a and Fig. 2b, respectively. In Fig. 2b L_b, L_c and L_d are equivalent inductors caused by the main transmission line. High-low impedance resonators are modeled by L_a, $C1$ and $C2$, where L_a determines high impedance transmission lines of these resonators. $C1$ and $C2$ show low impedance open-circuit transmission lines of resonators 1 and 2, respectively. The gaps g_1, g_2 and g_3 between low impedance open-circuit lines cause coupling effects, which are modeled by C_{g1}, C_{g2} and C_{g3}. Furthermore, C_{p1} and C_{p2} present the capacitance between the microstrip structure and the ground. *Lout* accounts for inductor of output transmission lines. Notice that the coupling capacitances between the main transmission line and open-circuit transmission lines are not included in the LC circuit as they are trivial.

Open-stub loads in the structure of high-low impedance resonators of the proposed power divider, modeled by $C1$ and $C2$ lead to a large shunt capacitance. Therefore, the circuit size of the proposed Wilkinson power divider could reduce because the propagation constant, i.e. β enhances (βproposed/βconventional is about 1.923). The relationship for β is given by:

$$\beta = \omega\sqrt{LC}\ , \tag{1a}$$

$$\beta = \frac{2\pi}{\lambda_g} \tag{1b}$$

where in (1a) L is the total inductance in per length unit of the main transmission line and high impedance line, and C depicts the total capacitance in per length unit of the main transmission line. In (1b) λ_g determines guided wavelength. Since C (the capacitance of proposed power divider) is increased in comparison with the transmission line of a conventional power divider, the propagation constant is enhanced considerably. As a result, the occupied area of circuit will be decreased [1].

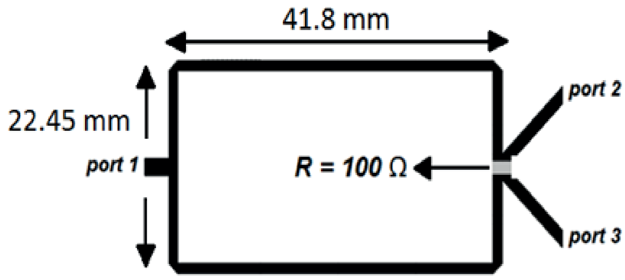

Fig. 1a. Topology of conventional Wilkinson power divider at operating frequency equal to 0.9 GHz.

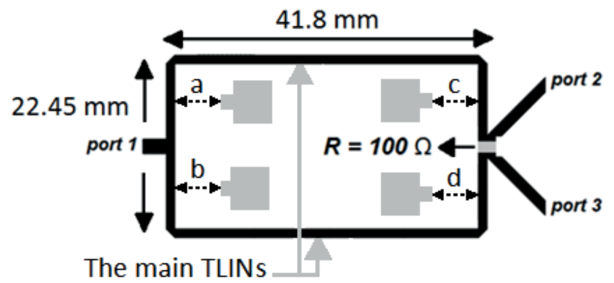

Fig. 1b. Topology of conventional Wilkinson power divider at operating frequency of 0.9 GHz with the locations of added high-low impedance resonators.

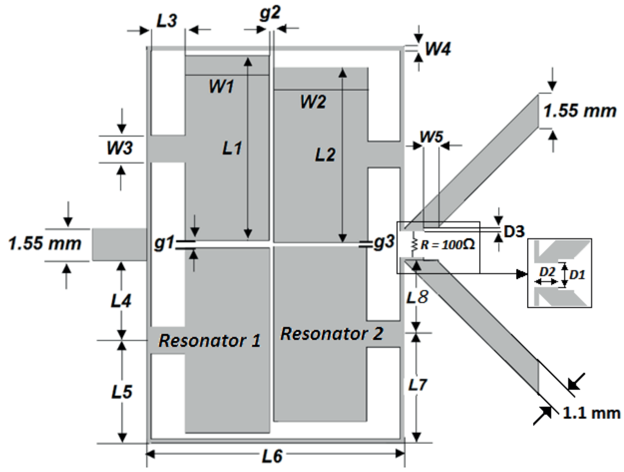

Fig. 2a. Topology of the proposed Wilkinson power divider.

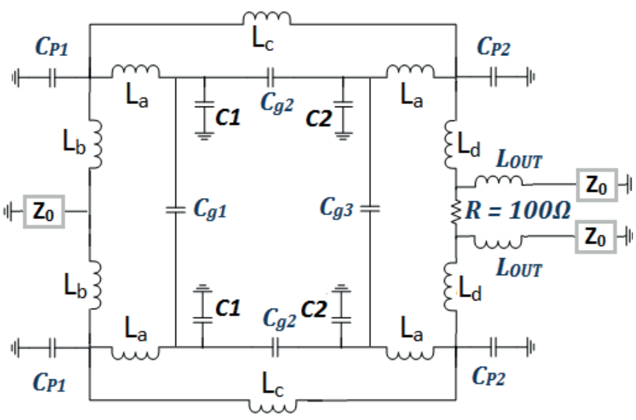

Fig. 2b. Equivalent LC circuit of the proposed Wilkinson power divider.

Moreover, based on insertion loss (S21) of the proposed structure shown in Fig. 6, optimized transmission line with high-low impedance resonators in higher frequencies has features of a lowpass filter. Spurious resonant frequencies of the resonator have been shifted by the high-low impedance resonators from the integer multiples of the basic resonant frequency [1]. So, replacing conventional quarter-wavelength transmission-line with a transmission line loaded by the high-low impedance resonators leads to harmonic suppression.

2.2 The Structure of the Proposed Power Divider

Comparison between the topology of conventional power divider in Fig. 1a and the proposed design, illustrated in Fig. 2a shows that in the proposed power divider, four microstrip high-low impedance resonator cells are used within the free area of the conventional Wilkinson power divider. The low impedance patches with rectangular shapes are microstrip open-stubs, so each of the high-low impedance resonator cells refers to a loaded capacitor. As a result, the capacitor loading not only reduces the circuit size, but also can suppress spurious frequencies.

The designed resonators, i.e. resonators 1 and 2 in both sides (left and right) have the same structure, but their rectangular patches have different dimensions. The circuit size of the proposed power divider and the conventional structure are 18.55 mm × 12 mm and 41.8 mm × 22.45 mm, respectively. It shows that the occupied area is reduced to 23.7% of the conventional power divider at operating frequency of 0.9 GHz. The type of the used 100 Ω isolation resistor is 0603, which is placed between two output ports. The dimensions of the proposed power divider shown in Fig. 2a are: W1 = 3.9, W2 = 4.3, W3 = 1.2, W4 = 0.2, W5 = 0.66, D1 = 1.15, D2 = 1.1, D3 = 0.2, L1 = 8.6, L2 = 8.2, L3 = 1.6, L4 = 3.7, L5 = 4.8, L6 = 12, L7 = 5.1, L8 = 3.4, g1 = 0.3, g2 = 0.2 and g3 = 0.15 (all in millimeter). The calculated values of inductors and capacitors of the shown LC circuit in Fig. 2b are [8]: La = 0.438 nH, Lb = 1.838 nH ,Lc = 12.38 nH, Ld = 1.68 nH, C1 = 1.36 pF, C2 = 1.43 pF, Cg1 = 25 fF, Cg2 = 128 fF, Cg3 = 42 fF,Cp1 = 0.471 pF, Cp2 = 0.466 pF. Note that the values of Cg1, Cg2 and Cg3 are achieved by tuning. Comparison between LC simulation and EM simulation results of the shown circuits in Figs. 2a and b on a substrate with permittivity of 2.2, thickness of 0.508 mm and loss tangent of 0.0009 are depicted in Figs. 3-6.

3. Simulated and Measured Results

The measured and simulated results of the proposed power divider are accomplished using Agilent's ADS Electromagnetic simulator (EM Simulator) software and HP 8720B vector network analyzer, respectively. The operating frequency of the proposed structure is located at 0.9 GHz. The designed microstrip Wilkinson power

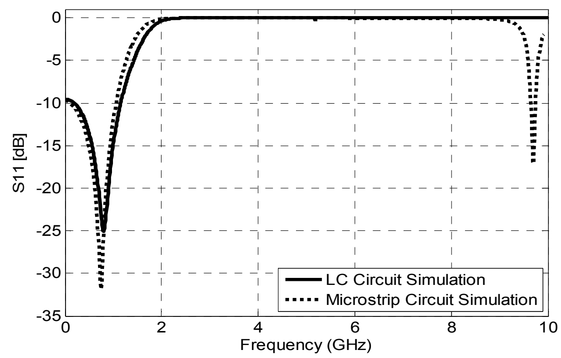

Fig. 3. Comparison between LC simulation and EM simulation results of input return-loss.

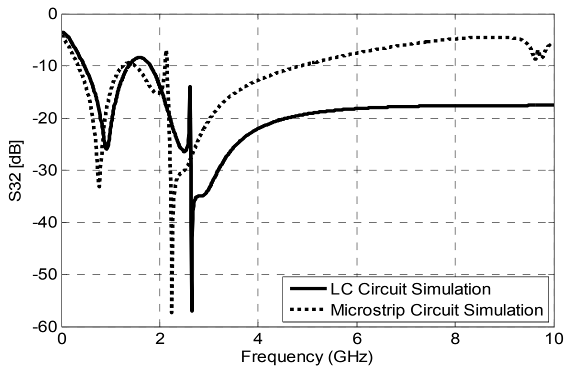

Fig. 4. Comparison between LC simulation and EM simulation results of isolation.

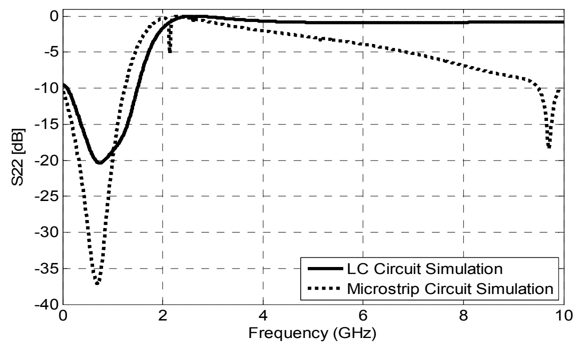

Fig. 5. Comparison between LC simulation and EM simulation results of output return-loss.

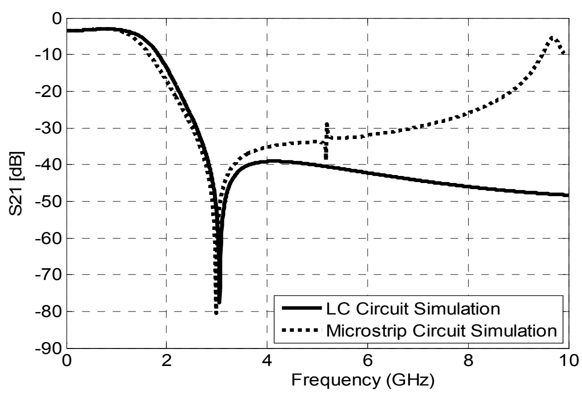

Fig. 6. Comparison between LC simulation and EM simulation results of insertion-loss.

divider is fabricated on RT/Duroid 5880 substrate with the thickness of 0.508 mm, the permittivity of 2.2 and the loss tangent of 0.0009. The results of measurement and simulation of S-parameters are illustrated in Figs. 7–11. As it is shown in Fig. 7, the measured return loss (S11) is at least –15 dB from 0.65 GHz to 1.1 GHz. In Fig. 8, the measurement shows over the frequency range 0.66–1.12 GHz the isolation (S23) is better than –15 dB. According to Fig. 9, the output return loss (S22) less than –15 dB from 0.28 GHz to 1.25 GHz is achieved. It can be observed from the measured insertion loss (S21) in Fig. 10, both even and odd spurious harmonics from 1.8 GHz to 9 GHz, i.e. second to tenth harmonics have been suppressed, where the 3rd to 10th harmonics are suppressed with a level less than –20 dB and the second harmonic is suppressed with a level better than -11 dB. It is to be noted that the suppression of higher order harmonic frequencies is related to S21 and S31. Exactly at operating frequency equal to 0.9 GHz, the measured S11, S32, and S22 are –33 dB, –38.88 dB and –48 dB, respectively. Furthermore, the measured insertion loss shows that S21 at 0.9 GHz is –3.087 dB. The characteristic impedance of all three ports are 50 Ω. Tab. 1 shows the comparison between the proposed power divider and the other published works. Based on the results of measurement shown in Fig. 11, an appropriate phase performance between two output ports around operating frequency is achieved. The measured phase difference of ports 2 and 3 as output ports is ± 0.15°. It shows that the proposed Wilkinson power divider is symmetric, so |S21| = |S31| (thus, harmonic suppression is related to both S21 and S31) and |S22| = |S33|. The photograph of the proposed Wilkinson power divider is shown in Fig. 12.

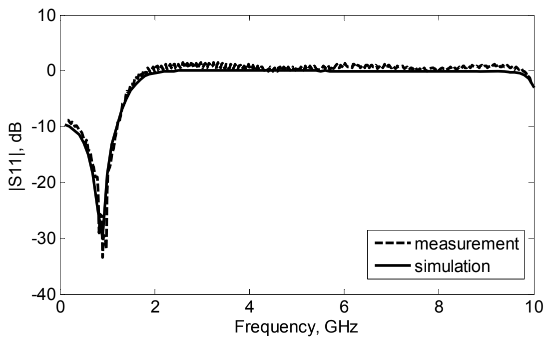

Fig. 7. Simulated and measured input return-loss.

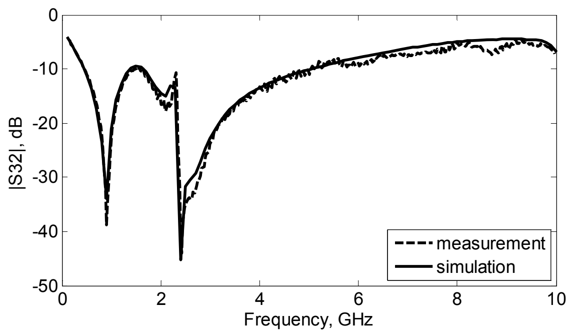

Fig. 8. Simulated and measured isolation.

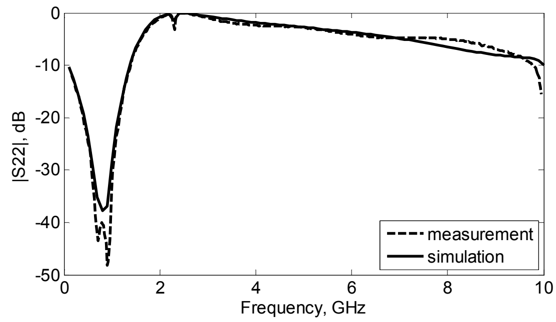

Fig. 9. Simulated and measured output return-loss.

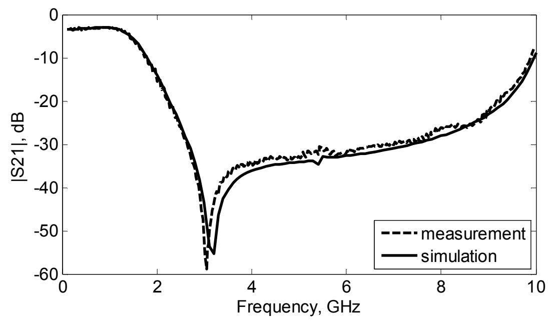

Fig. 10. Simulated and measured insertion-loss.

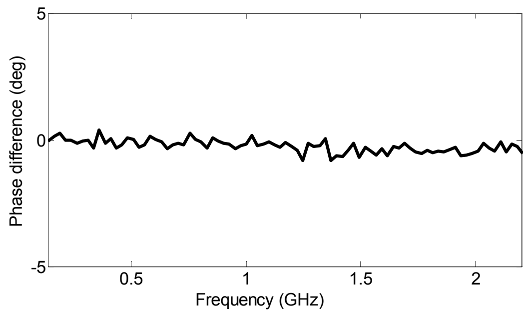

Fig. 11. Measured phase difference between S21 and S31 of the proposed power divider.

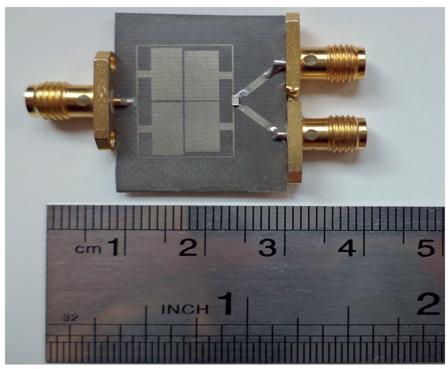

Fig. 12. Photograph of the proposed structure.

4. Conclusion

In this paper, a Wilkinson power divider using high-low impedance resonator cells for harmonic suppression and size reduction is proposed. The key features of the proposed structure are:

Ref.	Area reduction	Harmonic suppression (dB)								
		2nd	3rd	4th	5th	6th	7th	8th	9th	10th
[2]	63%	13	29	32	34	-	-	-	-	-
[3]	70%	8	32	10	12	-	-	-	-	-
[4]	39%	26	25	-	-	-		-	-	-
[5]	10%	18	15	-	-	-		-	-	-
[6]	66%	13	35	-	-	-		-	-	-
[7]	85.3%	-	-	-	-	-		-	-	-
This work	76.3%	11.3	31.5	35.5	33.2	32.4	30.1	25.9	25.9	22.4

Tab. 1. Comparison between the performance of the proposed power divider and previous works.

1- Small occupied area, i.e. 18.55 mm × 12 mm at the frequency of 0.9 GHz;

2- At operating frequency low insertion-losses of output ports (3.087 dB) and more than 30 dB return-losses at all ports are obtained. Moreover, better than 35 dB isolation and ±0.15° phase difference between output ports are achieved;

3- In the proposed structure spurious frequencies from 1.8 GHz up to 9 GHz, i.e. second to tenth harmonics are suppressed.

Therefore, the designed circuit with its operating frequency at 0.9 GHz can be used, where a power divider with small size and capable of suppress harmonics is required.

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