

# A 1.2 V and 69 mW 60 GHz Multi-channel Tunable CMOS Receiver Design

Ahmet ONCU

Dept. of Electrical and Electronics Engineering, Bogazici University, Istanbul, 34342, Turkey

ahmet.oncu@boun.edu.tr

**Abstract.** A multi-channel receiver operating between 56 GHz and 70 GHz for coverage of different 60 GHz bands worldwide is implemented with a 90 nm Complementary Metal-Oxide Semiconductor (CMOS) process. The receiver containing an LNA, a frequency down-conversion mixer and a variable gain amplifier incorporating a band-pass filter is designed and implemented. This integrated receiver is tested at four channels of center frequencies 58.3 GHz, 60.5 GHz, 62.6 GHz and 64.8 GHz, employing a frequency plan of an 8 GHz-intermediate frequency (IF). The achieved conversion gain by coarse gain control is between 4.8 dB and 54.9 dB. The millimeter-wave receiver circuit is biased with a 1.2 V supply voltage. The measured power consumption is 69 mW.

## Keywords

60 GHz, CMOS, integrated circuit, receiver design, low-power

## 1. Introduction

Research on the Complementary Metal-Oxide Semiconductor (CMOS) millimeter-wave transceiver operating at 60 GHz has been driven by the availability of the unlicensed bands in many countries, including Europe (57 ÷ 66 GHz), the United States (57 ÷ 64 GHz) and Japan (59 ÷ 66 GHz) as shown in Fig. 1. The available 9 GHz wide millimeter-wave band is also divided into approximately 2 GHz wide four sub-channels. This has resulted in many enabling design blocks and various modeling techniques reported in the literature [1–5]. Potential applications include low-power short-distance consumer applications such as wireless High-Definition Multimedia Interface (HDMI) for high-definition television (HDTV) video streaming and high data-rate wireless personal area networks. The distance limit is due to the 60 GHz electromagnetic waves being attenuated more as a result of oxygen absorption than at other frequencies. However, taking advantage of the wider multi-gigahertz bandwidth, short-distance applications can allow high data rates while allowing more frequency reuse in a limited area with minimal interference. A consequence is that the system offers

higher security since signals cannot travel far beyond the intended recipients. The motivation of this work is to develop further such a system using the CMOS process technology. Traditional developments of the 60 GHz system have been largely confined to process technologies such as GaAs or SiGe. With price-sensitive services, lower production cost and possible integrations consumer electronics driving developments, CMOS technology offers the advantages of an accessible foundry with the digital baseband. The present state-of-the art CMOS process nodes at sub-100nm demonstrate device  $f_t$  that exceeds 400 GHz [6], thereby providing reasonable gain and other design margins for 60 GHz systems.

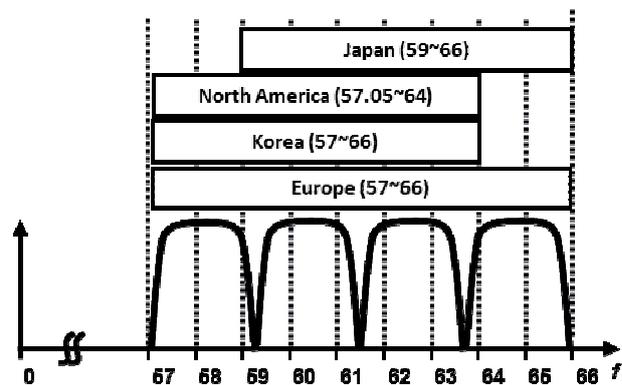


Fig. 1. Worldwide 60 GHz regulations with sub-channels.

A critical building block in the 60 GHz system is the millimeter-wave receiver, which includes the low-noise amplifier (LNA), down conversion mixer, band-pass filter and variable gain amplifier. In this work, a wideband CMOS receiver circuit that covers all 60 GHz bands and selects the sub-channels is proposed. In the following sections the design of the proposed receiver circuit and the performance of the implemented receiver are presented.

## 2. Design of Wideband Receiver

A block diagram of the proposed multi-channel tunable receiver based on the enhanced wide-band LNA is shown in Fig. 2. The receiver consists of an LNA, down-conversion mixer, an intermediate frequency (IF) variable gain amplifier (VGA) integrating a band-pass filter (BPF)

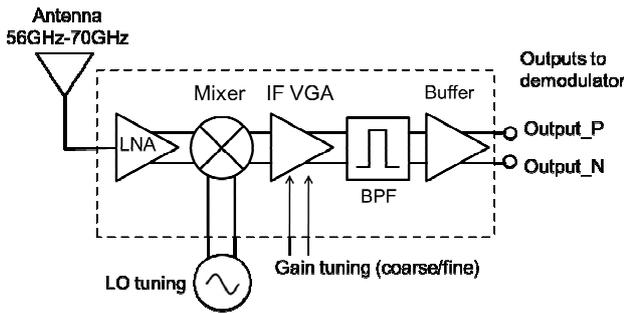


Fig. 2. Proposed receiver architecture.

and an output buffer. To test the performance of the proposed receiver chain, LO signal is externally applied, but in a practical application local oscillator will be implemented on the chip. A wideband LNA with active balun in the first stage to cover the all 60 GHz bands as reported in [9] is designed for this multi-channel receiver. Its schematic is shown in Fig. 3.

The LNA contains an internal balun. It has a single ended input and two outputs with 180° phase difference. The designed wideband LNA has 20 dB gain and 14 GHz bandwidth from 56 GHz to 70 GHz. It covers all 60 GHz bands sub-channels. The noise figure of the LNA is 6.8 dB at 60 GHz.

The main purpose of this receiver is to receive all four sub-channels of the license free 60 GHz bands from 57 GHz to 66 GHz. The LNA can amplify the signals from 56 GHz to 70 GHz frequency range. Therefore it is suitable for our application. The intermediate frequency is chosen as 8 GHz to be able to select the sub-channels and not to have an image rejection filter to have less complex receiver architecture. Since the frequency gap between the desired signal and the image will be 16 GHz, the image signal can be filtered out by the receiver front-end. For lower frequency bands, the image frequency will be far from the receiver's front-end coverage frequency band. When the desired frequency goes higher, image frequency goes closer to the coverage band.

When the receiver receives the 66 GHz signal, the highest frequency of the 60 GHz band sub-channel, the image frequency will be at 49 GHz in the worst case. It is outside of the LNA bandwidth. Therefore, the image frequency will be filtered by LNA. In practical wireless communication, an antenna will be connected to receiver input and it will also contribute to filter out the image signal.

Figure 4 shows the circuit of the implemented mixer. A double-balanced design is realized by the four transistors M10–M13 with each differential set of RF and LO inputs applied 180° out of phase. A modification made to this circuit from the standard Gilbert-cell configuration is the input of the RF signal directly into the source of the MOSFETs, instead of first passing through the gates of common source amplifiers. This current mode interface between the LNA and the mixer alleviates the low headroom limitation of the advanced CMOS process to improve the linearity and high-speed operation with a limited supply voltage

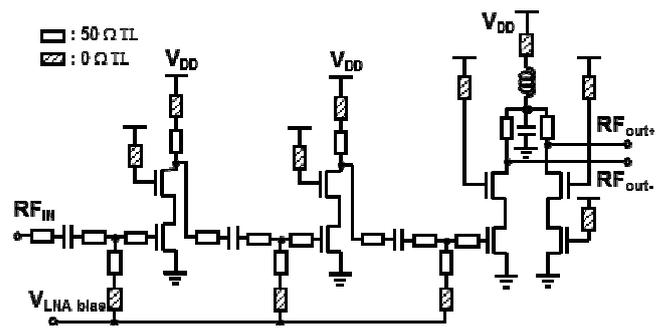


Fig. 3. Schematic of the LNA.

magnitude. A tail current control is then implemented by M9 to provide the appropriate DC current for the differential pairs. To avoid the noise contribution from M9 and its current source, a large bypass capacitance  $C_{bypass}$  is added [16]. Without the capacitor the noise from the M9 and the noise coming from the bias  $V_{b1}$  will inject to the mixer tail current in common mode. Due to the non-idealities in pair transistors, M10–M13, the noise will appear at the mixer output that will reduce receiver the sensitivity. A center tapped inductor shown by L5 and L6 are added to resonate out the parasitic capacitance at the source terminals of M10–M13. Thus, a high input impedance at the RF port from 56 GHz to 70 GHz can be achieved. These inductors can also reduce the signal loss caused by the parasitic capacitances. Inductors L1–L4 are chosen instead of resistors for gain and linearity purposes since an increase in resistance results in a decrease in the voltage headroom at the output node. Thus, there is a trade-off between conversion gain and linearity. In practice, L1–L4 and L5–L6 are implemented as single center-tap inductors in order to save chip area. The inductances L1–L4 and the parasitic capacitances of M10–M13 comprises two resonating tanks. The bandwidth of the tanks is equal to the bandwidth of the mixer. The bandwidth of the tank is narrower than the desired one. Therefore, in this design two resistors R1 and R2 are added to ensure 2 GHz bandwidth at 8 GHz IF center frequency.

In comparison with a conventional mixer, the proposed down-conversion mixer aims to achieve lower noise

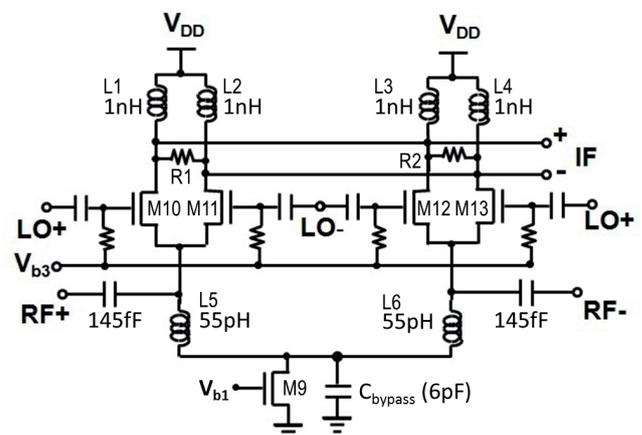


Fig. 4. Schematic of the mixer.

because of the absence of the noise generated from the transconductance stage in a conventional mixer. In addition, a DC current through this transconductance stage is not required. Thus the DC current can be reduced to improve the noise performance further. These considerations were necessary to reduce noise for stringent wideband and high frequency operations.

Figure 5 shows the circuit of the VGA and the BPF implemented. The VGA topology is a two-stage differential cascode. Due to the transconductance characteristic of the MOSFET, coarse tuning of the gain can be made in several discrete steps by selecting values of  $V_{b3}$  thereby directly setting M16, M17, M20 and M21 bias points. If desired, fine tuning can be made through  $V_{b2}$  at the gate of M14 and M15 to control the DC current through the differential cascodes.

The band-pass filter is implemented by two RLC circuits, each in parallel with the output of an amplifier stage. Fixed inductor sizes are used with capacitances to center the BPF at IF. The capacitances are tunable by varactors designed with a tuning range of 10%. Using this method, the 3-dB bandwidth can be controlled and the flatness of the BPF response can be adjusted with the proper selection of the value of R3 and R4 since the fractional bandwidth  $F_b$  of each parallel RLC can be characterized by (1). Note that the quality factor of the resonant tank is the inverse of  $F_b$ .

$$F_b = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (1)$$

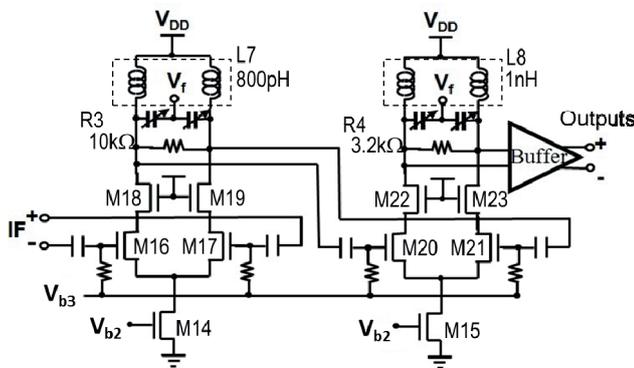


Fig. 5. Schematic of VGA, BPF and buffer block.

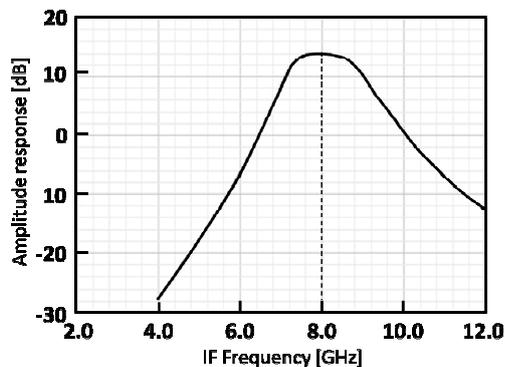


Fig. 6. Simulated results of IF filtering by BPF.

Equation (1) assumes a high-Q inductor. With a realistic CMOS inductor model [17], simulations were performed. Figure 6 shows the simulated results of the IF filtering by the BPF. The BPF is centered at 8 GHz with a bandwidth of 1.8 GHz. The simulated channel rejection at this bandwidth is 14.9 dB. Tuning is available with a range of 1.2 GHz. For measurement considerations, the unity gain open-drain buffers are used to drive the 50  $\Omega$  measurement system. It can drive the 50  $\Omega$  instruments and obtain the desired output signal. The buffer consumes 12.3 mW.

### 3. Experimental Result

Figure 7 shows the micrograph of the complete wideband receiver chip design. The LNA, mixer, VGA and band-pass filter are indicated on the micrograph. The receiver was fabricated using the 90 nm 1P8M CMOS process.

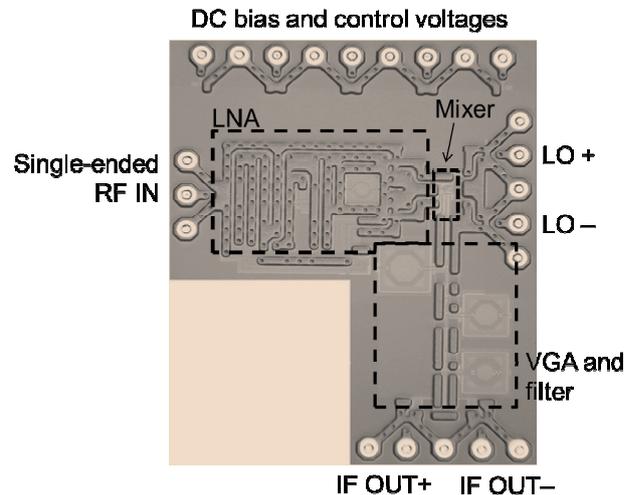


Fig. 7. Micrograph of wideband receiver chip.

The fabricated chip was tested by using a probe station. To test the performance of the fabricated receiver circuit the LO signal was applied from an external single ended millimeter-wave signal source by using an on chip GSG probe. But in practice the differential ended LO signal can be applied on the chip. It would reduce even order nonlinearities. In this measurement, the LO signal was injected at  $P_{LO} = -1$  dBm at four frequencies corresponding to four different channels to evaluate the multi-channel characteristics of the receiver. The IF output was maintained at 8 GHz. Setting the gain control voltages to  $V_{b2} = 0.65$  V and  $V_{b3} = 0.35$  V, the IF output power response as a function of the RF input frequency is shown in Fig. 8. In this figure, a gain of 23 dB is observed with an input-referred 1 dB-compression point at -29 dBm. To measure the nonlinear characteristic of the receiver, two tone millimeter wave signal was applied from two external sources through the RF input of the receiver by using a GSG probe. The measured fundamental and third order re-

sponses are shown in Fig. 9. The input referred third order interception point was measured to be a -20.5 dBm. The measured noise figure of the whole receiver is 8.1 dB. These performances can be acceptable for indoor short-range communications operating at low-power levels.

In such a scenario, adjacent channel interferences at 60 GHz are limited due to attenuation and the absence of large transmitter signals on the same chip, even though the receiver operates wideband. Depending on the linearity requirements of the modulation scheme, the trade-off between current drain for lower power consumption and linearity may be further adjusted. Figure 10(a) shows the results of the coarse tuning of the VGA gain.

As shown in Fig. 10, the coarse gain tuning of the VGA block is set by  $V_{b3}$  between 0.2 V and 0.5 V, corresponding to a minimum gain of 4.8 dB and a maximum of 54.9 dB. The coarse tuning demonstrates the limit of the gain obtainable by further fine tunings using  $V_{b2}$ . Results shown in Fig. 10(a) was obtained when  $V_{b2}$  is set to 0.65 V. It is noted that the gain flatness deteriorates at higher gain settings with a span of several gigahertz, resulting in changing 3-dB bandwidths. This is likely a result of the

VGA input impedance changing due to bias changes, causing the mixer-VGA wideband inter-stage matching network. For a system with narrowband channels, it is possible to adjust the band-pass filter bandwidth to achieve better gain flatness over different gain settings. Alternatively, in our envisioned pulse communication system that typically employs On-Off-Keying (OOK) or Amplitude-Shift Keying (ASK), such gain control characteristics may be sufficient.

Measurement of the receiver channel selection by LO tuning is shown in Fig. 10(b). The LO frequency is selected at four frequencies of 50.3 GHz, 52.5 GHz, 54.6 GHz and 56.8 GHz. With the IF at 8 GHz, the corresponding RF-input frequencies for channels 1 to 4 are 58.3 GHz, 60.5 GHz, 62.6 GHz and 64.8 GHz, respectively. The LO power is set to -1 dBm. It is noted that the frequency response at the third channel (CH3) is about 2 dB lower than the other channels. It is believed that this performance is caused by the limited gain flatness of the LNA. Its gain can be compensated by VGA gain tuning. This proposed receiver reports a considerable gain-bandwidth performance. The proposed wide-band single receiver can select all four 60 GHz band sub-channels and its gain can be controlled to improve the communication performance. In Tab. 1, recently reported wireless 60-GHz

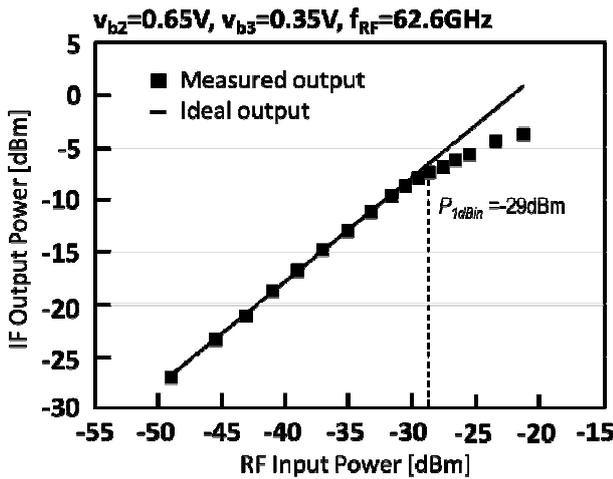


Fig. 8. Conversion gain characteristics of receiver.

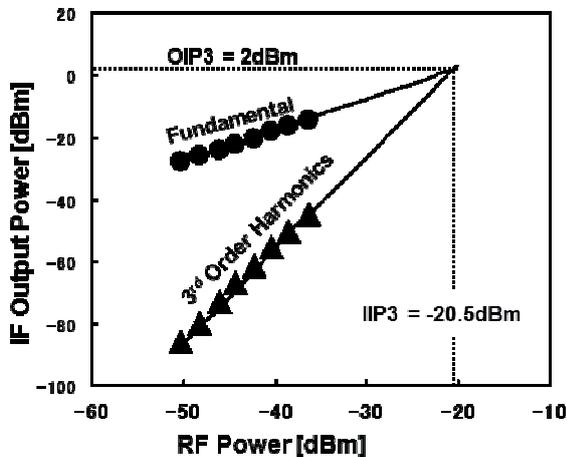


Fig. 9. Measured IIP3 of the receiver.

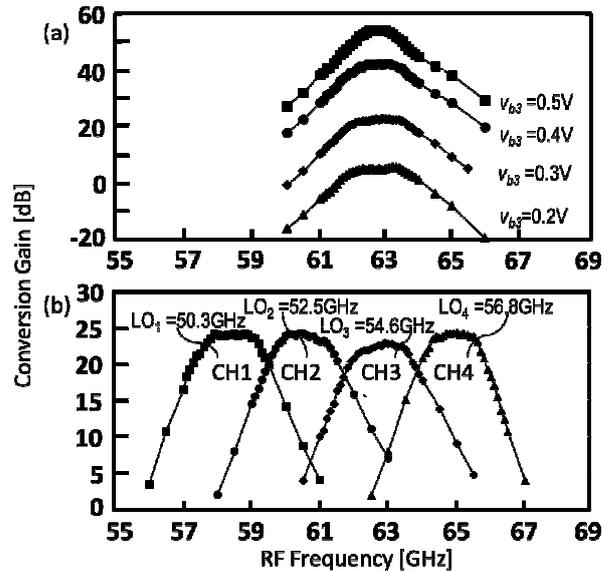


Fig. 10. (a) Receiver gain selection by VGA coarse tuning  $V_{b3}$  ( $V_{b2}$  set at 0.65 V). (b) Receiver channel selection by LO tuning (PLO = -1 dBm).

	Tech.	Freq. [GHz]	Gain [dB]	Power [mW]
This work	90nm CMOS	56.0-70.0	4.8-54.9	69.0
[18]	65nm CMOS	57.5-66.5	10.0-19.0	74.0
[19]	65nm CMOS	54.0-61.0	4.7-17.3	81.5
[20]	65nm CMOS	55.0-68.0	14.0-35.5	75.0
[21]	40nm CMOS	58.0	20.0	41.0
[22]	90nm CMOS	57-61.0	19.8-22.0	36.0
[23]	65nm CMOS	55.0-65.0	14.7	151.0
[24]	45nm CMOS	56.0-67.0	26.0	11.0-21.0
[25]	130nm SiGe	57.0-65.0	14.0	18.0

Tab. 1. Comparison of recent works.

band millimeter-wave receivers are compared. This proposed receiver using the enhanced LNA has the largest gain-bandwidth among them.

## 4. Conclusion

A multi-channel receiver operating between 56 GHz and 70 GHz for coverage of all four 60 GHz band sub-channels worldwide has been implemented with a 90 nm CMOS process. The receiver comprises of the millimeter-wave LNA, frequency mixer, VGA and bandpass filter. This enables the receiver to operate at wideband with reference measurements showing a 23 dB gain through LO injections of -1 dBm at each of the four channels tested, corresponding to receiver RF of 58.3 GHz, 60.5 GHz, 62.6 GHz and 64.8 GHz. Tuning of the VGA allows a range of gain to be selected with measured results between 4.8 dB and 54.9 dB. It requires a 1.2 V supply voltage and consumes 69 mW power. The proposed millimeter-wave multi-channel CMOS receiver can be used for low-voltage, low-power consuming and high-speed wireless communication applications.

## Acknowledgements

The chip in this work was realized in 90nm CMOS process through Silicon Library Inc. Author thanks Prof. Minoru Fujishima for accessing millimeter-wave measurement facilities, Dr. Lai Chee Hong and Mr. Pong for their valuable discussion on low power-LNA and layout designs.

## References

- [1] DOAN, C. H., EMAMI, S., NIKNEJAD, A. M., BRODERSEN, R. W. Design of CMOS for 60GHz applications. In *IEEE International Solid-State Circuits Conference ISSCC Digest of Technical Papers*, 2004, p. 440–441. DOI: 10.1109/ISSCC.2004.1332783
- [2] REYNOLDS, S. K., FLOYD, B. A., PFEIFFER, U. R., BEUKEMA, T., GRZYB, J., HAYMES, C., GAUCHER, B., SOYUER, M. A silicon 60-GHz receiver and transmitter chipset for broadband communications. *IEEE Journal on Solid-State Circuits*, 2006, vol. 41, no. 12, p. 2820–2831. DOI: 10.1109/JSSC.2006.884820
- [3] LAI, I. C. H., KAMBAYASHI, Y., FUJISHIMA, M. 60-GHz CMOS down-conversion mixer with slow-wave matching transmission lines. In *Proceedings of the IEEE Asian Solid-State Circuits Conference ASSCC 2006*. Hangzhou (China), 2006, p. 195–198. DOI: 10.1109/ASSCC.2006.357884
- [4] RAZAVI, B. A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider. In *IEEE International Solid-State Circuits Conference ISSCC Digest of Technical Papers*, 2007, p. 188–189. DOI: 10.1109/ISSCC.2007.373357
- [5] EMAMI, S., WISER, R. F., ALI, E., FORBES, M. G., GORDON, M. Q., GUAN, X., LO, S., MCELWEE, P. T., PARKER, J., TANI, J. R., GILBERT, J. M., DOAN, C. H. A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications. In *IEEE ISSCC Digest of Technical Papers*, 2004, p. 164–166.
- [6] YASUTAKE, N., OHUCHI, K., FUJIWARA, M., ADACHI, K., HOKAZONO, A., KOJIMA, K., AOKI, N., SUTO, H., WATANABE, T., MOROOKA, T., MIZUNO, H., MAGOSHI, S., SHIMIZU, T., MORI, S., OGUMA, H., SASAKI, T., OHMURA, M., MIYANO, K., YAMADA, H., TOMITA, H., MATSUSHITA, D., MURAOKA, K., INABA, S., TAKAYANAGI, M., ISHIMARU, K., ISHIUCHI, H. A hp22 nm node low operating power (LOP) technology with sub-10 nm gate length planar bulk CMOS devices. In *VLSI Technology Symposium Digest of Technical Papers*, 2004, p. 84–85. DOI: 10.1109/VLSIT.2004.1345407
- [7] VARONEN, M., KARKKAINEN, M., KANTANEN, M., HALONEN, K. Millimeter-wave integrated circuits in 65-nm CMOS. *IEEE Journal of Solid-State Circuits*, 2008, vol. 43, no. 9, p. 1991–2002. DOI: 10.1109/JSSC.2008.2001902
- [8] COSTANTINI, A., LAWRENCE, B., MAHON, S., HARVEY, J., MCCULLOCH, G., BESSEMOULIN, A. Broadband active and passive balun circuits: Functional blocks for modern millimeter-wave radio architectures. In *Proceedings of the 1<sup>st</sup> European Microwave Integrated Circuits Conference*. Manchester (UK), 2006, p. 421–424. DOI: 10.1109/EMICC.2006.282672
- [9] NATSUKARI, Y., FUJISHIMA, M. 36 mW 63 GHz CMOS differential low-noise amplifier with 14 GHz bandwidth. In *CORD Conference Proceedings*. June 2009, p. 252–253.
- [10] RAZAVI, B. A 60GHz direct-conversion CMOS receiver. In *IEEE International Solid-State Circuits Conference ISSCC Digest of Technical Papers*. San Francisco (USA), 2005, p. 400–401. DOI: 10.1109/ISSCC.2005.1494038
- [11] MARCU, C., CHOWDHURY, D., THAKKAR, C., KONG, L. K., TABESH, M., PARK, J. D., WANG, Y., AFSHAR, B., GUPTA, A., ARBABIAN, A., GAMBINI, S., ZAMANI, R., NIKNEJAD, A. M., ALON, E. A 90nm CMOS low-power 60GHz transceiver with integrated baseband circuitry. In *IEEE International Solid-State Circuits Conference ISSCC Digest of Technical Papers*. 2009, p. 314–315.
- [12] PINEL, S., SARKAR, S., SEN, P., PERUMANA, B., YEH, D., DAWN, D., LASKAR, J. A 90nm CMOS 60GHz radio. In *IEEE International Solid-State Circuits Conference ISSCC Digest of Technical Papers*. San Francisco (USA), 2008, p. 130–131. DOI: 10.1109/ISSCC.2008.4523091
- [13] LEE, J., HUANG, Y., CHEN, Y., LU, H., CHANG, C. A low-power fully integrated 60GHz transceiver system with OOK modulation and on-board antenna assembly. In *IEEE International Solid-State Circuits Conference ISSCC Digest of Technical Papers*. San Francisco (USA), 2009, p. 316–318. DOI: 10.1109/ISSCC.2009.4977435
- [14] WEYERS, C., MAYR, P., KUNZE, J. W., LANGMANN, U. A 22.3dB voltage gain 6.1dB NF 60GHz LNA in 65nm CMOS with differential output. In *International Solid-State Circuits Conference ISSCC Digest of Technical Papers*. San Francisco (USA), 2008, p. 192–606. DOI: 10.1109/ISSCC.2008.4523122
- [15] CHAO-SHIUN WANG, J. W. H. A 0.13 $\mu$ m CMOS fully differential receiver with on-chip baluns for 60GHz broadband wireless communications. In *Proc. of Custom Integrated Circuits Conference CICC 2008*. San Jose (USA), 2008, p. 479–482. DOI: 10.1109/CICC.2008.4672125
- [16] CHEN, P.-H., CHEN, M.-C., KO, C.-L., WU, C.-Y. An integrated CMOS front-end receiver with a frequency tripler for V-band applications. *IEICE Transactions on Electronics*, 2010, vol. E93–C, no. 6, p. 877–883. DOI: 10.1587/transele.E93.C.877
- [17] BLASCHKE, V., VICTORY, J. A scalable model methodology for octagonal differential and single-ended inductors. In *Proceedings*

- of *Custom Integrated Circuits Conference CICC 2006*. San Jose (USA), 2006, p. 717–720. DOI: 10.1109/CICC.2006.320897
- [18] SILIGARIS, A., RICHARD, O., MARTINEAU, B., MOUNET, C., CHAIX, F., FERRAGUT, R., DEHOS, C., LANTERI, J., DUSSOPT, L., YAMAMOTO, S. D., PILARD, R., BUSSON, P., CATHELIN, A., BELOT, D., VINCENT, P. A 65nm CMOS fully integrated transceiver module for 60GHz wireless HD applications. In *IEEE International Solid-State Circuits Conference ISSCC Digest of Technical Papers 2011*. San Francisco (USA), 2011, p. 162–164. DOI: 10.1109/ISSCC.2011.5746264
- [19] OKADA, K., MATSUSHITA, K., BUNSEN, K., MURAKAMI, R., MUSA, A., SATO, T., ASADA, H., TAKAYAMA, N., LI, N., ITO, S., CHAIVIPAS, W., MINAMI, R., MATSUZAWA, A. A 60GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE 802.15.3c. In *IEEE International Solid-State Circuits Conference ISSCC 2011 Digest of Technical Papers*. San Francisco (USA), 2011, p. 160–162. DOI: 10.1109/ISSCC.2011.5746263
- [20] VECCHI, F., BOZZOLA, S., POZZONI, M., GUERMANDI, D., TEMPORITI, E., REPOSSI, M., DECANIS, U., MAZZANTI, A., SVELTO, F. A wideband mm-wave CMOS receiver for Gb/s communications employing interstage coupled resonators. In *IEEE International Solid-State Circuits Conference ISSCC 2010 Digest of Technical Papers*. San Francisco (USA), 2010, p. 220–221. DOI: 10.1109/ISSCC.2010.5433953
- [21] KAWASAKI, K., AKIYAMA, Y., KOMORI, K., UNO, M., TAKEUCHI, H., ITAGAKI, T., HINO, Y., KAWASAKI, Y., ITO, K., HAJIMIRI, A. A millimeter-wave intra-connect solution. In *IEEE International Solid-State Circuits Conference ISSCC 2010 Digest of Technical Papers*. San Francisco (USA), 2010, p. 414 to 415. DOI: 10.1109/ISSCC.2010.5433831
- [22] PARSA A., RAZAVI, B. A new transceiver architecture for the 60-GHz band. *IEEE Journal of Solid-State Circuits*, 2009, vol. 44, no. 3, p. 751–762. DOI: 10.1109/JSSC.2008.2012368
- [23] TOMKINS, A., AROCA, R. A., YAMAMOTO, T., NICOLSON, S. T., DOI, Y., VOINIGESCU, S. P. A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link. *IEEE Journal of Solid-State Circuits*, 2009, vol. 44, no. 8, p. 2085–2099. DOI: 10.1109/JSSC.2009.2022918
- [24] BORREMANS, J., RACZKOWSKI, K., WAMBACQ, P. A digitally controlled compact 57-to-66GHz front-end in 45nm digital CMOS. In *IEEE International Solid-State Circuits Conference ISSCC2009 Digest of Technical Papers*. San Francisco (USA), 2009, p. 492–493. DOI: 10.1109/ISSCC.2009.4977523
- [25] NATARAJAN, A., TSAI, M.-D., FLOYD, B. 60GHz RF-path phase-shifting two-element phased-array front-end in silicon. In *Dig. Symposium on VLSI Circuit*. Kyoto (Japan), 2009, p. 250 to 251.

## About the Author ...

**Ahmet ONCU** was born in Istanbul, Turkey in 1979. He received the B.S. degree in Physics and the B.S. degree in Electrical and Electronics Engineering from Middle East Technical University (METU), Ankara, Turkey, in 2001 and 2002, respectively. He received the M.S. degree in Microwave Engineering from the Technical University of Munich, Germany, in 2004. He received the PhD degree in Frontier Sciences from the University of Tokyo, Japan, in 2008. Currently he is an assistant professor at the Department of Electrical and Electronics Engineering, Bogazici University, Istanbul, Turkey. Dr. Oncu received FP7 Marie Curie Reintegration Grant for (project no: 268232) (UWB-IR) Study on Low-power Multi-Gbps Ultra-Wideband Impulse Radio at License-free UWB and 60GHz bands in 2010. His research interests are in designs of high-speed low-power CMOS analog and RF integrated circuits.