Everything You Wish to Know About Memristors But Are Afraid to Ask

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Abstract. *This paper classifies all memristors into three classes called* ***Ideal****,* ***Generic****, or* ***Extended*** *memristors. A subclass of Generic memristors is related to Ideal memristors via a one-to-one mathematical transformation, and is hence called Ideal Generic memristors. The concept of non-volatile memories is defined and clarified with illustrations. Several fundamental new concepts, including* ***Continuum-memory memristor****,* ***POP*** *(acronym for Power-Off Plot),* ***DC V-I Plot****, and* ***Quasi DC V-I Plot****, are rigorously defined and clarified with colorful illustrations. Among many colorful pictures the* ***shoelace*** *DC V-I Plot stands out as both stunning and illustrative. Even more impressive is that this bizarre* ***shoelace*** *plot has an* ***exact analytical*** *representation via 2* ***explicit*** *functions of the state variable, derived by a novel* ***parametric approach*** *invented by the author.*

Keywords

Memristor, discrete-memory memristors, continuum-memory memristor, POP, Power-Off Plot, DC V-I Plot, Quasi DC V-I Plot, Shoelace V-I Plot, parametric approach, graphical composition, piecewise-linear (PWL) function

1. Some Nagging Questions about Memristors

Ever since the publication of the *hp*'s seminal paper in Nature [1], reporting its fabrication of a *2-terminal device* that bears the fingerprints of the *memristor* [2], there has been a torrent of memristor activities from both industry and academia to exploit the unique properties of the memristor for building a new generation of smart computers [3] and brain-like machines [4], [35]. Since the memristor is intrinsically a *nonlinear* electronic device, researchers and engineers unfamiliar with *nonlinear dynamics* are often confused, if not intimidated. Following are some questions researchers and engineers are afraid to ask:

1. How do I know whether my experimental device is a memristor ?
2. What are the *fingerprints* of a memristor?
3. Does memristor possess a *signature* that distinguishes it from the 3 classic circuit elements (resistor, capacitor, inductor)?
4. What is a *non-volatile memory*?
5. Is every memristor a *non-volatile memory*?
6. What unique attribute of the memristor is exploited to make a *non-volatile memory*?
7. How does one *write* a binary bit "0", or "1", on a memristor?
8. How does one *read* a binary bit "0", or "1", from a memristor?
9. What does it mean to say the memristor can store *analog* data?
10. Most 2-terminal solid state devices, such as the p-n junction diode, have a DC V-I curve. What does the *DC V-I curve* of a memristor look like?
11. Can we store *energy* on a memristor?
12. Why are *synapses* memristors?
13. Why are the sodium and potassium ion channels in the classic *Hodgkin-Huxley axon membrane model* not time-varying resistors, but are in fact memristors?
14. Why are brains made of memristors?

2. Experimental Definition of Memristors

Any 2-terminal device exhibiting a *pinched hysteresis loop* which *always passes through the origin* in the voltage-current plane when driven by *any periodic* input current source, or voltage source, with zero DC component is called a *memristor*[1]. If the input is a current source, it is called a *current-controlled memristor* as shown in Fig. 1. If it is a voltage source, it is called a *voltage-controlled memristor* as shown in Fig. 2.

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The above is an *axiomatic*, or *black box*, *definition* because the *internal composition* of the device is *irrelevant.* Indeed, not only can memristors be made from different materials, they have even been found in amoeba, squids and plants, and numerous other living beings [5].

Once a device is identified from experimental measurements to be a memristor, it is natural to develop a mathematical model which can mimic approximately the measured pinched hysteresis loops.

For pedagogical reasons, it is convenient to classify a memristor according to the complexity of its mathematical representation into the 4 classes listed in Tab. 1, in the order of decreasing complexity.

The Venn diagram in Fig. 3 shows the memristor universe and the relationship among the 4 classes of memristors listed in Tab. 1.

The simplest class of memristors defined in the lowest part of Tab. 1 is called an *ideal memristor*, which coincides with the original definition postulated in [2]. Indeed, we can recover its *constitutive relation*, within an arbitrary constant $\varphi(0)$,via

$$\varphi \triangleq \varphi(0) + \int_0^q R(q)\,dq \triangleq \hat{\varphi}(q) \ . \tag{1}$$

Observe that differentiating both sides of (1) with respect to time t gives

$$\frac{d\varphi}{dt} = R(q)\frac{dq}{dt} \tag{2}$$

or

$$v = R(q)\,i \tag{3}$$

upon identifying $\frac{d\varphi}{dt} = v$ and $\frac{dq}{dt} = i$, respectively.

Equation (1), which is equivalent to (2), is called the *constitutive relation* of a charge-controlled memristor in [2], [6], [7]. The dual *constitutive relation* of a flux-controlled memristor

$$q = \hat{q}(\varphi) \tag{4}$$

is equivalent to the *voltage-controlled memristor*

$$i = G(\varphi)v \ , \tag{5}$$

$$\frac{d\varphi}{dt} = v \tag{6}$$

defined in the lower right corner of Tab. 1. The uninitiated readers are referred to several primers on the *ideal memristor* in [8], [9], [10].

3. Ideal Memristors

To avoid clutter, we will present this section only for the class of *Voltage-Controlled Memristors*. The *dual case* for *Current-Controlled Memristors* follows the same developments, *mutatis mutandis*.

The *ideal* voltage-controlled memristor is defined by a single scalar function $G(\varphi)$, called the *memductance*. Since the input in this case is a voltage source, the independent variable is the flux φ, defined by

$$\varphi(t) \triangleq \int_{-\infty}^{t} v(\tau)\,d\tau = \varphi(0) + \int_0^t v(\tau)\,d\tau \ . \tag{7}$$

Once the voltage source function $v = v(t)$, and the *initial flux* $\varphi(0)$ are given, the flux waveform $\varphi(t)$ is calculated via (7), which when substituted into the memductance $G(\varphi)$ gives the *time-varying conductance* $G(\varphi(t))$, and the corresponding current waveform $i(t)$ via the *state-dependent Ohm's law* $i(t) = G(\varphi(t))\,v(t)$. Plotting the loci of $(v(t), i(t))$ in the i *vs.* v plane with the time t as parameter, the resulting graph is in general multi-valued, and always passes through the origin, hence the name *pinched hysteresis loop*.

As an example, consider an ideal flux-controlled memristor described by the odd-symmetric piecewise-linear (PWL) constitutive relation (shown in the left column of Fig. 4). For future reference, the equation of the identical PWL curve in Figs. 4(a) and 4(c) is given in (8).

$$q = \hat{q}(\varphi) = 0.01\varphi + 0.04|\varphi + 0.25| - 0.04|\varphi - 0.25| \ . \tag{8}$$

Let us connect a voltage source $v(t) = 1.2 \sin t$ across this memristor, and choose 2 different initial states identified as point ❶ on the q *vs.* φ curve in Figs. 4(a), (c), respectively. The corresponding pinched hysteresis loop is shown in Figs. 4(b), (d), respectively[2].

Pinched Hysteresis Loops Depend on Initial States !

Two pinched hysteresis loops measured from an ideal memristor driven by the same periodic voltage source (resp., current source) but different initial states can look very different from each other.

[1] Our axiomatic definition requires a *pinched hysteresis loop* to be measured not only for one input signal, but for *all* possible periodic input signals with zero mean. In practice, only a finite number of measurements could be made.

Our definition did *not* require *the same* pinched hysteresis loop to be measured whenever the same input signal is applied, because for *non-volatile* memristors, the pinched hysteresis loop depends not only on the input waveform $i(t)$ or $v(t)$, but also on the initial conditions of the relevant state variables, such as Fig. 42 of [5], where two *different* pinched hysteresis loops are measured for the same input current source $i(t) = 10 \sin(\omega t)$, but different initial states $x(0) = -6.3$ and $x(0) = 6.3$, respectively.

[2] Readers puzzled by the dramatic difference between the 2 pinched hysteresis loops in Fig. 4(b) and 4(d) calculated from *the same* memristor constitutive relation $q = \hat{q}(\varphi)$, and the same input $v(t) = 1.2 \sin t$ are referred to the exact calculations and graphical illustrations in Fig. 28 and Fig. 27 of [5], respectively.

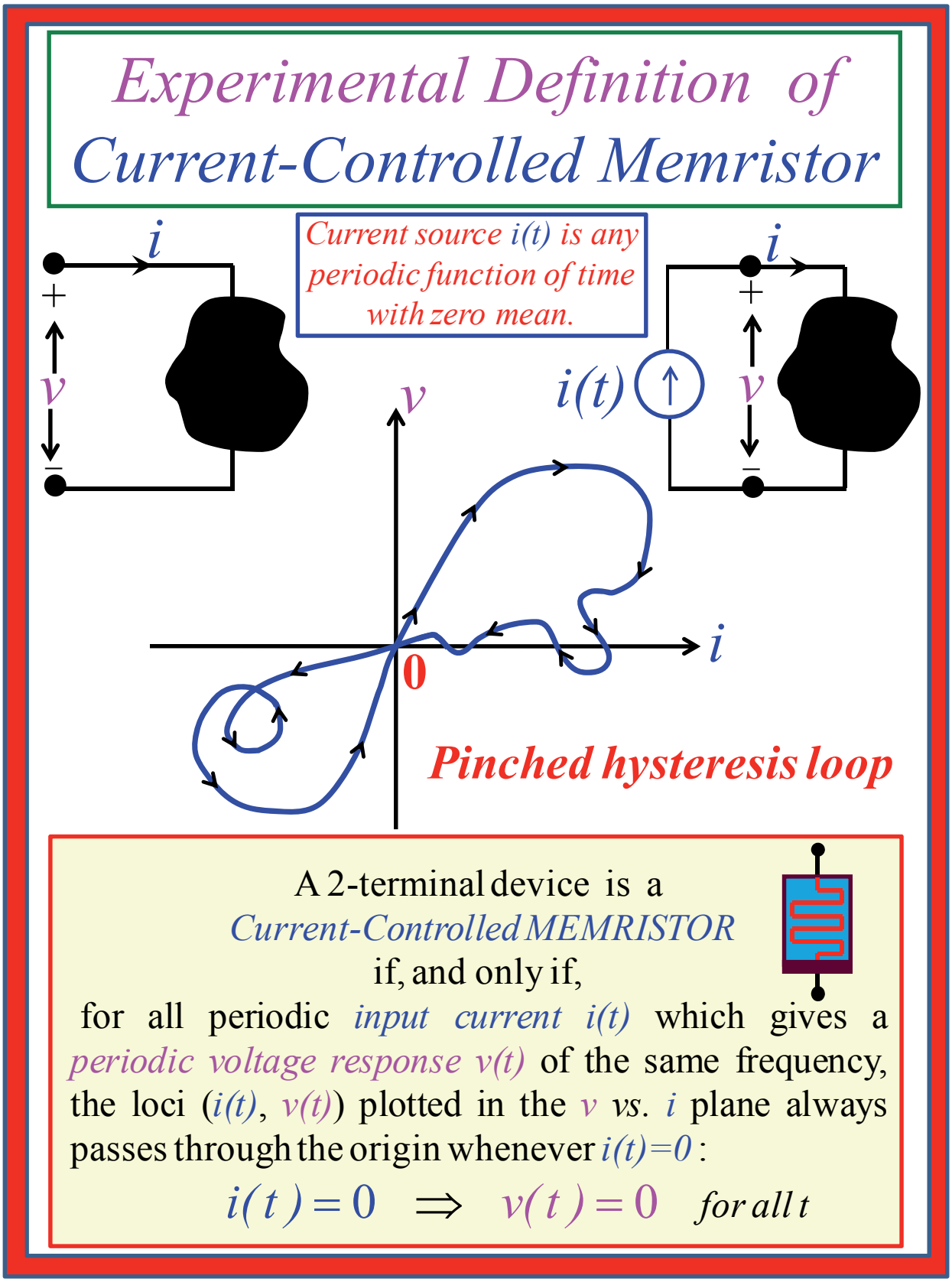


Fig. 1. A *pinched hysteresis loop* in the voltage *vs.* current plane defines a current-controlled memristor. The ($i(t)$, $v(t)$) loci may intersect itself, or with the horizontal i -axis, but *not* with the vertical v-axis.

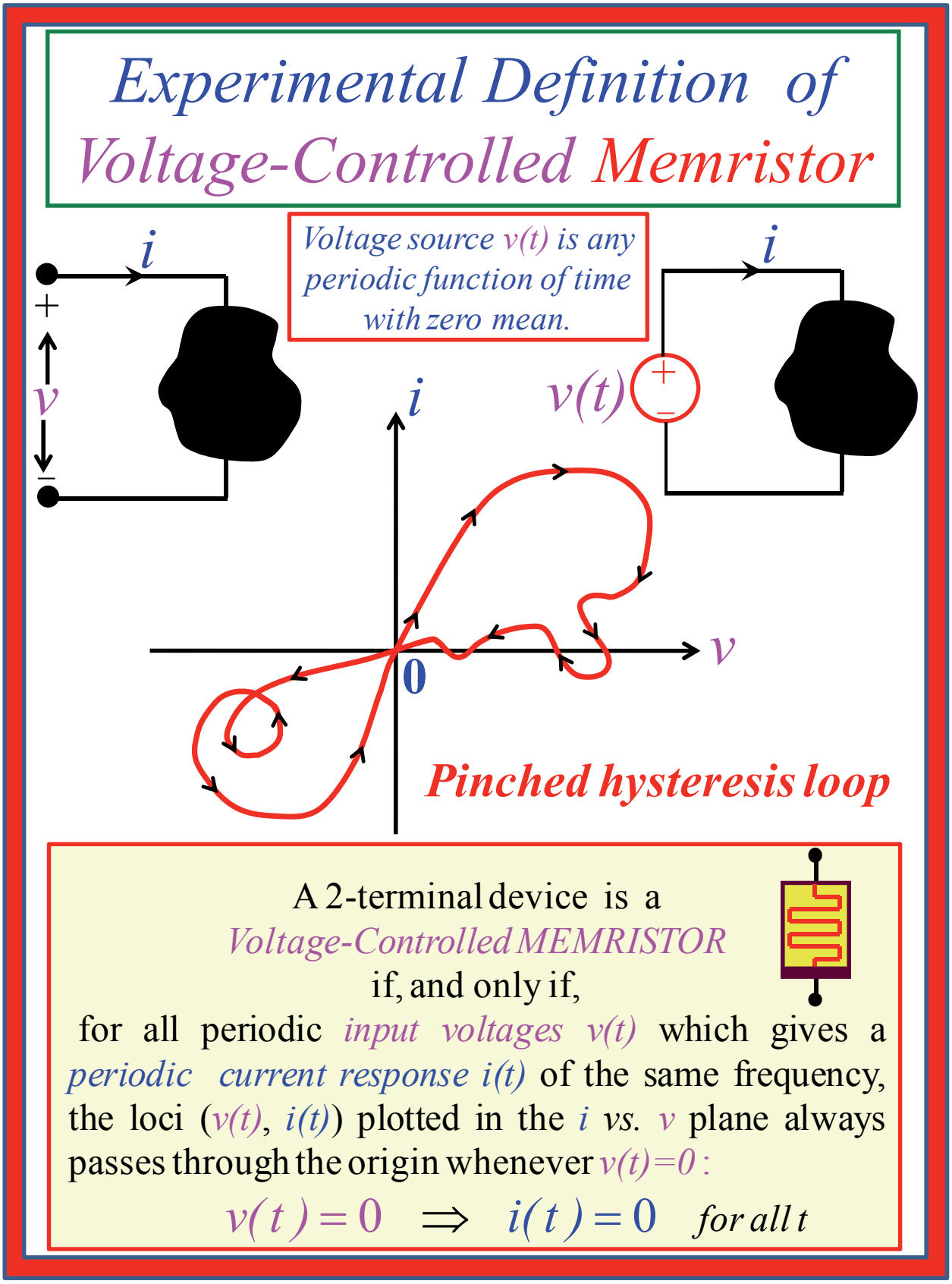
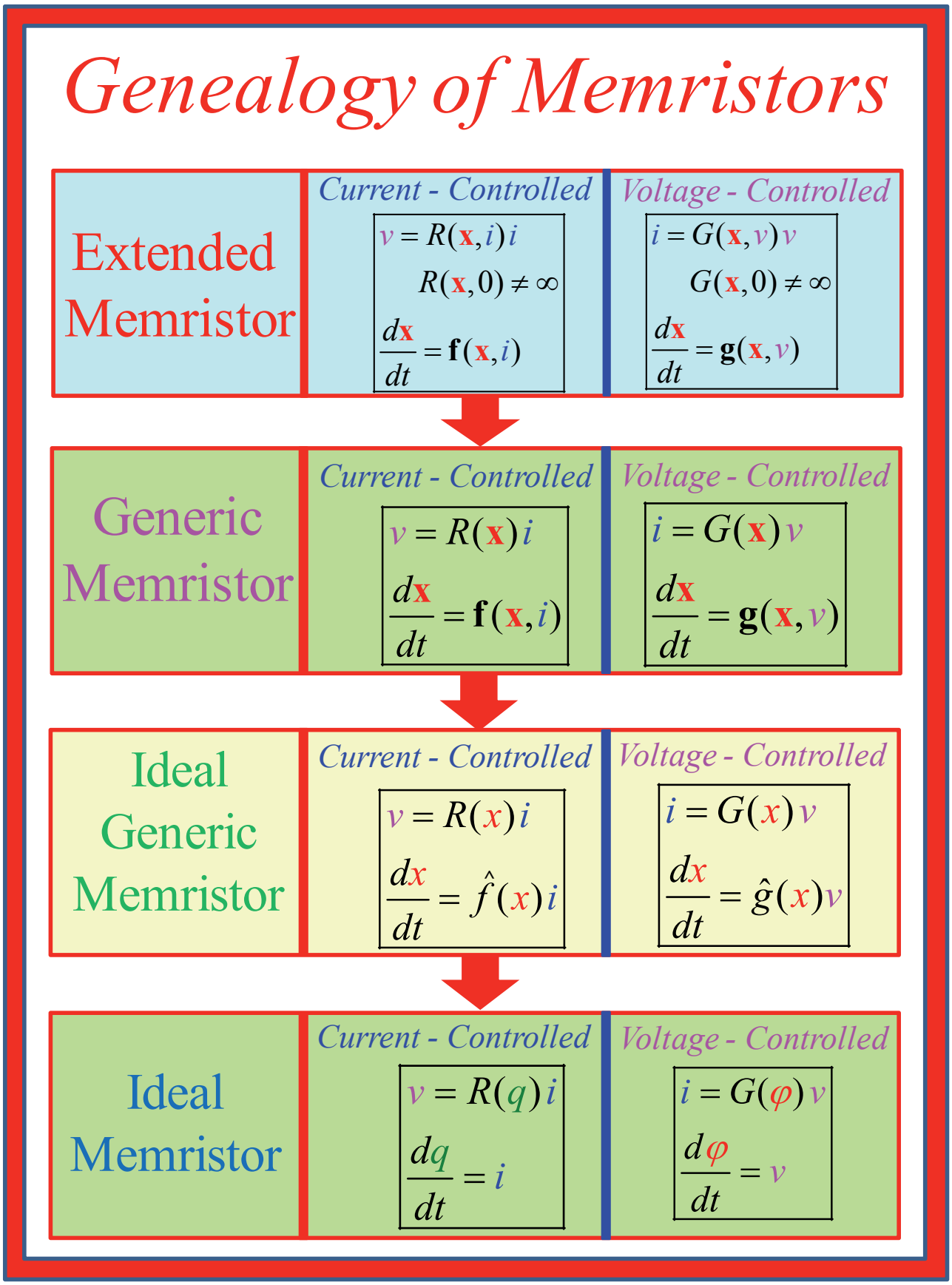


Fig. 2. A *pinched hysteresis loop* in the current *vs.* voltage plane defines a voltage-controlled memristor. The ($v(t)$, $i(t)$) loci may intersect itself, or with the horizontal v-axis, but *not* with the vertical i-axis.



Tab. 1. Four classes of memristors.

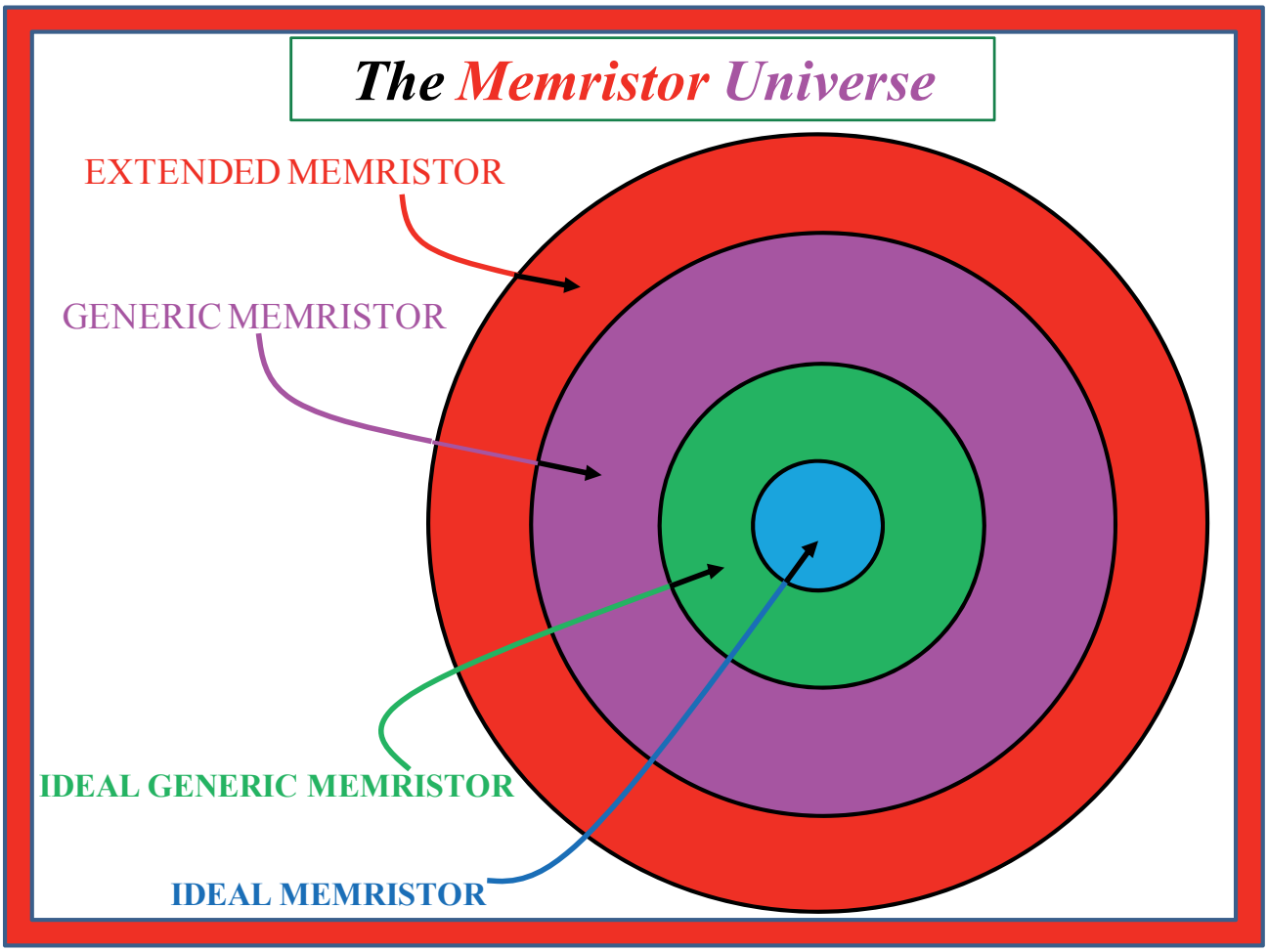


Fig. 3. Venn diagram showing the relationship among the 4 classes of memristors.

The alert reader would have noticed that the pinched hysteresis loops in Fig. 4 are both *odd symmetric*. They may even argue that this symmetry property follows from the fact that both the constitutive relation $q = \hat{q}(\varphi)$ and the input $v = 1.2 \sin t$ are symmetric with respect to the origin.

The above reasoning, however, is *not* correct. In fact, even if we modify the q *vs.* φ curve in Fig. 4(a) to make it not symmetric, as shown in Fig. 5(a) where the slope of the leftmost segment is reduced to differ from that of Fig. 4(a), and hence described by the following PWL equation[3]

$$q = -0.00375 + 0.025\varphi + 0.04|\varphi + 0.25| - 0.025|\varphi - 0.25| \quad (9)$$

we would still obtain an odd-symmetric pinched hysteresis loops, as shown in Fig. 5(b).

The correct source of the symmetry comes from the observation that one traverses from point ❶ (initial state) to point ❻ during the first half cycle $0 \le t \le \pi$ of the periodic input signal, and *retraces* the same path from point ❻ to the initial point ❶ at the end of the negative half cycle. In fact the following symmetry theorem has been proved in [11];

Pinched hysteresis loop symmetry theorem:

The pinched hysteresis loop derived from any ideal memristor driven by a half-wave odd-symmetric input voltage source, or current source, is odd-symmetric, and crosses each other with distinct slopes at the origin provided that the loci is double-valued in a small neighborhood of the origin.

4. Ideal Generic Memristor

A memristor is called an *Ideal Generic Memristor* if it's State-Dependent Ohm's Law and State Equation assumes the form shown in the third row of Tab. 1. Given any ideal memristor, we can create an *infinite* number of

[3] Observe the two PWL equations (8) and (9) give rise to two different PWL curves in Fig. 4(a) and Fig. 5(a), respectively. Unlike Fig. 4(a), the PWL curve in Fig. 5(a) is not odd symmetric due to the presence of a constant term in (9).

ideal generic memristor *siblings* by choosing any piecewise differentiable 1:1 function, via the simple steps presented in Tab. 2 for creating a voltage-controlled sibling.

Let us illustrate the memristor sibling algorithm in Tab. 2 with an example.

Example 4.1

Let us choose the ideal voltage-controlled memristor from Fig. 5(a) whose PWL q *vs.* φ curve is reproduced in Fig. 6, along with its flux-dependent memductance $G(\varphi)$ whose analytical equation is expressed via the *signum function* defined in Appendix (Fig. B).

To apply *step 1* from Tab. 2, we must choose a piecewise-differentiable 1:1 function $x = \hat{x}(\varphi)$, and derive its inverse function $\varphi = \hat{x}^{-1}(x)$. For simplicity, let us choose the *2-segment piecewise-linear* (PWL) function[4] $x = \hat{x}(\varphi)$, and its inverse PWL function $\varphi = \hat{x}^{-1}(x)$ shown in Fig. 7.

To apply *step 2* from Tab. 2, we must first derive the *analytical equation* of $G(\varphi) = d\hat{q}(\varphi)/d\varphi$, which is a function of φ as shown in Fig. 6. Next, we must substitute the inverse function $\varphi = \hat{x}^{-1}(x)$ from Fig. 7 for φ in the above expression to obtain the state-dependent function $G(x)$, as shown in Fig. 8.

To apply *step 3* from Tab. 2, we must first derive $d\hat{x}(\varphi)/d\varphi$ from Fig. 7, which is a function of φ. We must next substitute the inverse function $\varphi = \hat{x}^{-1}(x)$ from Fig. 7 for φ in the above expression to obtain the *morphing* function $\hat{g}(x)$, as shown in Fig. 9.

To apply the final *step 4* from Tab. 2, we simply plot the functions $G(x)$ and $\hat{g}(x)$ derived in Fig. 8, and Fig. 9, respectively, as shown on the right side of Fig. 10.

4.1 Graphical Composition Method for Generating $G(x)$ and $\hat{g}(x)$ from a Voltage-Controlled Ideal Memristor

In the case where the piece-wise differentiable 1:1 function $x = \hat{x}(\varphi)$ from step 1 of Tab. 2 is chosen to be a *non-piecewise-linear* function, then its *inverse function* $\varphi = \hat{x}^{-1}(x)$ will usually *not* have an explicit equation, and will have to be calculated *numerically*, or plotted *graphically*. In such situations, the two functions $G(x)$ and $\hat{g}(x)$ defining the ideal memristor sibling can be found either numerically by writing a special program specifying the inverse function, or by the *graphical composition method* which we illustrate next, using the same example presented in Fig. 6.

The *graphical composition method* [24] for deriving $G(x)$ is illustrated in Fig. 11. Each point P on the $d\hat{q}(\varphi)/d\varphi$ curve (upper-left corner) is projected vertically downward, and horizontally to the right. The point where the vertical projection intersects the unit-slope line is then projected horizontally to the right until it intersects the $\varphi = \hat{x}^{-1}(x)$ curve (lower-right corner), where upon it is projected vertically upward, until it intersects the horizontal projection line emanating from point P on the upper-left function $d\hat{q}(\varphi)/d\varphi$. This intersection gives one point on $G(x)$. Repeating this *graphical composition procedure* with a sufficient number of points from $d\hat{q}(\varphi)/d\varphi$, and drawing a smooth curve through these points, one would obtain the desired function $G(x)$.

The graphical composition method for deriving $\hat{g}(x)$ is illustrated by a similar procedure in Fig. 12.

4.2 Graphical Composition Method for Generating $R(x)$ and $\hat{f}(x)$ from a Current-Controlled Ideal Memristor

So far we have chosen a flux-controlled *ideal memristor* described by a *PWL* function $q = \hat{q}(\varphi)$. Let us now consider an example of a charged-controlled Ideal Memristor described by a smooth function $\varphi = \hat{\varphi}(q)$ as shown in Tab. 3. Here we have chosen a very special 1:1 function $x = \hat{x}(q) = q^3$ that has an *analytical inverse* function $q = \hat{x}^{-1}(x) = x^{1/3}$, in order that we can verify our *graphical composition procedure* gives the same results.

The graphical composition procedure for deriving the memristance $R(x)$ is shown in Fig. 13.

The graphical composition method for deriving $\hat{f}(x)$ is illustrated by a similar procedure in Fig. 14.

We end Sec. 4.2 by emphasizing that the *graphical composition method* for creating Ideal Generic Memristor Siblings is a general method applicable to any situation where one has to plot a *function of another function* in graphical form. One could of course write a computer program to implement the graphical composition procedure. But a quick sketch on paper is often more illuminating because it identifies how and where each point on the sibling memristor characteristic functions is related to a corresponding point on its ideal memristor parent.

4.3 Ideal Memristors and its Siblings Give Identical Pinched Hysteresis Loops

Let us examine the $q = \hat{q}(\varphi)$ constitutive relation of the Ideal memristor with the memductance $G(x)$ and the morphing function $\hat{g}(x)$ of its memristor sibling derived earlier in Fig. 10. Superficially, they look very different

[4] Although one can choose any piecewise-differentiable function $x = \hat{x}(\varphi)$, it is rare that its inverse function $\varphi = \hat{x}^{-1}(x)$ has an analytical equation. We opted for a PWL function because not only it has an explicit equation, as shown in Appendix A, its *inverse* function is also a PWL function, and hence will also have an explicit equation.

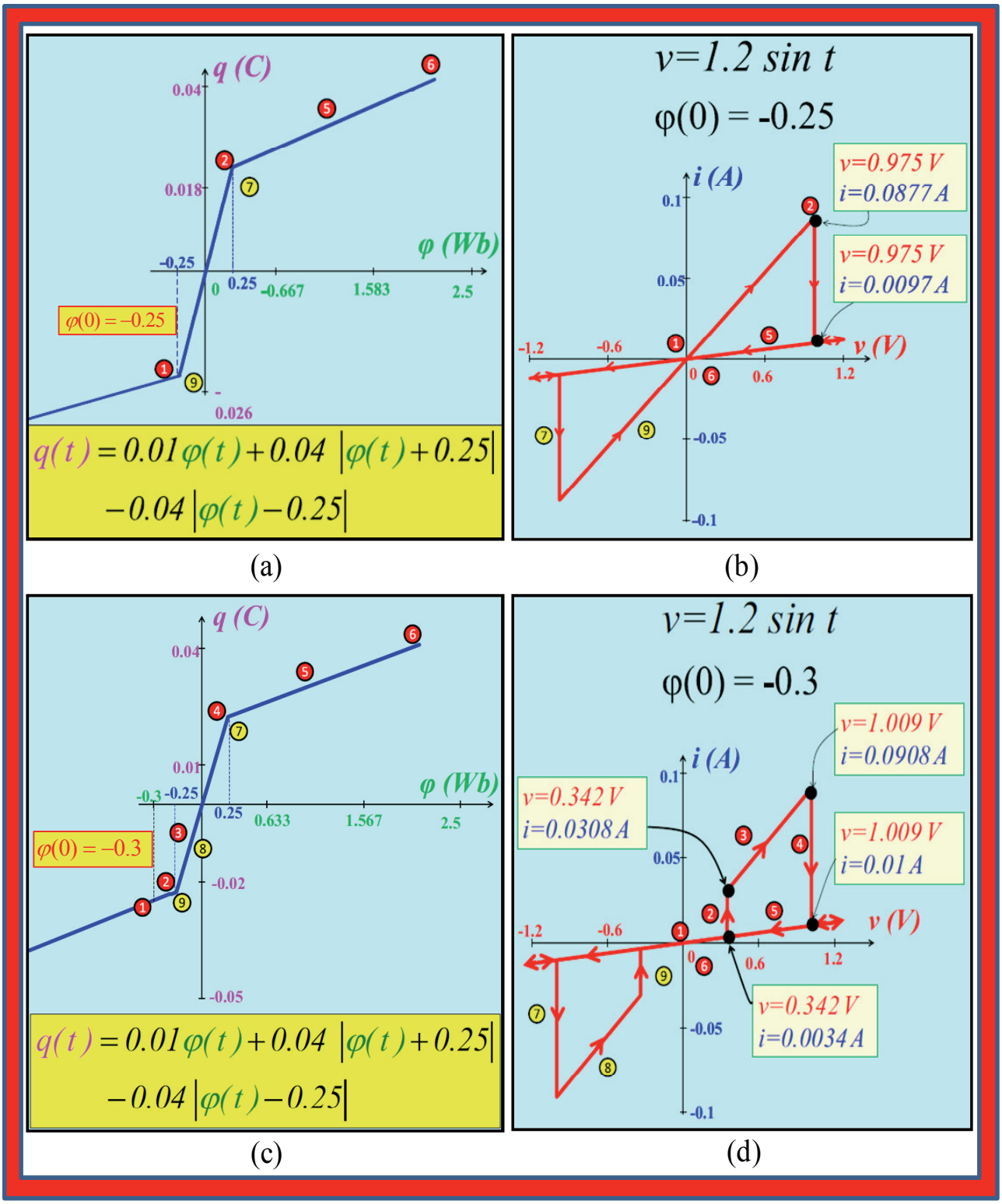


Fig. 4. Two pinched hysteresis loops resulting from the *identical constitutive relation* on the left, and the *same input voltage* $v(t) = 1.2 \sin t$, but *different initial states*: (a) $\varphi(0) = -0.25$; (b) Pinched hysteresis loop for $\varphi(0) = -0.25$; (c) $\varphi(0) = -0.3$, (d); Pinched hysteresis loop for $\varphi(0) = -0.3$.

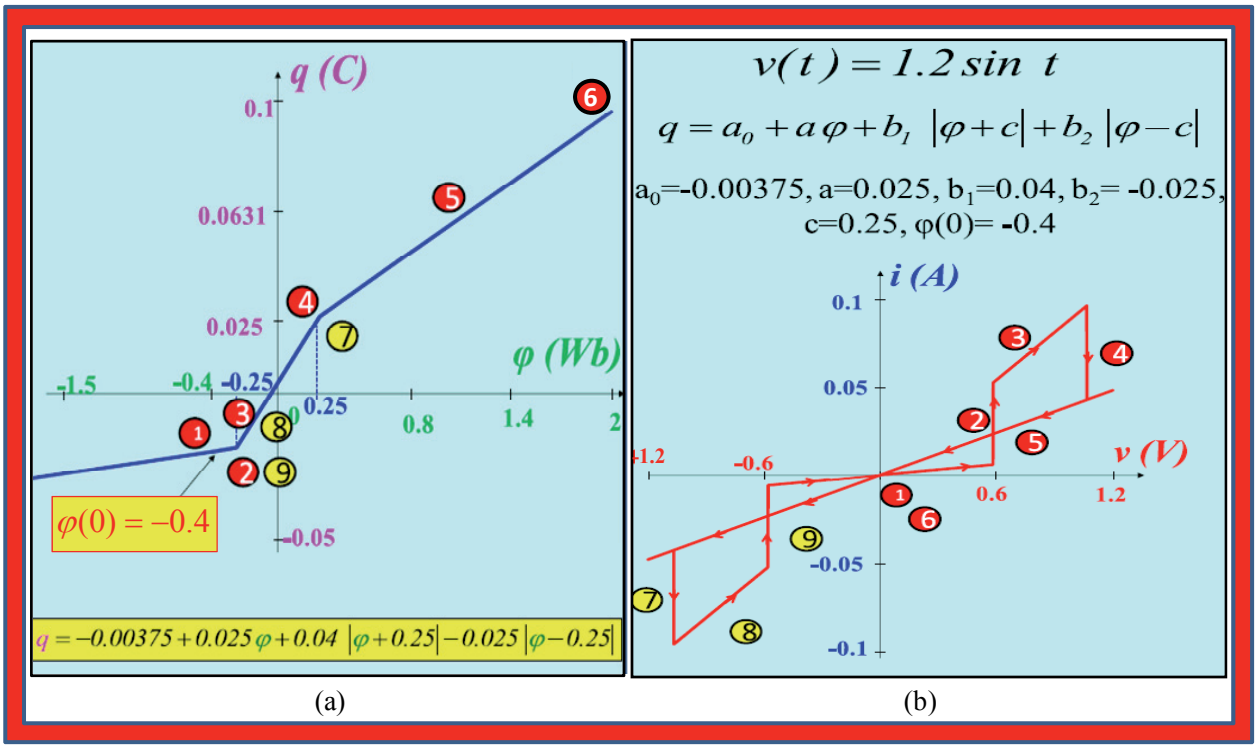


Fig. 5. A not-symmetric constitution relation $q = \hat{q}(\varphi)$ also gives rise to an odd-symmetric pinched hysteresis loop.

Creating voltage-controlled memristor sibling

Given constitutive relation: $q = \hat{q}(\varphi)$

Step 1: Choose any piecewise-differentiable 1:1 function $x = \hat{x}(\varphi)$
and denote its inverse function by $\varphi = \hat{x}^{-1}(x)$

Step 2: Define $$G(x) \triangleq \left.\frac{d\hat{q}(\varphi)}{d\varphi}\right|_{\varphi=\hat{x}^{-1}(x)}$$

Step 3: Define $$\hat{g}(x) = \left.\frac{d\hat{x}(\varphi)}{d\varphi}\right|_{\varphi=\hat{x}^{-1}(x)}$$

Step 4: Define the memristor sibling as follows

$$i = G(x)\, v$$
$$\frac{dx}{dt} = \hat{g}(x)\, v$$

Tab. 2. Four steps to create an Ideal Memristor Sibling.

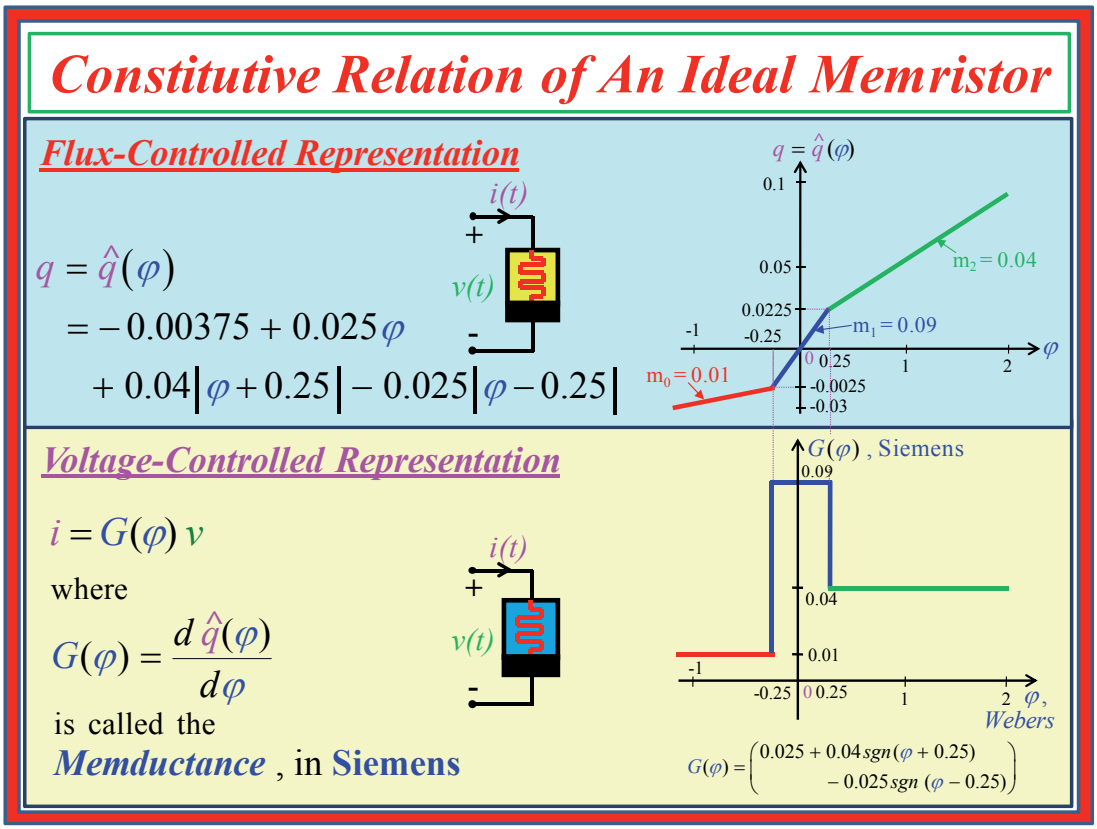


Fig. 6. Constitutive relation and memductance of an ideal voltage-controlled memristor.

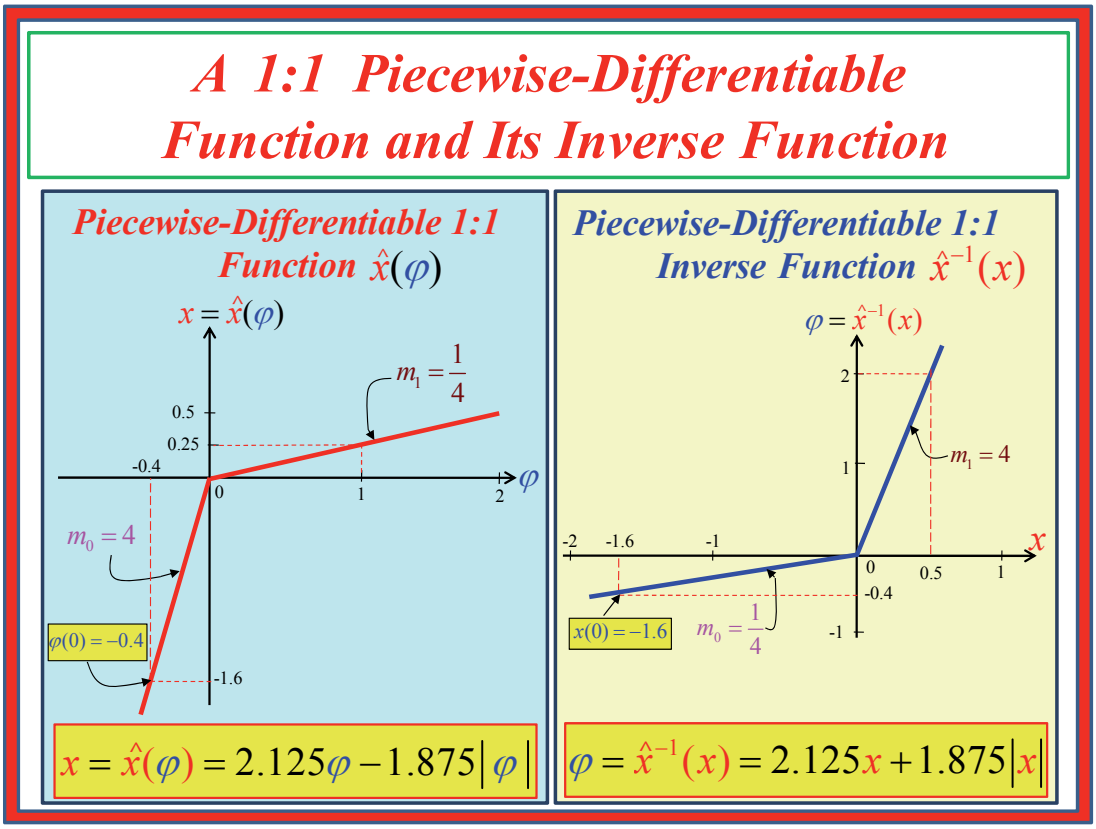


Fig. 7. The graph and equation of the PWL function $x = \hat{x}(\varphi)$ on the left, and its inverse PWL function $\varphi = \hat{x}^{-1}(x)$ on the right.

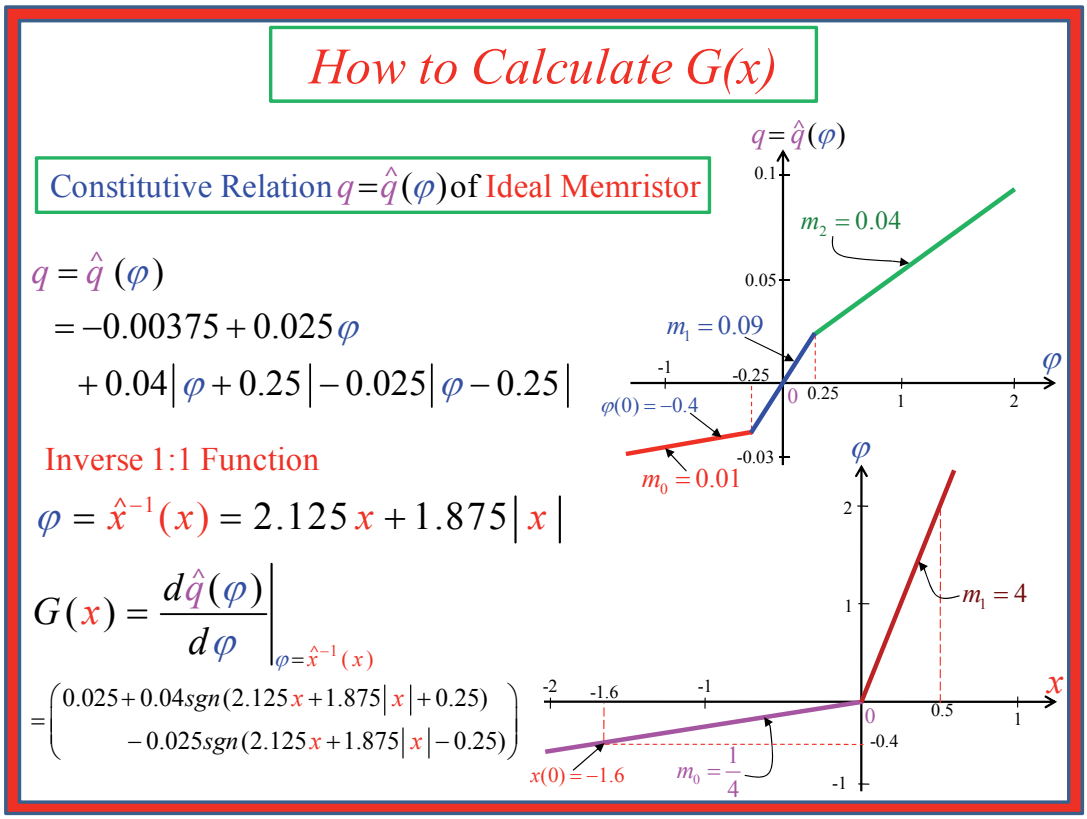


Fig. 8. Derivation of $G(x)$ via algebra.

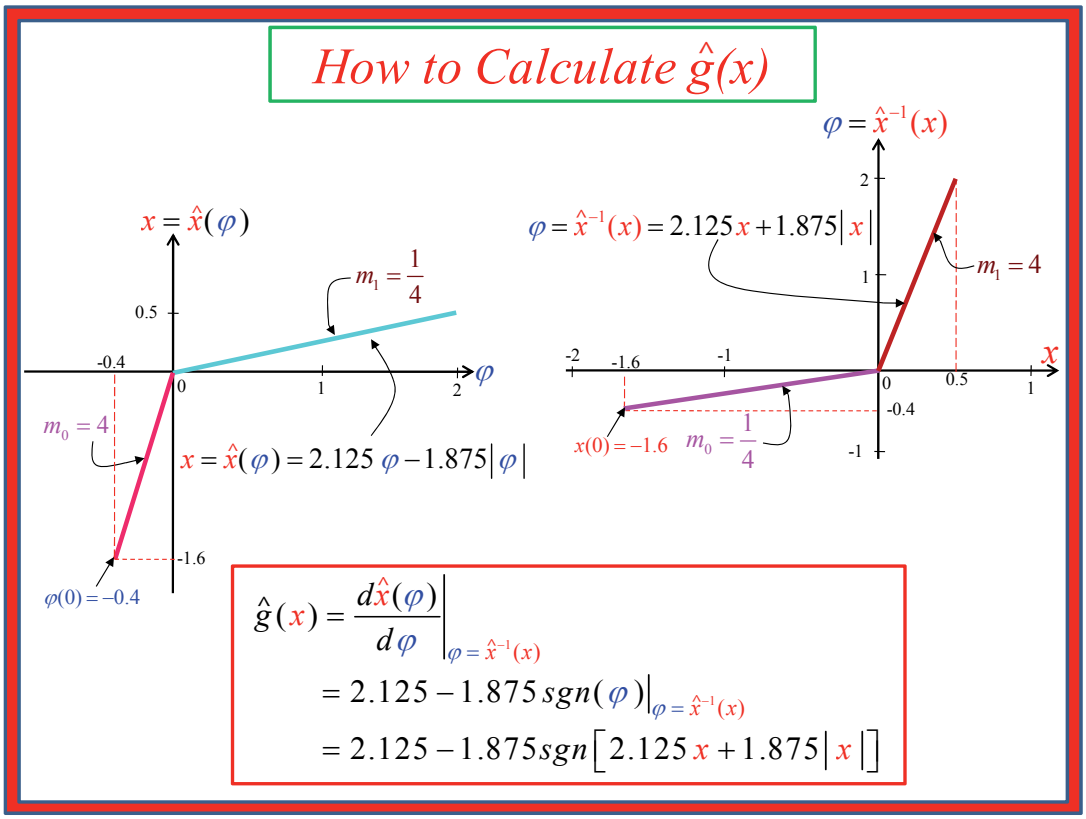


Fig. 9. Derivation of $\hat{g}(x)$ via algebra.

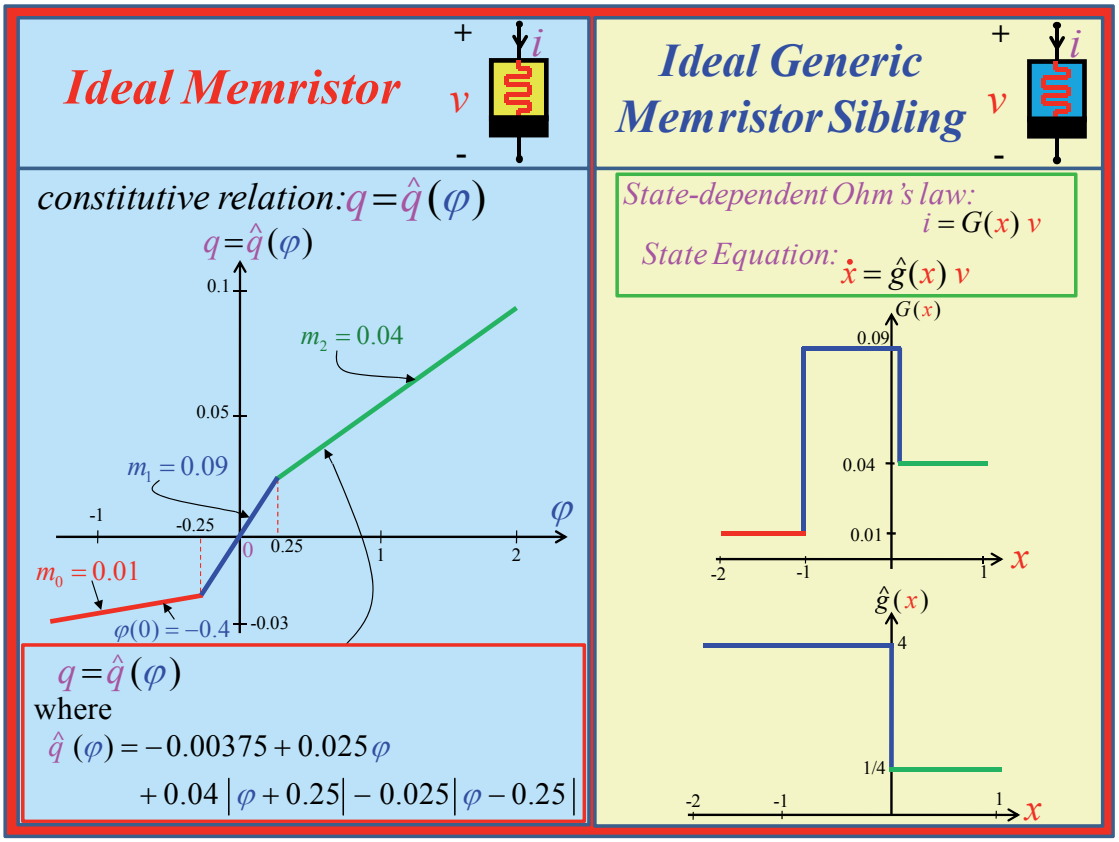


Fig. 10. The constitutive relation of a flux-controlled ideal memristor (left) and the state-dependent Ohm's law and state equation of its associated memristor sibling (right).

from each other. Indeed, if we apply the same voltage signal $v = 1.2 \sin t$ with initial flux $\varphi(0) = -0.4$ for the ideal memristor on the left, and[5]

$$\left.\begin{aligned} x(0) = \hat{x}\big(\varphi(0)\big) &= 2.125\,\varphi(0) - 1.875\,|\varphi(0)| \\ &= 2.125\,(-0.4) - 1.875\,|-0.4| \\ &= -1.6 \end{aligned}\right\} \qquad (10)$$

for the memristor sibling on the right side of Fig. 10, the waveform of $\varphi(t)$ (left column, row 2) and $x(t)$ (right column, row 2) as shown in Fig. 15 are very different indeed. Yet their respective memductance $G(t)$, current $i(t)$, and pinched hysteresis loop in Fig. 15 are identical.

We will summarize the above result as follows:

Identical Pinched Hysteresis Loop Theorem

Each ideal memristor, and its infinitely many *Ideal Generic Memristor Siblings*, exhibit *identical pinched hysteresis loops* in the voltage-current plane, when driven by the same input signal, with corresponding initial states.

4.4 Recovering Ideal Memristor from Its Siblings

Since any Ideal Generic Memristor Sibling gives the *same* pinched hysteresis loop as its associated *Ideal Memristor*, it makes sense to use the Ideal Memristor, which is characterized by only one scalar function (its constitutive relation), compared to two functions required for its memristor siblings, to perform all calculations and analysis. Tab. 4 (left column) shows the simple procedure to recover the memristance $\hat{R}(q)$ of the ideal current-controlled Memristor associated with any of its ideal generic memristor siblings[6].As an illustrative example, let us choose the memristor sibling given in the bottom-right corner of Tab. 3. The corresponding memristance $\hat{R}(q)$ is shown in the bottom-right corner of Tab. 4.

5. Generic Memristor

A memristor is called a *Generic Memristor* if its State-Dependent Ohm's Law and State Equation assumes the form shown in the second row of Tab. 1. Note the *Ideal*

[5]Recall the 1:1 function we used to derive the memristor sibling in Fig. 10 is defined by $x = \hat{x}(\varphi) = 2.125\varphi - 1.875|\varphi|$.

[6]The same algorithm applies for voltage-controlled memristors.

Example: Ideal Generic Memristor Sibling

Step 1: Choose

$$\varphi = q + \frac{1}{3}q^3 \triangleq \hat{\varphi}(q) \tag{1}$$

Step 2: Choose

$$x = q^3 \triangleq \hat{x}(q) \tag{2}$$

and its inverse

$$q = x^{1/3} \triangleq \hat{x}^{-1}(x) \tag{3}$$

Step 3: Apply $R(x) \triangleq \left.\frac{d\hat{\varphi}(q)}{dq}\right|_{q=\hat{x}^{-1}(x)}$ in (1)

$$R(x) = \left.\frac{d\hat{\varphi}(q)}{dq}\right|_{q=x^{1/3}} = \left.\left(1+q^2\right)\right|_{q=x^{1/3}} = 1 + x^{2/3} \tag{4}$$

Step 4: Apply $\hat{f}(x) \triangleq \left.\frac{d\hat{x}(q)}{dq}\right|_{q=\hat{x}^{-1}(x)}$ in (2)

$$\hat{f}(x) = \left.\frac{d\hat{x}(q)}{dq}\right|_{q=x^{1/3}} = \left.3q^2\right|_{q=x^{1/3}} = 3x^{2/3} \tag{5}$$

$$\boxed{\begin{aligned} v &= R(x)\, i \\ \frac{dx}{dt} &= \hat{f}(x)\, i \end{aligned}} \quad \Rightarrow \quad \boxed{\begin{aligned} v &= \left(1 + x^{2/3}\right) i \\ \frac{dx}{dt} &= 3x^{2/3}\, i \end{aligned}} \tag{6}$$

Tab. 3. Algorithm for creating an Ideal Generic Memristor Sibling from a current-controlled Ideal Memristor.

Recovering Ideal Memristor from its Sibling ?

Given:

State-Dependent Ohm's Law: $v = R(x)\, i$

State Equation: $\dfrac{dx}{dt} = f(x)\, i$; *where* $f(x) \geq 0$

Step: 1

Calculate $q = \int \left[\dfrac{1}{f(x)} \right] dx \triangleq h(x)$

Step: 2

Calculate *inverse function*:

$x = h^{-1}(q)$

Step: 3

Substitute $h^{-1}(q)$ for x in $R(x)$:

$R(x)\big|_{x=h^{-1}(q)} \triangleq \hat{R}(q)$

Step: 4

Ideal Memristor is describe by

$$v = \hat{R}(q)\, i$$
$$\frac{dq}{dt} = i$$

Example

Given:

State-Dependent Ohm's Law:

$$v = \underbrace{(1 + x^{2/3})}_{R(x)}\, i$$

State Equation: $\dfrac{dx}{dt} = \underbrace{\left(3x^{2/3}\right)}_{f(x)}\, i$

Step: 1

$q = \int \left[\dfrac{1}{3x^{2/3}} \right] dx = x^{1/3} \triangleq h(x)$

Step: 2

$x = h^{-1}(q) = q^3$

Step: 3

$R(x)\big|_{x=q^3} = (1 + x^{2/3})\big|_{x=q^3} = 1 + q^2 \triangleq \hat{R}(q)$

Step: 4 *Ideal Memristor*

$$v = \left(1 + q^2\right) i$$
$$\frac{dq}{dt} = i$$

Tab. 4. *Four-step Procedure* to recover the constitutive relation of an Ideal Memristor from any one of its infinitely many Ideal Generic Memristor Siblings [12].

Generic Memristor defined in the preceding section 4 differs from a Generic Memristor only in the form of their state equations, where the current i (resp., voltage v) in an Ideal Generic Memristor appears outside of the nonlinear function $\hat{f}(x)$ (resp., $\hat{g}(x)$).

Following are some example of real electronic devices whose mathematical models are *non-ideal Generic Memristors*.

Example 5.1 *Negative-temperature coefficient (NTC) thermistor* [6]

A voltage controlled *NTC thermistor* can be modeled as follow:

State-Dependent Ohm's Law: $i = W(x)\, v$ (11a)

State Equation : $\dfrac{dx}{dt} = \dfrac{\delta_N}{H_{CN}}(T_{0N} - x) + \dfrac{W(x)}{H_{CN}} v^2$ (11b)

The memductance $W(x)$ is defined by:

$$W(x) = \left[R_{ON}\; e^{\beta_N \left(\frac{1}{x} - \frac{1}{T_{0N}} \right)} \right]^{-1} \qquad (11c)$$

where $\delta_N, \beta_N, H_{CN}, R_{ON}, T_{0N}$ are constants, and the *state variable* x denotes the *NTC thermistor body temperature*.

Example 5.2 *Positive-temperature coefficient (PTC) thermistor* [6], [21]

A voltage controlled *PTC thermistor* can be modeled as follow:

State-Dependent Ohm's Law: $i = W(x)\, v$ (12a)

State Equation : $\dfrac{dx}{dt} = \dfrac{\delta_P}{H_{CP}}(T_{0P} - x) + \dfrac{W(x)}{H_{CP}} v^2$ (12b)

The memductance $W(x)$ is defined by:

$$W(x) = \left[R_{OP}\; e^{\beta_P (x - T_{0P})} \right]^{-1} \qquad (12c)$$

where $\delta_P, \beta_P, H_{CP}, R_{OP}, T_{0P}$ are constants, and the *state variable* x denotes the *PTC thermistor body temperature*.

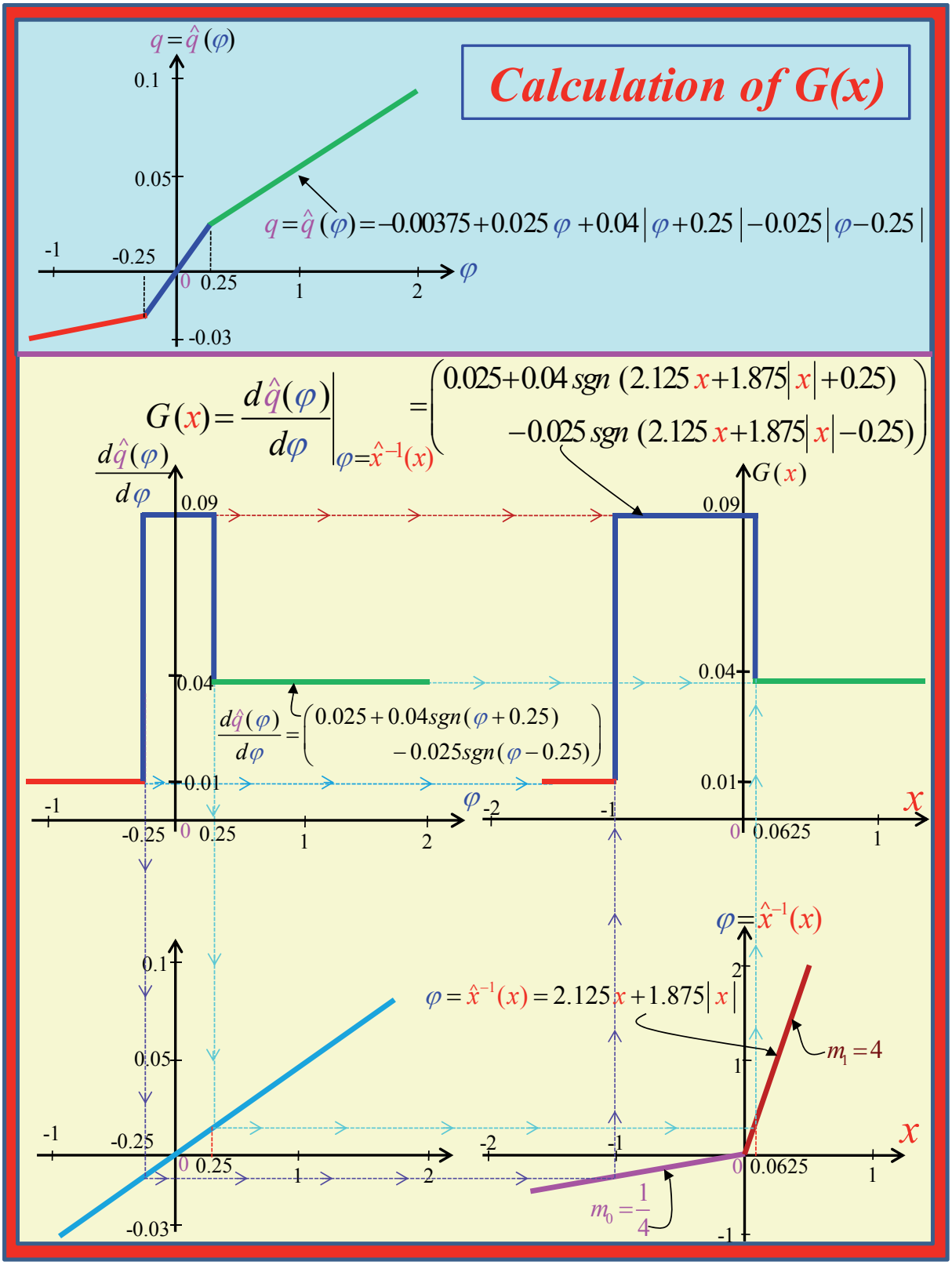


Fig. 11. The memductance $G(x)$ is derived graphically in the yellow part of the figure. The function $d\hat{q}(\varphi)/d\varphi$ (upper-left corner) and $\varphi=\hat{x}^{-1}(x)$ (lower-right corner) are given functions of φ and x, respectively. The memductance function $G(x)$ obtained by *graphical projections* of corresponding points on these 2 curves is shown in the upper-right corner.

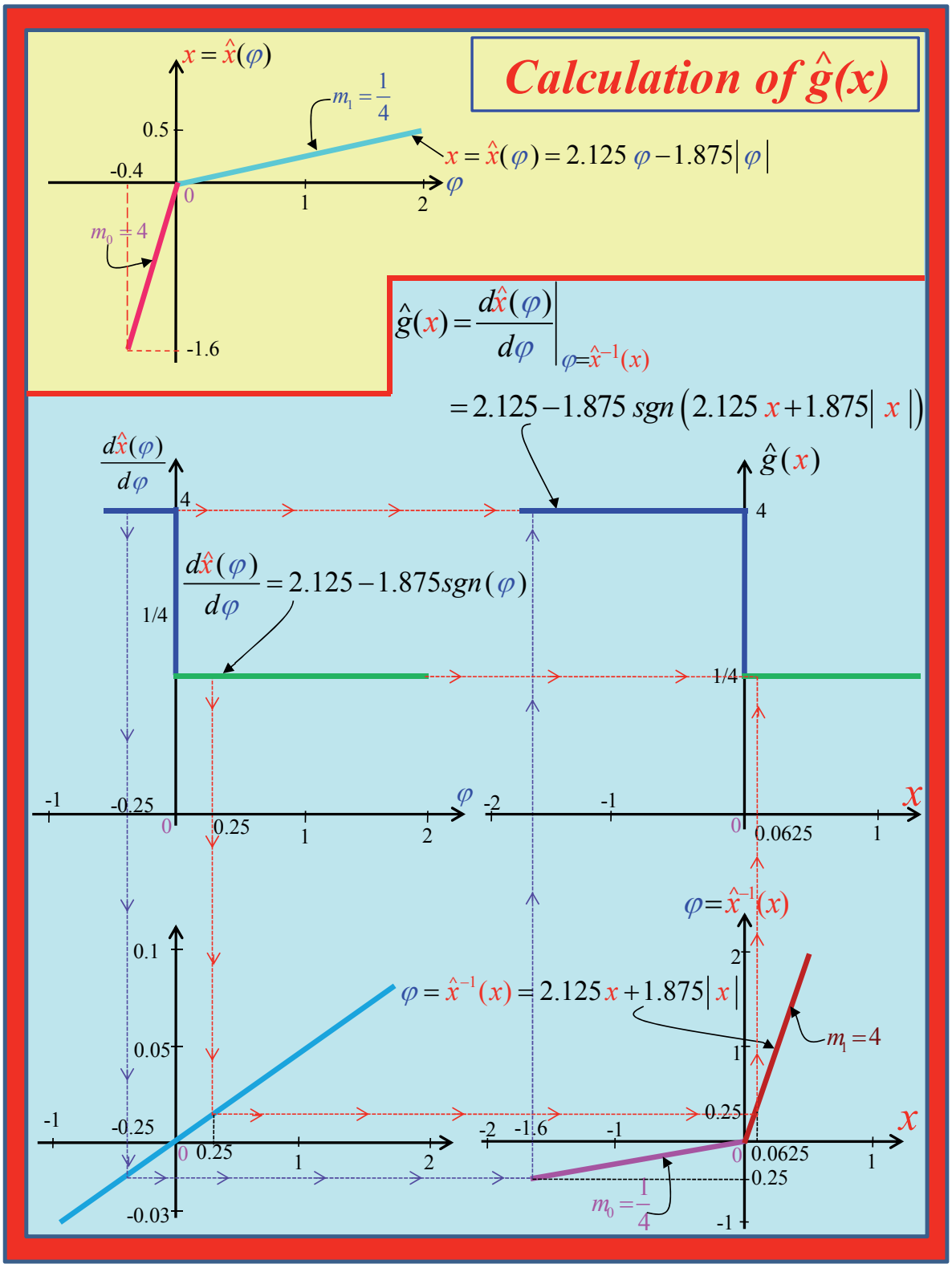


Fig. 12. The memristor *morphing function* $\hat{g}(x)$ is derived in the cyan part of the figure. The functions $d\hat{x}(\varphi)/d\varphi$ (upper-left corner) and $\varphi = \hat{x}^{-1}(x)$ (lower-right corner) are given functions of φ and x, respectively. The memristor morphing function $\hat{g}(x)$ obtained by *graphical composition* [24] of corresponding points on these 2 curves is shown in the upper-right corner.

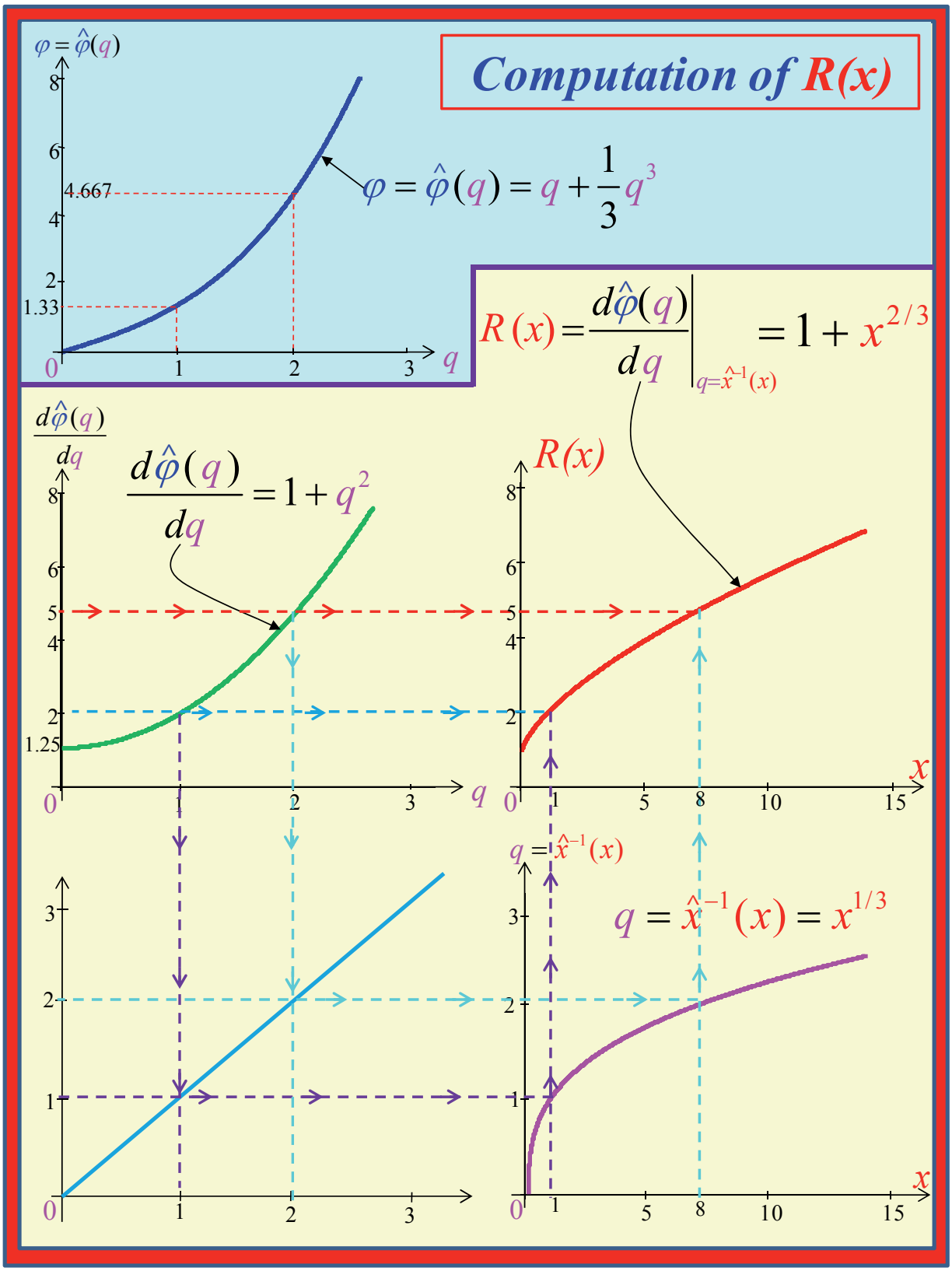


Fig. 13. The memristance $R(x)$ is derived graphically in the yellow part of the figure. The functions $d\hat{\varphi}(q)/dq$ (upper-left corner) and $q = \hat{x}^{-1}(x)$ (lower-right corner) are given functions of q and x, respectively. The memristance function $R(x)$ obtained by *graphical projections* of corresponding points on these 2 curves is shown in the upper-right corner.

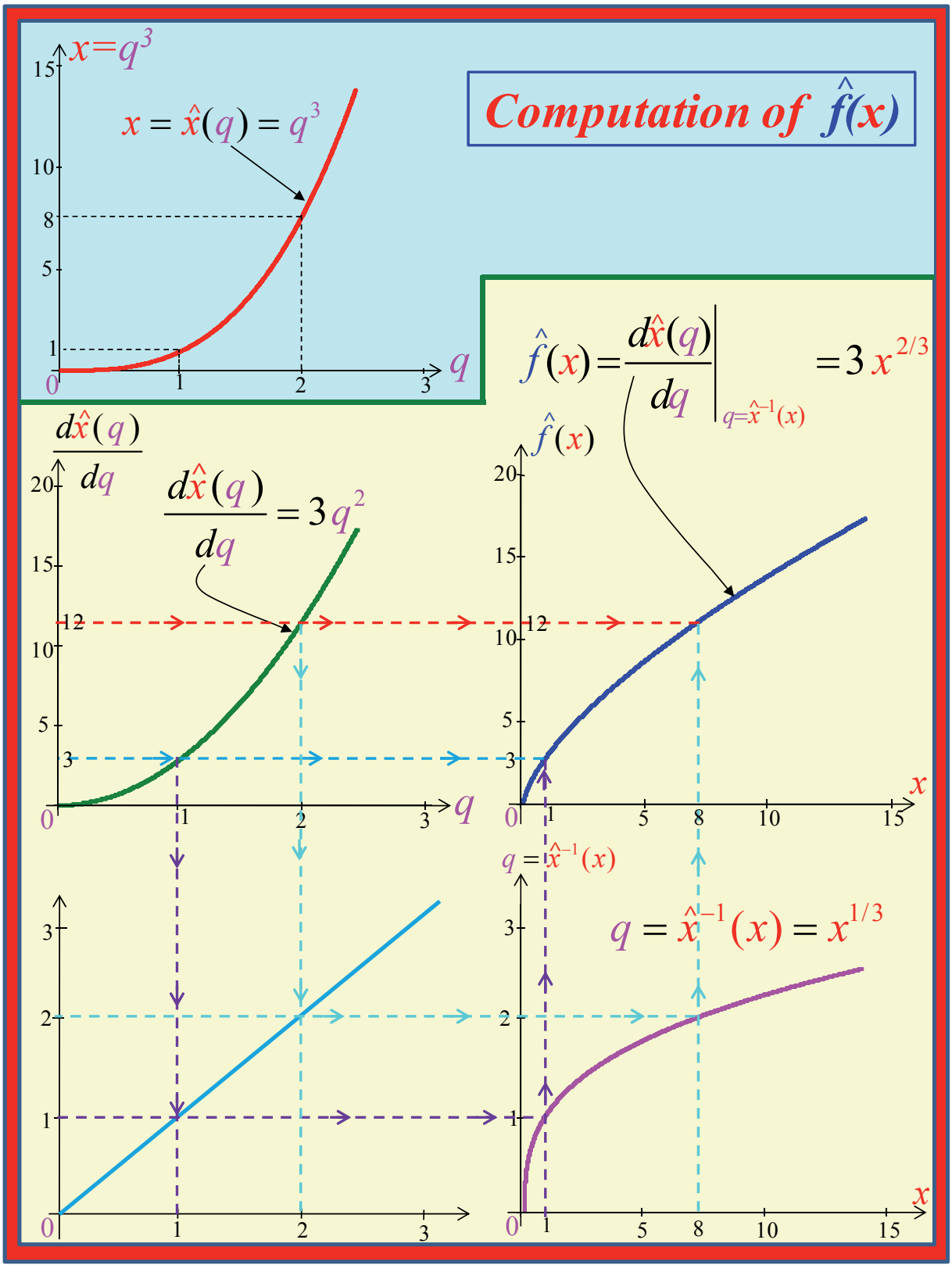


Fig. 14. The memristor *morphing function* $\hat{f}(x)$ is derived in the yellow part of the figure. The functions $d\hat{x}(q)/dq$ (upper-left corner) and $q=\hat{x}^{-1}(x)$ (lower-right corner) are given functions of q and x, respectively. The memristor morphing function $\hat{f}(x)$ obtained by *graphical composition* of corresponding points on these 2 curves is shown in the upper-right curve.

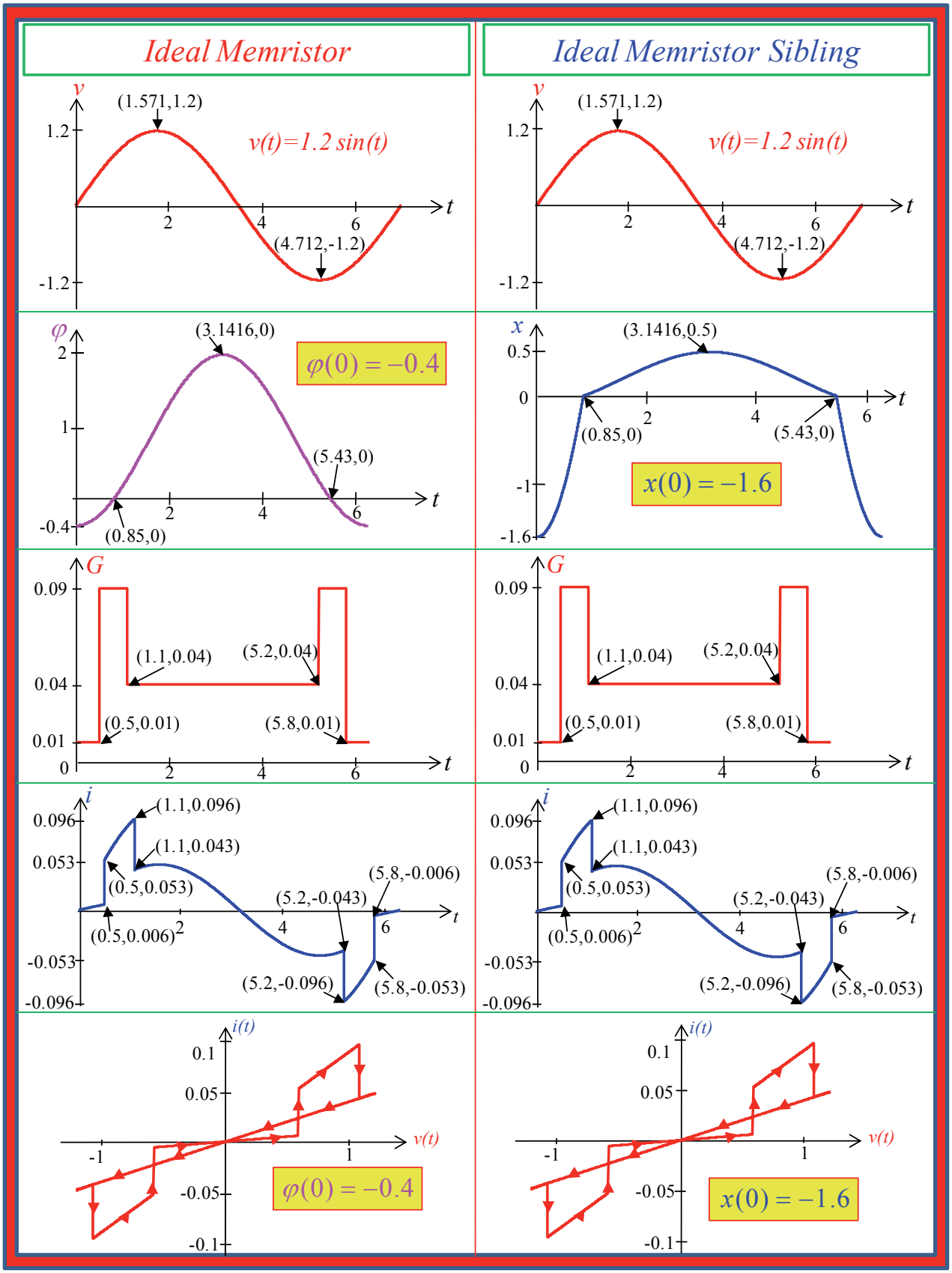


Fig. 15. The current $i(t)$ of an ideal memristor and any one of its siblings are identical when driven with the same input voltage, with corresponding initial states. Observe, however, that the flux $\varphi(t)$ of an ideal memristor is different from the state $x(t)$ of its corresponding memristor sibling.

Example 5.3 Hodgkin-Huxley Potassium Ion Channel [14]

State-Dependent Ohm's Law: $i = W(x)\, v$ (13a)

State Equation : $$\frac{dx}{dt} = f_n(x,\, v) \tag{13b}$$

The memductance $W(x)$ is defined by:

$$W(x) = \overline{g}_k\, x^4, \tag{13c}$$

$$f_n(x,\, v) \triangleq \left\{ \frac{0.01\left[(v + E_k) + 10\right]}{\exp\left[\frac{(v + E_k) + 10}{10}\right] - 1} \right\}(1 - x) - 0.125\left\{\exp\left[\frac{(v + E_k)}{80}\right]\right\} x \tag{13d}$$

where $\overline{g}_k, E_k$ are constants.

Example 5.4 Hodgkin-Huxley Sodium Ion Channel [14]

State-Dependent Ohm's Law: $i = G(x_1,\, x_2)\, v$ (14a)

State Equations : $$\frac{dx_1}{dt} = f_m(x_1,\, v), \tag{14b}$$

$$\frac{dx_2}{dt} = f_h(x_2,\, v) \tag{14c}$$

The memductance $G(x_1,\, x_2)$ is defined by:

$$G(x_1,\, x_2) = \overline{g}_{Na}\, x_1^{\,3}\, x_2, \tag{14d}$$

$$f_m(x_1,\, v) \triangleq \left\{ \frac{0.1\left[(v - E_{Na}) + 25\right]}{\exp\left[\frac{(v - E_{Na}) + 25}{10}\right] - 1} \right\}(1 - x_1) - 4\left\{\exp\left[\frac{(v - E_{Na})}{18}\right]\right\} x_1 \tag{14e}$$

$$f_h(x_2,\, v) \triangleq \left\{0.07 \exp\left[\frac{(v - E_{Na})}{20}\right]\right\}(1 - x_2) - \left\{ \frac{1}{\exp\left[\frac{(v - E_{Na}) + 30}{10}\right] + 1} \right\} x_2 \tag{14f}$$

where $\overline{g}_{Na}$, E_{Na} are constants.

Example 5.5 A Second-Order Memristor [15]

State-Dependent Ohm's Law: $i = G(x_1,\, x_2)\, v$ (15a)

State Equations : $$\frac{dx_1}{dt} = f_1(x_1, x_2,\, v) \tag{15b}$$

$$\frac{dx_2}{dt} = f_2(x_1, x_2,\, v) \tag{15c}$$

The memductance $G(x_1,\, x_2)$ is defined by:

$$G(x_1,\, x_2) = \frac{1}{\left(\left(K_1 e^{\beta_1 (x_1 - \gamma_1)}\right) + \left(K_2 e^{\beta_2\left(\frac{1}{x_2} - \frac{1}{\gamma_2}\right)}\right)\right)}, \tag{15d}$$

$$f_1(x_1, x_2, v) \triangleq \frac{1}{\alpha_1}\left[\delta_1 (\gamma_1 - x_1) + \frac{K_1 e^{\beta_1 (x_1 - \gamma_1)}}{\left(\left(K_1 e^{\beta_1 (x_1 - \gamma_1)}\right) + \left(K_2 e^{\beta_2\left(\frac{1}{x_2} - \frac{1}{\gamma_2}\right)}\right)\right)^2} v^2 \right], \tag{15e}$$

$$f_2(x_1, x_2, v) \triangleq \frac{1}{\alpha_2}\left[\delta_2 (\gamma_2 - x_2) + \frac{K_2 e^{\beta_2\left(\frac{1}{x_2} - \frac{1}{\gamma_2}\right)}}{\left(\left(K_1 e^{\beta_1 (x_1 - \gamma_1)}\right) + \left(K_2 e^{\beta_2\left(\frac{1}{x_2} - \frac{1}{\gamma_2}\right)}\right)\right)^2} v^2 \right] \tag{15f}$$

where $\alpha_1, \alpha_2, \beta_1, \beta_2, \delta_1, \delta_2, \gamma_1, \gamma_2, K_1$ and K_2 are constants.

Example 5.6 Hypothetical PWL Memristor [5]

State-Dependent Ohm's Law: $i = G(x)\, v$ (16a)

State Equation : $$\frac{dx}{dt} = f(x) + v \tag{16b}$$

The memductance $G(x)$ is defined by:

$$G(x) = G_0\, x^2 \tag{16c}$$

where G_0 is a constant.

The non-linear function defined by

$$f(x) = 30 - x + |x - 20| - |x - 40| \tag{16d}$$

is a 3-segment PWL function with breakpoints at $x = 20$ and $x = 40$, respectively, as shown in Fig. 16.

6. Extended Memristor

A memristor is called an *Extended Memristor* if its *memristance* $R(\boldsymbol{x}, i)$, or *memductance* $G(\boldsymbol{x}, v)$, is a function

of *not* only the state variables $\boldsymbol{x} = (x_1, x_2, \ldots\ldots, x_n)$, but also of the input current source i, or input voltage source v. In addition, the memristance $R(\boldsymbol{x}, 0)$, or memductance $G(\boldsymbol{x}, 0)$ must be a *finite* number when $i = 0$, or $v = 0$, respectively, as specified in the upper row of Tab. 1 [36].

In particular, a current-controlled device with $R(\boldsymbol{x}, 0) = \infty$, or a voltage-controlled device with $G(\boldsymbol{x},0)= \infty$, is *not* a memristor. Indeed, consider a voltage-controlled device described by

State-Dependent Ohm's Law: $i = G(x, v)\, v$ (17a)

State Equation : $\dfrac{dx}{dt} = g(x, v)$ (17b)

where the *memductance* $G(x, v)$ is defined by:

$$G(x,v) \triangleq \frac{x}{v} \tag{17c}$$

and

$$g(x,v) \triangleq v \ . \tag{17d}$$

Substituting (17c) into (17a), we obtain

$$i = \left(\frac{x}{v}\right) v = x \ . \tag{18}$$

Integrating (17b) with $x(0) = 0$, we obtain

$$x(t) = \int_0^t v(\tau)\, d\tau = \varphi(t), \quad t \geq 0 \ . \tag{19}$$

Substituting (19) for x in (18), we obtain

$$\varphi(t) = i(t) \tag{20}$$

which is the defining equation of a *1-Henry inductor!*

In other words, (17) defines an *inductor*, and *not a memristor*. The above mistaken identity is caused by the presence of an *infinite memductance* resulting from substituting $v = 0$ in (17c) :

$$\lim_{v \to 0} G(x,v) = \lim_{v \to 0} \frac{x}{v} = \infty \ . \tag{21}$$

Indeed, if we apply a sinusoidal voltage source

$$v = A \sin t \tag{22}$$

across the device defined by (17), with initial state $x(0) = -A$, we would obtain

$$x(t) = x(0) + \int_0^t A \sin \tau d\tau = -A \cos t \ . \tag{23}$$

It follows from (18) that

$$i(t) = -A \cos t \ . \tag{24}$$

Observe from (22) and (24) that the loci of (22) and (24) in the i *vs.* v plane is a *circle* of *radius* A, namely,

$$v^2(t) + i^2(t) = A^2 \tag{25}$$

as depicted in Fig. 17.

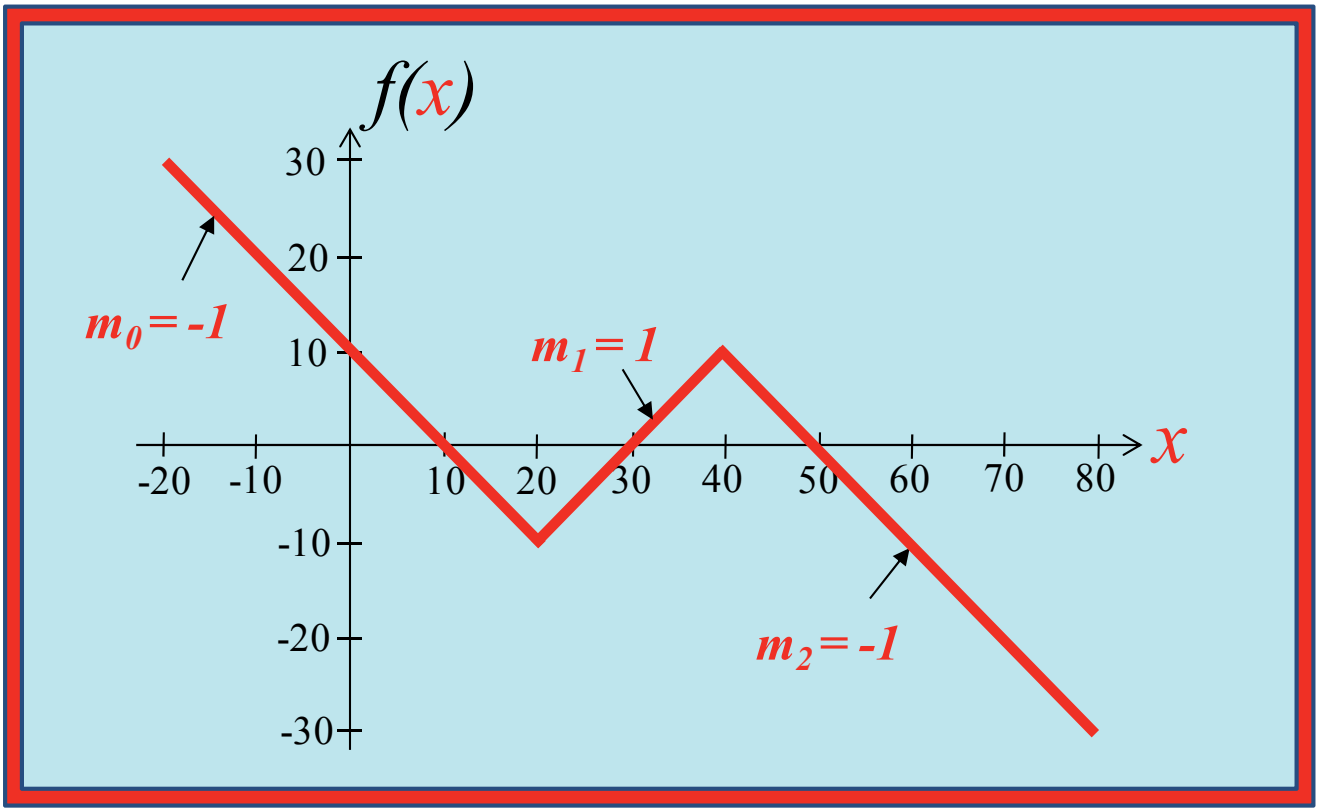


Fig. 16. The nonlinearity in the state equation (16b) is a 3-segment piecewise-linear (PWL) function with breakpoints at $x = 20$ and $x = 40$, and slopes $m_0 = -1$, $m_1 = 1$, and $m_2 = -1$.

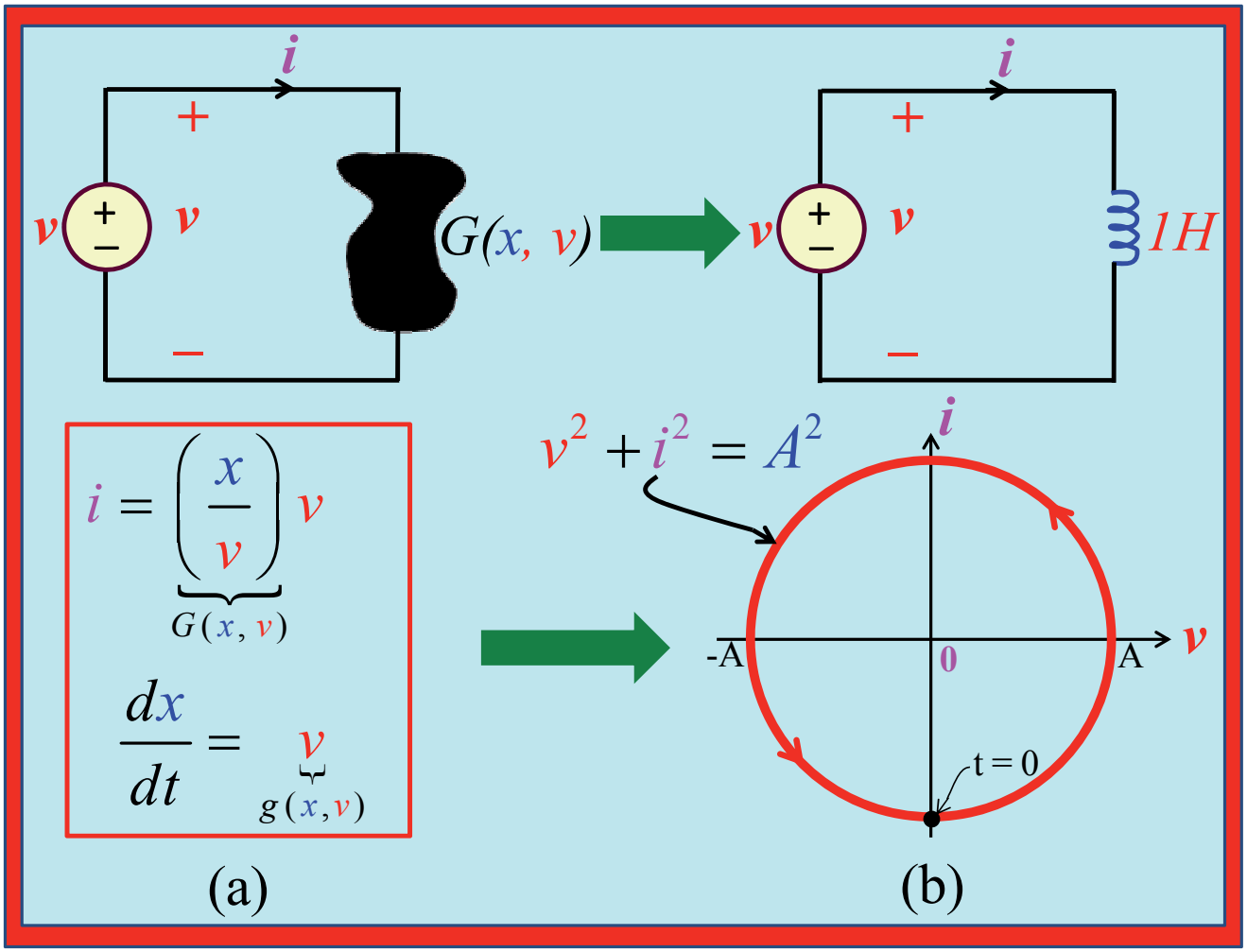


Fig. 17. Although the device shown in (a) is described by the same equations defining a voltage-controlled memristor in Tab. 1, the loci in the *i*-*v* plane when driven by a sinusoidal voltage source $v = A \sin t$ (with initial state $x(0) = -A$) is *not* a *pinched* hysteresis loop, but a *circle* with radius A, described by $v = A \sin t$, $i = -A \cos t$ as expected if the device defined in (a) is correctly identified as a 1H inductor.

It follows from the above example that if the hysteresis loop in the *v*-*i* plane of a 2-terminal device is not pinched, then it is NOT a memristor.

Following are two examples of an *Extended Memristor* where the denominator has the same form as (17), but $G(x, 0) \neq \infty$.

Example 6.1

State-Dependent Ohm's Law: $$i = \underbrace{x^3 \left(\frac{\sin v}{v}\right)}_{G(x,v)} v \qquad (26a)$$

State Equation : $$\frac{dx}{dt} = (x^2 - 1)\, v^3 \qquad (26b)$$

Observe that an application of the L'Hospital Rule [16] implies $\lim_{v \to 0} G(x,v) = \lim_{v \to 0} x^3 \left(\frac{\sin v}{v}\right) = x^3 \neq \infty$.

Example 6.2

State-Dependent Ohm's Law:

$$i = \underbrace{\left(x^3 + 2x^2 - x - 5\right)\left(\frac{v}{e^v - 1}\right)}_{G(x,v)} v \qquad (27a)$$

State Equation : $$\frac{dx}{dt} = e^x \sin v + x^3 v^5 \qquad (27b)$$

Observe that an application of the L'Hospital Rule [16] implies

$$\lim_{v \to 0} G(x, v) = \lim_{v \to 0} \left(x^3 + 2x^2 - x - 5\right)\left(\frac{v}{e^v - 1}\right) \qquad (28)$$
$$= x^3 + 2x^2 - x - 5 \neq \infty$$

7. Pinched Hysteresis Loop Fingerprints

It follows from the mathematical formulas defining the following *state-dependent Ohm's Law*

Current-Controlled State-Dependent Ohm's Law

$$v = R(q)\,i \quad \text{(Ideal Memristor and its Siblings)}$$
$$v = R(\mathbf{x})\,i \quad \text{(Generic Memristor)}$$
$$v = R(\mathbf{x}, i)\,i \quad \text{(Extended Memristor)}$$
$$R(\mathbf{x}, 0) \neq \infty \tag{29a}$$

Voltage-Controlled State-Dependent Ohm's Law

$$i = G(\varphi)\,v \quad \text{(Ideal Memristor and its Siblings)}$$
$$i = G(\mathbf{x})\,v \quad \text{(Generic Memristor)}$$
$$i = G(\mathbf{x}, v)\,v \quad \text{(Extended Memristor)}$$
$$G(\mathbf{x}, 0) \neq \infty \tag{29b}$$

from Tab. 1 that *all* Current-Controlled (resp., Voltage-Controlled) memristors must exhibit a *pinched hysteresis loop*, as depicted in Fig. 1 (resp., Fig. 2) when driven by *any periodic* current source $i(t)$ (resp., voltage source $v(t)$) with *zero mean*, assuming the voltage-response $v(t)$ (resp., current response $i(t)$) is periodic of the same frequency.

Because any *model*, by definition, is an *abstraction* of a real physical device [17], [33] no model can predict *exactly* the response of a real physical device imbedded in a circuit and driven by arbitrary voltage and current sources. Not even the time-honored *resistor* obeys Ohm's Law *exactly* because all resistors exhibit some *tiny but non-zero* parasitic effects, such as, capacitance, inductance, and whose resistance changes with temperature and frequencies. Likewise, no *real memristor* device is described exactly by (29a) or (29b). For example, in many biological (see Fig. 11, page no. 10 of [5]) [18], chemical [19], [34] and plant [20] memristors, the *pinched point* of the hysteresis loop is found to be *offset slightly* from the origin. If this departure from non-ideality can be modeled by introducing external parasitic circuit elements, voltage sources, and current sources, as illustrated in [21], then such a dominantly memristive device will be called an *imperfect memristor* [5].

Numerous examples of *pinched hysteresis loops* of memristors can be found in [3], [13], [22]. Not only do pinched hysteresis loops provide the characteristic fingerprints of *all* memristors, they all behave in a similar fashion as a function of the frequency of the periodic excitations [21]. In particular, it can be proved that beyond some *critical frequency* f^*, the area of each lobe of the pinched hysteresis loop of all memristors is a *strictly monotone-decreasing* function of the frequency f. Moreover, at sufficiently high frequencies, the pinched hysteresis loops must tend to *straight lines* (whose *slope* depends on the amplitude of the exciting periodic waveform) for all *Generic Memristors*, or to a *single-valued function* (whose precise curve varies with the amplitude of the periodic input signals) in the v *vs.* i plane for *all Extended Memristors* [21], [5], [36].

8. Coincident Zero-Crossing Signatures

While the *pinched hysteresis loop fingerprints* presented in the preceding section 7 provide necessary and sufficient conditions for identifying experimentally whether a device is a memristor, or not, the present section presents the most general experimental memristor identification scheme, dubbed the *Coincident Zero-Crossing Signatures*, thereby contributing to the circuit-theoretic foundation of memristors.

Indeed, the experimental testing scheme from Sec. 7 assumes that both the current waveforms $i(t)$, and the voltage waveforms $v(t)$, are periodic functions of the same frequency, and is therefore a special case of the present section, where any measured pairs of waveform $(i(t), v(t))$, be they periodic or not, must be included in the test. This is important from a circuit-theoretic perspective because one should be able to identify a memristor from the current-voltage waveform pairs $(i(t), v(t))$ measured from a memristor *in vivo*, i.e., with the memristor already connected in an arbitrary circuit, which may contain any type of circuit elements such as linear, and nonlinear resistors, capacitors, inductors, controlled sources, transistors, op-amps, other memristors, etc., powered by current sources and voltage sources [24], as depicted in Fig. 18(a). The Coincident Zero-Crossing Signature to be presented below also includes measured *transient* waveform pairs, such as the *sweat duct* measurement given in Fig. 10(d) of [25].

Fig. 18(a) depicts a circuit made of an arbitrary interconnection of circuit elements, including one or more memristors, current sources, and voltage sources. To enhance clarity let us pick, arbitrarily, one of the memristors and focus on the schematic showing only this memristor (on the right) connected to a cyan box representing the other part of the circuit (on the left) whose internal circuit diagram is irrelevant in the following discussion. In the special case where the cyan box contains only a current source $i(t)$ (resp., voltage source $v(t)$), Fig. 18(a) reduces to the current-controlled memristor setup in Fig. 1(resp., voltage-controlled memristor setup in Fig. 2).

Now let $(i(t), v(t))$ (resp.,$(v(t), i(t))$) denote a *corresponding pair* of waveforms measured experimentally from the memristor in Fig. 18(a), for some *prescribed initial conditions* at all dynamic circuit elements inside the cyan box - henceforth referred to as an *admissible signal pair* of the memristor. We assume that for each cyan box, and each set of internal initial conditions, there is a unique admissible signal pair that is measured. Consider next the *Gedanken* experiment where we change the cyan box to all possible circuits, while keeping the memristor in Fig. 18(a) unchanged. To each such experiment, we measured a cor-

responding admissible signal pairs ($i(t)$, $v(t)$) (resp., ($v(t)$, $i(t)$), for some prescribed internal initial states. We are now ready to state the following universal signatures exhibited by all memristors defined in Tab. 1.

Coincident Zero-Crossing Memristor Signatures:

The *waveform* of the voltage $v(t)$ (resp., current $i(t)$) associated with the current $i(t)$ (resp., voltage $v(t)$) of any admissible signal pair ($i(t)$, $v(t)$) (resp.,($v(t)$, $i(t)$) measured from the memristor setup in Fig. 18(a) must cross the time axis *whenever* $i(t) = 0$ (resp., $v(t) = 0$) .

The above memristor signatures follow directly from the prescribed form of the equation defining a current-controlled (resp., voltage-controlled) memristor in Tab. 1.

To clarify the application of the above universal memristor signatures, the waveforms of a hypothetical pair of admissible signal pair ($i(t)$, $v(t)$) (resp., ($v(t)$, $i(t)$) of a current-controlled (resp., voltage-controlled) memristor are shown in Fig. 18(b) (resp., Fig. 18(c)).

Observe from Fig. 18(b) (resp., Fig. 18(c)) that the Coincident Zero-Crossing Signature asserts *only* that the waveform of the voltage $v(t)$ (resp., current $i(t)$) of a current-controlled (resp., voltage-controlled) memristor must cross the time axis at the same instants of time whenever the waveform of the current $i(t)$ (resp., voltage $v(t)$) crosses the time axis.

It is important to understand that the statement of the Coincident Zero-Crossing Signatures *does not* forbid the waveform of the voltage $v(t)$ (resp., current $i(t)$) from also crossing the time axis at other instants of time where the current $i(t)$ (resp., voltage $v(t)$) is *not* zero, as illustrated in Fig. 18(b) (resp., Fig. 18(c)). Such situations can in fact occur if the memristor is *active*[7], compared to *passive* memristors where the memristance $R(x, i) \geq 0$ (resp., memductance $G(x, v) \geq 0$).

Example 8.1: Active Memristor

The circuit shown in Fig. 19(a) consists of a current-controlled memristor in series with a passive linear capacitor C and inductor L. The memristor is described by:

$$\text{State-Dependent Ohm's Law :} \quad v = R(x)\, i \tag{30a}$$

$$\text{State Equation :} \quad \frac{dx}{dt} = f(x, i) \tag{30b}$$

where

$$R(x) = \beta\left(x^2 - 1\right), \tag{30c}$$

$$f(x, i) = i\,(1 - x) - \alpha\, x\,. \tag{30d}$$

This memristor is *active* because its memristance $R(x)$ is negative for some values of x; namely,

$$R(x) < 0, \quad \text{for } -1 < x < 1\,. \tag{31}$$

Since *active* electronic devices can be used to amplify electrical energy, it does not exist as an intrinsic device, such as a p-n junction diode, or a thermistor, but it can be built from off-the-shelf components, such as transistors and op-amps, powered by an energy source, such as a battery. Indeed, the above active memristor has been built [26] and its measured memristance $R(x)$, shown in Fig. 19(b), closely resembles that defined in (30c).

For readers unfamiliar with the fundamentals of Nonlinear Circuit Theory [24] we wish to point out that the electronic circuit schematic given in Fig. 44, p. 35 of [5] is a *physical* 2-terminal memristor *device*, and *not* an analog computer, or an emulator. Indeed, the circuit inside the box in Fig. 44 of [5] can be integrated into a single chip with 2 memristor terminals. From a circuit-theoretic perspective, the power supply needed to power the transistors and op-amps is imbedded *inside* the box in Fig. 44(a) of [5], and hence the device has only 2 external terminals. In fact, one can in principle replace the battery by integrating an array of solar cells inside the chip, with a small window for accessing sun lights.

The circuit in Fig. 19(a) is an example of Fig. 18(a), where the cyan box consists of a linear capacitor in series with a linear inductor. The circuit in Fig. 19(a) is remarkable in the sense that it not only can function as an oscillator (for some values of L and C), but it can generate *chaotic* oscillations (for some other values of L and C) whose waveforms are *not* periodic, but persist indefinitely as *transients*, somewhat reminiscent of *amplified* noisy signals.

For example, Fig. 19(c) shows the chaotic waveforms of the memristor current $i(t)$, and memristor voltage $v(t)$, measured from the circuit in Fig. 19(a). Observe that the zero-crossing points of $v(t)$ include not only *all* zero-crossing points of $i(t)$, but also several additional instants of time when $i(t)$ is not zero (such as between $t = 40$ and $t = 50$, and between $t = 90$ and $t = 100$), thereby providing the signature of a *current-controlled* memristor. The presence of zero-crossing points of $v(t)$ which were not present in $i(t)$ manifests, in this example, as points in the 2nd and 4th quadrant of the v-i plane, when the loci of $v(t)$ and $i(t)$, also known as a *Lissajous figure*, is projected onto the v *vs.* i plane, as shown in Fig. 19(d)[8].

[7] A current-controlled (resp., voltage-controlled) memristor is *passive if, and only if*, its memristance $R(x, i) \geq 0$ (resp. memductance $G(x, v) \geq 0$). A memristor is *active if, and only if*, it is *not passive*.

[8] Fig. 19(d) illustrates why the *Coincident Zero-Crossing signature* is more general than that of a *pinched hysteresis loop fingerprint*; namely, since both $i(t)$ and $v(t)$ waveforms are *not* periodic, their associated Lissajous figure is *not* a *closed* loop, but an unending loci, which if left to continue printing unstopped would eventually lead to a uniformly blue color inside each lobe. But remarkably, both blue lobes would share a common *pinched* point at the origin at all times, thereby confirming the nonlinear device defined in Fig. 19(a) is a *memristor*.

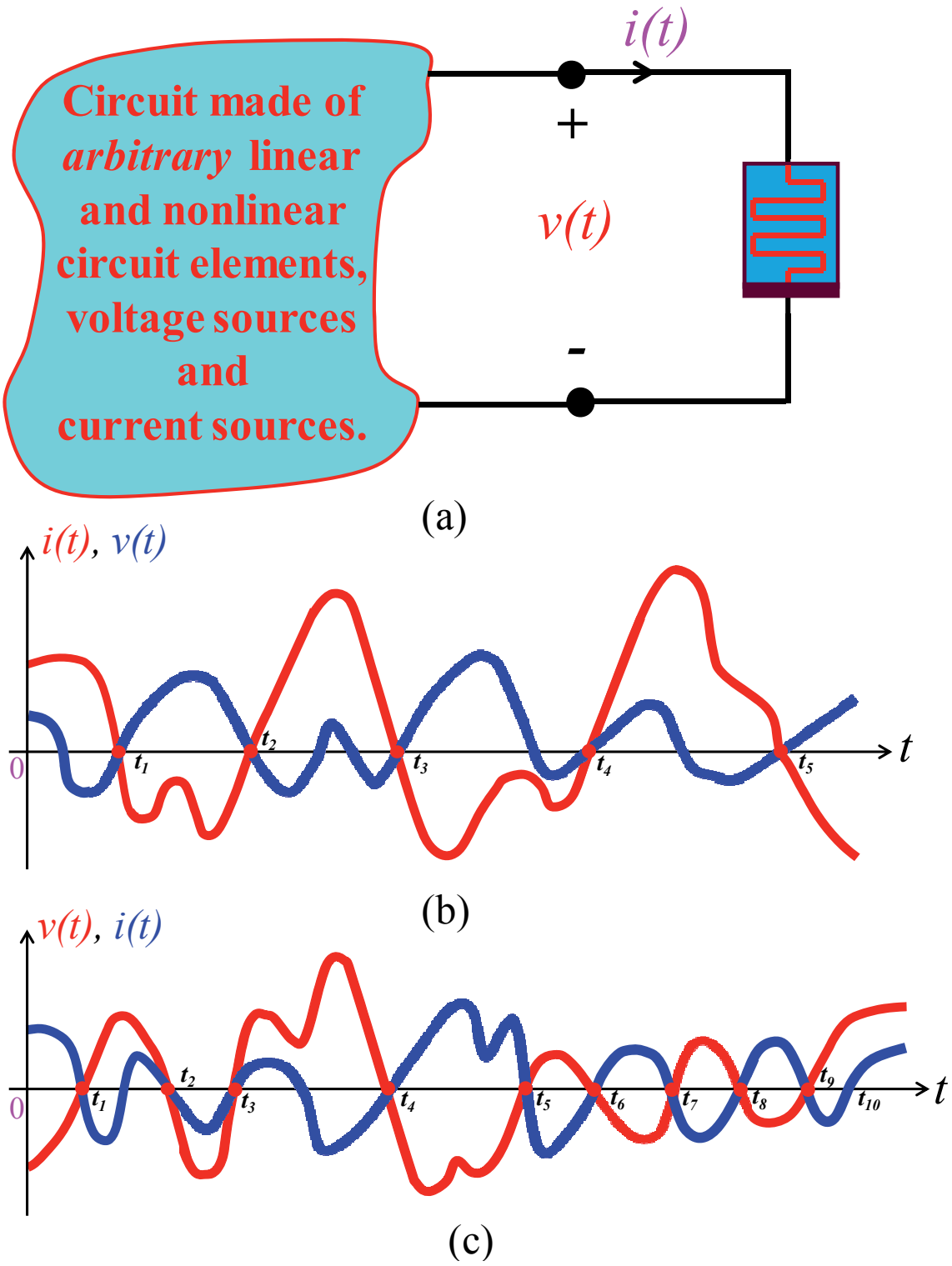


Fig. 18. Illustrations of *Coincident Zero-Crossing Signatures*.

(a) A memristor imbedded in a circuit is highlighted by redrawing it outside of the cyan box for analysis. It is assumed the voltage waveform $v(t)$ across the memristor, and the current waveform $i(t)$ entering the memristor have been measured and available for analysis.

(b) The pair of waveforms ($v(t)$, $i(t)$) in (b) implies the memristor shown on the right side of (a) is a *current-controlled* memristor defined by one of the 3 formulas in (29a), where $v(t) = 0$ whenever $i(t) = 0$, as depicted in Fig. 1. Note that $v(t)$ may intersect the time axis at additional points (e. g., the intersections of the blue waveform with the time axis between $t = 0$ and t_1, between t_2 and t_3, and between t_4 and t_5) where $i(t) \neq 0$.

(c) The pair of waveforms ($i(t)$, $v(t)$) in (c) implies the memristor shown on the right side of (a) is a *voltage-controlled* memristor defined by one of the 3 formulas in (29b), where $i(t) = 0$ whenever $v(t) = 0$, as depicted in Fig. 2. Note that $i(t)$ may intersect the time axis at additional points (e. g., the intersections of the blue waveform with the time axis between t_1 and t_2, between t_3 and t_4, and $t > t_9$) where $v(t) \neq 0$.

8.1 Passive Memristors Have Identical Zero Crossings

The set of *zero crossing* times $\{t_1(i), t_2(i),\ldots,t_M(i)\}$ of the current waveform $i(t)$ and $\{t_1(v), t_2(v),\ldots, t_N(v)\}$ of the voltage waveform $v(t)$ associated with a *passive* memristor are *identical*. In particular, $t_k(i) = t_k(v)$, and $M = N$.

The proof of the above property follows from an inspection of Fig. 1 and Fig. 2 where the pinched hysteresis loops ventures into the 4th quadrant, whereby the instantaneous power

$$p(t) = v(t)\, i(t) < 0 \tag{32}$$

implying that *power* is being *discharged* by the memristor into the cyan box at all time instants when (32) holds. But this is impossible because $R(x, i) > 0$ and $G(x, v) > 0$ for a *passive* memristor, implying

$$p = vi = M(x, i)\, i^2 > 0 \tag{33a}$$

for all times t, thereby contradicting (32), and

$$p = iv = G(x, v)\, v^2 > 0\ . \tag{33b}$$

It follows from the above analysis that the pinched hysteresis loops of all *passive* memristors are restricted to the first and the third quadrants of the v-i plane, and that the set of *zero-crossing* times of both $i(t)$ and $v(t)$ of *passive* memristors are identical.

8.2 Passive Memristors Have Zero Phase Shifts

The above zero-crossing property among passive memristors implies the following additional fundamental property:

Zero Phase Shift Property:

The *phase shift*[9] between a periodic current waveform $i(t)$ (resp., voltage waveform $v(t)$) and its associated periodic voltage waveform $v(t)$ (resp., current waveform $i(t)$) of the same frequency in any *passive* memristor is zero.

We close this section by observing that the above *Zero Phase - Shift* property implies that unlike capacitors, and inductors, it is impossible to store energy in a passive memristor.

9. P O P: Power-Off Plot

The following very short discourse deserves a separate section because it provides the answer to the following question everybody wishes, but is afraid, to ask:

WHEN IS A MEMRISTOR NON-VOLATILE ?

The answer to the above *nagging* question is found by plotting the loci - henceforth called *Power-Off Plot*, or simply *POP* - of the *rate of change* (dx/dt) (defined by the right-hand side $f(x, i)$ (resp., $g(x, v)$) in the memristor *state equation*) as a function of the *state variable* x with the input current i (resp., input voltage v) in the current-controlled state equation (resp., voltage-controlled state equation) in Tab. 1 set equal to zero.

In the special case where the state variable x is a *scalar*, POP is just a curve in the $f(x,0)$ *vs.* x plane (resp., $g(x,0)$ *vs.* x plane).

Example 9.1: POP of Positive – Temperature Coefficient Thermistor

The POP of the current-controlled memristor (Positive-Temperature Coefficient thermistor in Example 5.2) defined in (12) is just a straight line (Fig. 20) defined by

$$\frac{dx}{dt} = \frac{\delta_P}{H_{CP}}(T_{0P} - x) \tag{34}$$

The upper arrowhead pointing *to the right* indicates that the solution $x(t)$ starting from any initial state $x(0) \neq x(Q)$ on POP *above* the x-axis must move to the right of $x(0)$ (because $(dx/dt) > 0$ at $x(0)$) for $t > 0$, as long as $x(t)$ lies above the x-axis.

Conversely, the lower arrowhead pointing *to the left* indicates that the solution $x(t)$ starting from any initial state $x(0) \neq 0$ below the x-axis on POP must move to the left of $x(0)$ (because $(dx/dt) < 0$) for $t > 0$,as long as $x(t)$ lies below the x-axis.

Each intersection of POP with the x-axis is called an *equilibrium point* of the *power-off* memristor because $(dx/dt) = 0$ at such intersections, implying that the state $x(t)$ starting from an initial state $x(0) = x(Q)$ must remain *motionless* at $x(t) = x(Q)$ for $t > 0$.

The *equilibrium point* $x = x(Q)$ in Fig. 20 is said to be *asymptotically stable*[10] in the *Theory of Nonlinear Dynamics* [27] because the solution $x(t)$ starting from any initial state $x(0) \neq x(Q)$ *must* tend to the *equilibrium point* $x = x(Q)$ as $t \to \infty$.

It follows from Fig. 20 that the state variable $x(t) \to x(Q)$ in (12b) (with $v = 0$) and its memductance

$$W(x(t)) \to W(x(Q)) = \left[R_{OP} e^{\beta_P (x(Q) - T_{0P})}\right]^{-1} = \frac{1}{R_{OP}} \tag{35}$$

[9] The *phase shift* between two periodic waveforms $i(t)$ and $v(t)$ of the same frequency is the distance in time measured between their two closest zero crossings.

[10] The adjective *asymptotically* is used in a *mathematical* sense meaning that $x(t)$ will not arrive at $x(t) = x(Q)$ at a *finite* time.

as $t \to \infty$, for any initial state $x(0)$. In other words, the *Power-Off* PTC memristor is equivalent to a linear passive resistor with resistance equal to R_{OP} at ambient temperature $T = 300$ K. Such a memristor is said to be *volatile* because the initial condition $x(0)$ (which can be interpreted as a summary of the *past* history of $x(t)$) has no effect on the value of the *small-signal* resistance $(\delta v(t)/\delta i(t))$ measured from this memristor by applying an infinitesimal voltage $\delta v(t)$ across the memristor and measuring its current response $\delta i(t)$. It is *volatile* in the sense that the effect of the past input signals that this memristor has been subjected to have been forgotten.

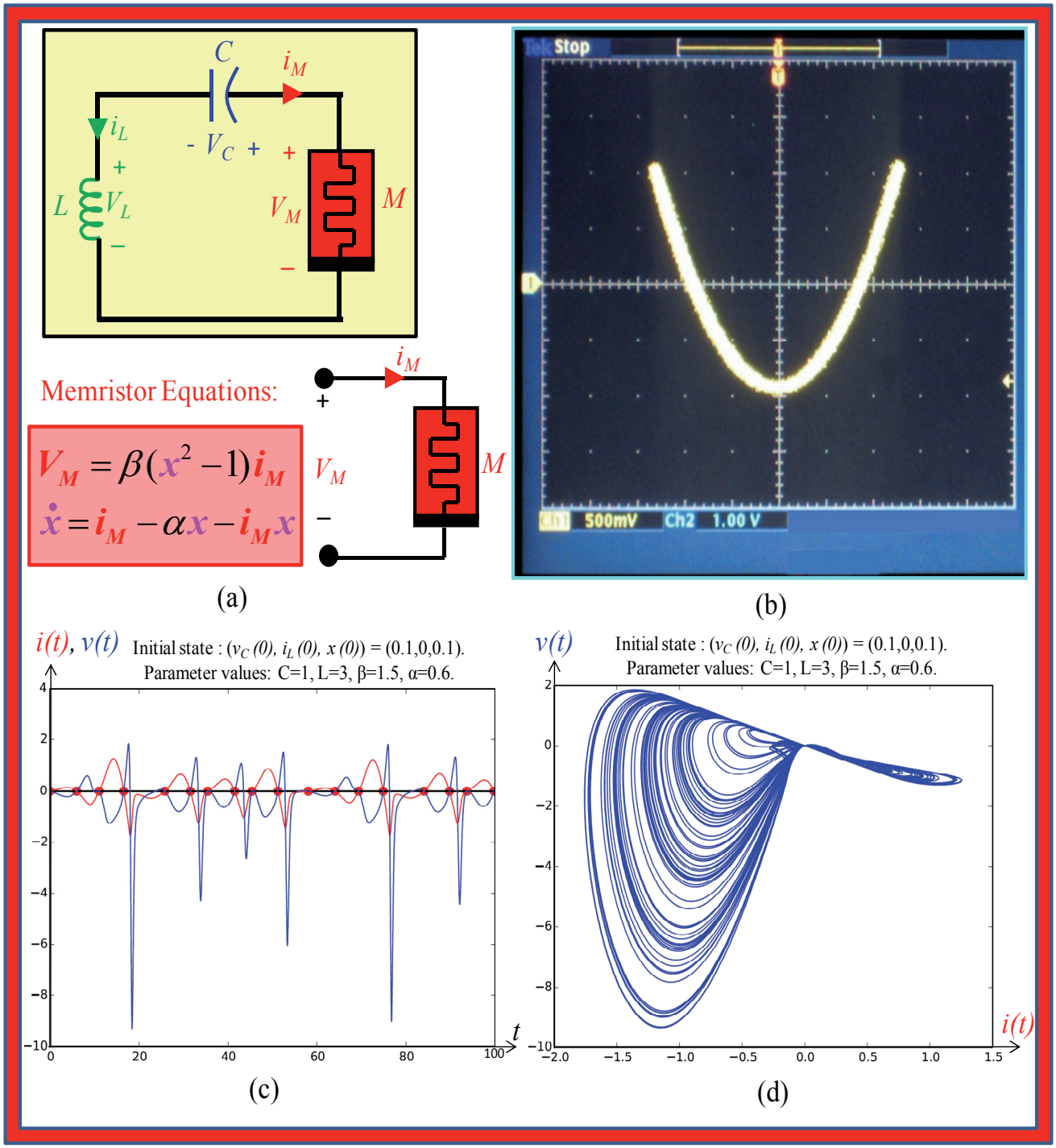


Fig. 19. A 3-element chaotic circuit with the memristor providing *both local activity* and *nonlinearity* essential for generating *chaotic* oscillations [28]. Such a memristor – called a *locally-active memristor* – can be built using transistors, op-amps, etc., powered by a battery [5], [26]. The memristance $R(x)$ measured from this 2-terminal *electronically-synthesized* memristor is shown in (b), where the horizontal and vertic*al axes represent the memristor current i(M) and voltage v(M) in (a). The pair of numerically – calculated red current waveform* $i(t)$ and blue voltage waveform $v(t)$ in (c) are *non-periodic.* Their associated Lissajous figure in (d) is called a *strange attractor* [29]. Observe that though not a closed loop, it is pinched at the origin.

Example 9.2 : POP of Hypothetical Memristor

The POP of the hypothetical voltage-controlled generic memristor defined earlier in (16) is given in Fig. 16. It has 3 equilibrium points located at $x = 10$, $x = 30$, and $x = 50$, respectively, where $dx/dt = 0$.

We can indicate the direction of motion along the POP by attaching an arrowhead pointing to the right (resp., to the left) on each segment of the PWL function lying above (resp., below) the x-axis where $dx/dt > 0$ (resp., $dx/dt < 0$), as shown in Fig. 21, where the 3 equilibrium points are labeled as Q_0 ($x = 10$), Q_1 ($x = 50$), and Q_2 ($x = 30$), respectively. Such a diagram depicting the motion of $x(t)$ in the (dx/dt) vs. x plane is called a *dynamic route* [24].

Observe that while each intersection of the POP in Fig. 16 with the x-axis is an *equilibrium point* of a circuit made of a voltage-controlled (resp., current-controlled) memristor, terminated by a *short circuit* (resp., an *open circuit*), the associated *dynamic route* provides additional information for classifying each equilibrium point on the POP as asymptotically *stable*, or *unstable*. For the memristor in Example 9.2, the dynamic route in Fig. 21 identifies the equilibrium points Q_0 and Q_1 to be asymptotically *stable*, whereas the equilibrium point Q_2 is identified to be *unstable*.

A cursory inspection of the dynamic route in Fig. 21 shows that it is endowed with a *non-volatile* memory in the sense that, depending on the initial state $x(0)$, the memristor can exhibit one of two *asymptotically stable* equilibrium states, namely,

$$x = x(Q_0) = 10, \text{ if } x(0) < 30 \qquad (36a)$$

$$= 50, \text{ if } x(0) > 30. \qquad (36b)$$

These 2 distinct equilibrium states give rise to the following 2 corresponding *stable* small-signal conductance (assuming $G_0 = 1$ in (16c))[11]

$$W\left(x(Q_0)\right) = (10)^2 = 100\ S, \quad if \quad x(0) < 30 \qquad (37a)$$

$$= (50)^2 = 2500\ S, \quad if \quad x(0) > 30 \qquad (37b)$$

Since the 2 distinct stable values of the memductance $W(x(Q_0))$ can be used to represent the *binary* state 0, or 1, this memristor is said to be a *non-volatile* memory because the memductance $W = 100$ S, or $W = 2\,500$ S is retained for all times $t > 0$, until an appropriate external voltage signal is applied to switch the equilibrium state to the other stable state.

The above example can be easily generalized into a theorem:

Non-Volatile Memristor Theorem:

A memristor with a scalar state variable x is *non-volatile* if its POP intersects the x-axis at 2 or more points with a *negative slope*.

Example 9.3: POP of a Continuum-Memory Memristor

Consider a hypothetical Extended Voltage-Controlled memristor described by :

State-Dependent Ohm's Law:	$i = G(x, v)\, v$ $G(x, 0) \neq \infty$	(38a)
State Equation :	$\dfrac{dx}{dt} = g(x, v)$	(38b)

where

$$g(x, v) \triangleq \frac{v}{x}. \qquad (38c)$$

Let us leave $G(x, v)$ in (38a) unspecified in this example in order to emphasize that *non-volatile memories* of memristors are determined by the intersection points of their POP (*Power – Off Plot*) with the x-axis, and therefore does not need the memductance function $G(x, v)$.

The POP of the above memristor (obtained by setting $v = V = 0$) in (38c) is given by

$$\text{POP}: \frac{dx}{dt} = \frac{0}{x} = 0 \qquad (39)$$

as shown by the bold red line in Fig. 22, namely, the entire x-axis. It follows that the above memristor is endowed with a *continuum of stable* (but *not asymptotically stable*) equilibrium points[12]. We will henceforth call a memristor whose POP coincides with the x-axis as a *Continuum-Memory Memristor*[13]. Since every state $x(Q) \in (-\infty, \infty)$ of a *Continuum-Memory Memristor* gives rise to a conductance determined by the memductance function $G(x, v)$ evaluated at $x = X_Q$, and $v = V_Q$, this memristor is endowed with a continuum of *non-volatile* non-negative conductance memories, assuming that $G(x, 0)$ assumes all values of $G(x, 0) \geq 0$ over the x-axis.

In the case where the memductance function $G(x, 0)$ is a smooth function x, then this memristor can be used as a *synapse* [3], [32], [35] in *brainslike* machines.

[11] To simplify arithmetic, we pick $G_0 = 1$. In practice, G_0 is a scaling constant chosen to fit the intrinsic memductance scale of the memristor.

[12] An equilibrium point $x(Q)$ of a differential equation $\dot{\boldsymbol{x}} = \boldsymbol{f}(\boldsymbol{x})$ is said to be *asymptotically stable* if a small ball placed initially at $x(Q)$ will always return to $x(Q)$ when it is displaced by an arbitrarily small perturbation of arbitrarily short duration by following the direction of motion indicated by the arrowhead along the dynamic route where the perturbed state $\hat{x} = x(Q) + \Delta x$ is located. If the perturbed state $\hat{x}$ did not return to $x(Q)$, but remains motionless after the perturbation Δx became zero, then the equilibrium point is said to be *stable*.

[13] For a more comprehensive theory on non-volatile memories, we can generalize our definition of a *Continuum-Memory Memristor* to allow its POP to contain only one, or more, contiguous intervals $a \leq x \leq b$ on the x-axis, such as the 2 intervals [–2, –1] and [1, 2] in Fig. 35 of [5].

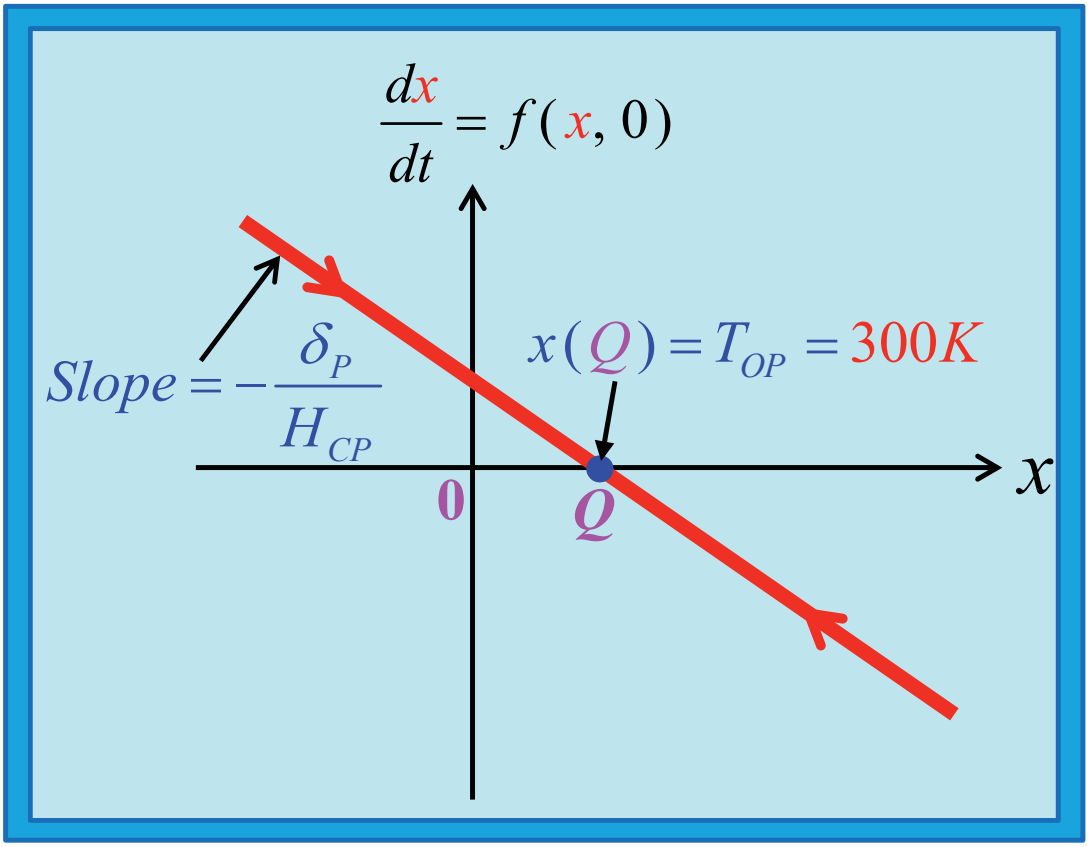


Fig. 20. POP of the current-controlled *Positive-Temperature Coefficient (PTC)* thermistor where $\delta_P = 0.8$ W/K, $H_{CP} = 0.8$ J/K, $T_{OP} = 300$ K. The arrowhead points to the direction of motion of x on the POP.

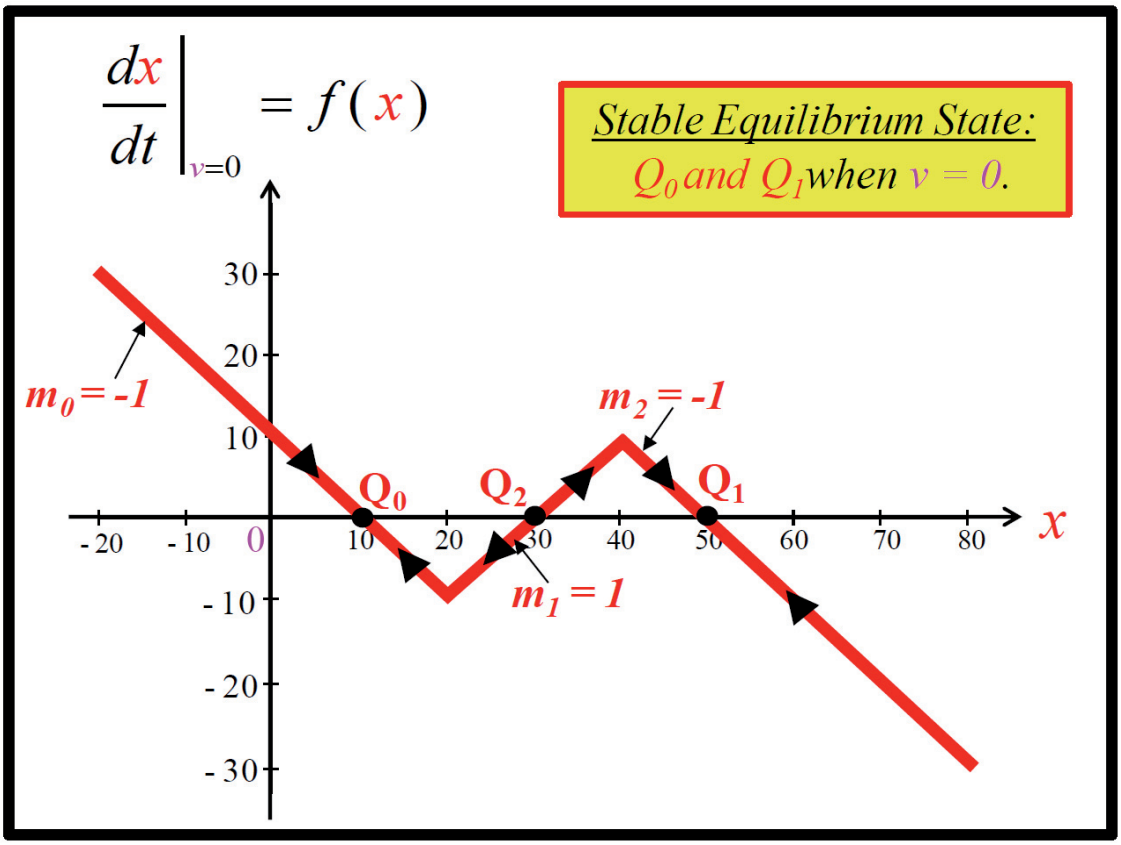


Fig. 21. Dynamic route associated with the POP of the voltage-controlled memristor defined by (16).

In the special case where $G(x, 0)$ assumes only 2 distinct values G_1 and G_2, say

$$\begin{aligned} G(x, 0) &= G_1, \qquad 0 < x < 10 \\ &= G_2, \qquad 10 < x < \infty \end{aligned} \tag{40}$$

this memristor can be used as a *non-volatile* binary memory, with G_1 representing the binary state "0", and G_2 representing the binary state "1" [5].

It is easy to switch from any non-volatile state $x(Q_1)$ to another non-volatile $x(Q_2)$ of the continuum-memory memristor (38), or vice-versa, by applying a *square* voltage pulse of appropriate height ΔE, and duration ΔT.

For example, suppose one wishes to switch from the non-volatile state Q_2 to the non-volatile state Q_1 shown in Fig. 23(a). For simplicity, let us pick a *negative* square pulse of height $\Delta E = 1$ Volt at $t = t_0$ and calculate the time $t = t_1$ on the green dynamic route in Fig. 23(a) whose projection onto the x-axis is Q_1. In this case, $\Delta T = t_1 - t_0 = \Delta_1$.

Conversely, to switch from the non-volatile state Q_1 to the non-volatile state Q_2, we simply apply a *positive* square pulse as shown in Fig. 23(b), where (assuming $\Delta E = 1$) the pulse width can be calculated as $\Delta T = t_4 - t_3 = \Delta_2$.

Observe from (38c) that for each value $V > 0$, there are 2 odd-symmetric blue dynamic routes located in the 1st and the 3rd quadrants. Similarly, for each value $V < 0$, there are 2 odd-symmetric green dynamic routes located in the 2nd and the 4th quadrants. Observe also that since *no dynamic routes* corresponding to (38c) can cross the x-axis, the POP of this Continuum Memory Memristor restricts all dynamic routes to either the upper half plane $(dx/dt) > 0$, or lower half plane $(dx/dt) < 0$.

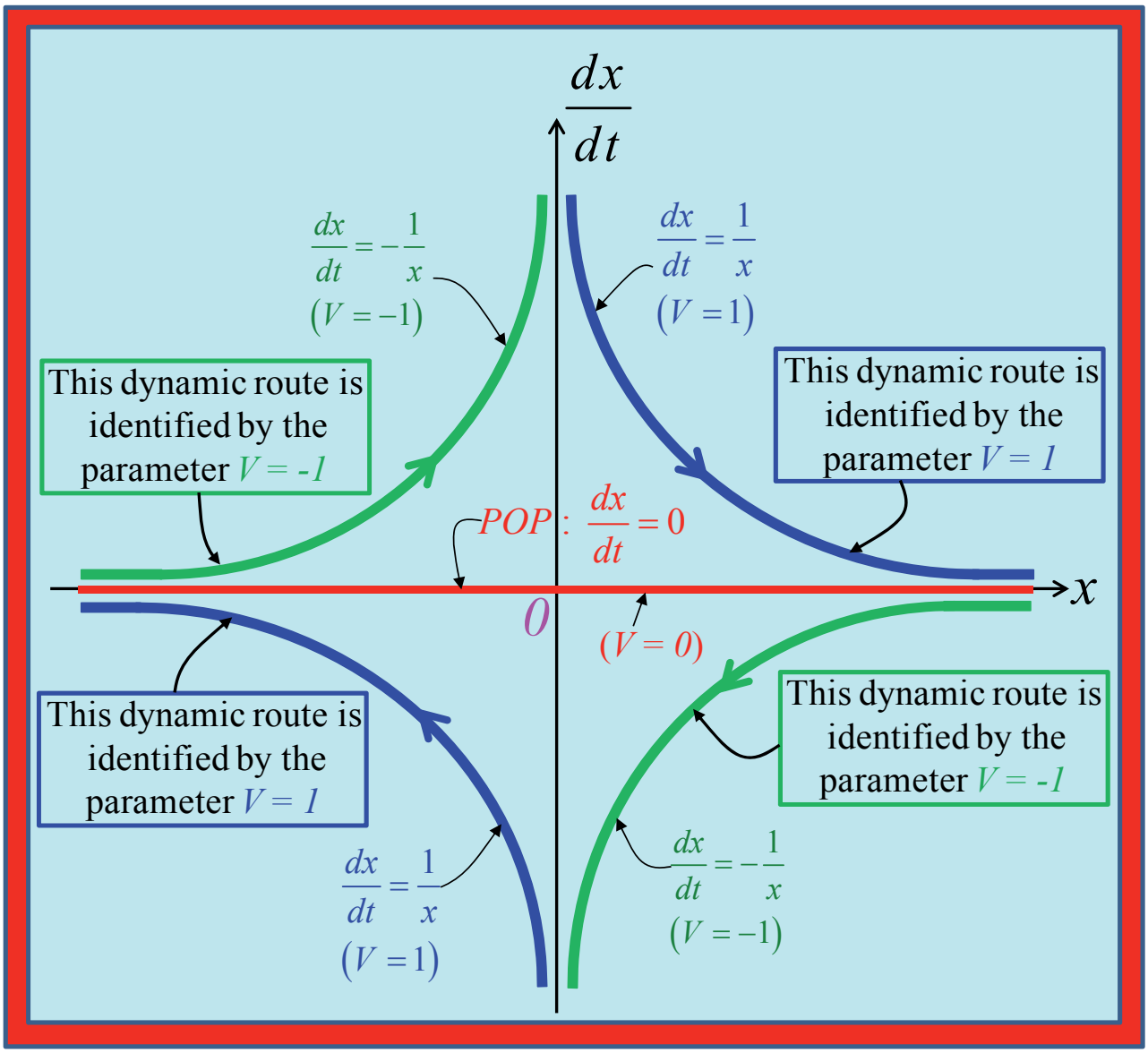


Fig. 22. The POP of the memristor defined in (38) coincides with the x-axis, where every point is a stable (but not asymptotically stable) equilibrium point. Four dynamic routes corresponding to $V = 1$(blue) and $V = -1$(green) indicate the direction of motion from an *initial state* $x(0)$ lying on any of the 4 paths.

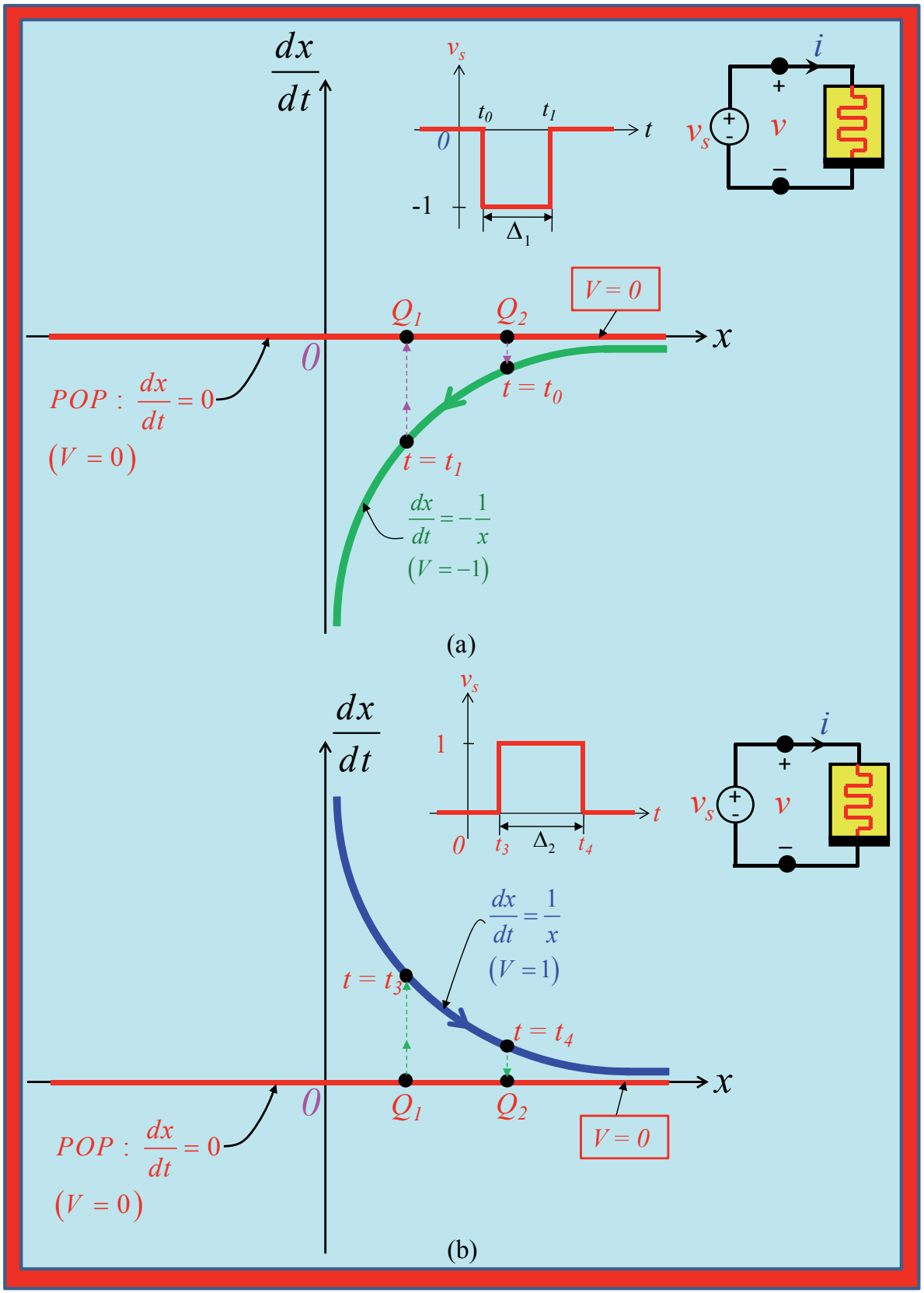


Fig. 23. A square voltage pulse of appropriate polarity, height ΔE, and duration ΔT can be used to switch from any non-volatile state to any other non-volatile state: (a) switching from Q_2 to Q_1, via a *negative* voltage pulse of height ΔE = 1 and width Δ_1. (b) switching from Q_1 to Q_2, via a *positive* voltage pulse of height ΔE =1 and width Δ_2.

10. DC *V-I* Plots

All freshmen in electrical engineering are taught that most 2-terminal devices have a DC *V-I* curve obtained by connecting a battery with voltage $v = V$ across the device and measuring its corresponding DC current I. By repeating the experiment with many different voltages V, we obtain a set of points on the *V-I* plane. A smooth curve passing through these points is called the *DC V-I curve*[14] of the device. Notice that the adjective *DC* is important because the measured curve may change if one substitutes the DC power supply with a low-frequency sinusoidal, or triangular, voltage source. This latter measurement scheme is often adopted because it replaces the rather slow manual tuning of DC voltages by an automated set-up where the slow variation of the periodic waveform is assumed to produce the same effect as manual tuning.

Unfortunately, for memristors, the manual and automated tuning schemes can give *completely different* results, no matter how low is the frequency chosen for the periodic voltage signal. In this section, we will see that many memristor DC *V-I* curves measured by conventional automated instruments are *erroneous*, and that the correct DC *V-I* curve of many memristors is *not* a curve, but a *set of points* on the *V-I* plane, ranging from a large collection of points forming multiple branches, or to just *one point* – a *singleton* on the *V-I* plane!

Since it is misleading to call such bizarre set of points a curve, we will henceforth use the terminology *DC V-I Plot*, instead of the traditional DC *V-I* curve, unless the set of points actually lie on a curve.

Example. 10.1 DC V-I Plot of PTC Thermistor

Consider the PTC thermistor defined in (12). To measure the DC *V-I* Plot of this memristor, we must substitute a set of constant voltages $V = V_1, V_2, ..., V_m$ for v in (12a) and (12b), and measure the corresponding constant current $i = I = I_1, I_2, ..., I_m$ after all transient had decayed to zero.

The corresponding *set of points* $(V_1, I_1), (V_2, I_2), ..., (V_m, I_m)$ is the DC *V-I* Plot of the PTC thermistor. The *caveat* here is how long should the experimentalist wait before he can proceed to measure the next point? To answer this fundamental question, let us suppose the PTC memristor behaves exactly according to (12). At *zero* transient, the measured state variable $x = X_Q$ must be a *constant* because $\left.\frac{dx}{dt}\right|_{x=X_Q} = 0$. Such a value of x is called an *equilibrium state* in the *theory of nonlinear dynamics* [24], [27]. The equilibrium state of a memristor is obtained by equating the right-hand side of (12b) to zero and solving for all *constant* values of x, for *each* assigned constant value $v = V$, which satisfied the following *Memristor Equilibrium Equation* :

$$\frac{\delta_P}{H_{CP}}(T_{0P} - x) + \frac{1}{H_{CP}}\left[R_{OP}\ e^{\beta_P(x - T_{0P})}\right]^{-1} V^2 = 0\ . \quad (41)$$

In general, memristor equilibrium equations are strongly nonlinear *algebraic* equations and their solutions must be calculated *numerically*, or *graphically*. There are many numerical softwares for solving nonlinear algebraic equations. They are highly efficient and reliable if the equation has only one solution for each value of V. Unfortunately, such software can find only one solution even if the equation has multiple solutions[15].

Although the above memristor equilibrium equation (41) can be solved analytically, we will solve it via a *graphical method* which is completely general, albeit much less accurate than numerical methods. It has the unique advantage, however, that *all* DC current I, for each DC voltage V, are guaranteed to be found[16]. Even more important, our graphical method provides numerous *insights* about the dynamics of the memristor which no numerical software, or emulator, could provide.

Since our goal is to calculate all DC (V, I) that satisfy (12a), we must substitute x in (12a), which is generally a function of time, except at equilibrium points. Let us plot the memductance function $W(x)$ defined in (12c) as a function of $x = X_Q$ over the range of X_Q relevant to the PTC thermistor, as shown in Fig. 24[17].

The next step in our *graphical method* is to plot dx/dt (defined by the right hand side of (12b)) as a function of x, for each DC voltage V relevant to our PTC thermistor. Each curve in Fig. 25 corresponds to one DC value $V = V_K$, and has 2 arrowheads indicating the direction of motion starting from any initial point $x = x(0)$. The direction of arrowhead in each curve points to the right in the upper half plane $dx/dt > 0$, and to the left in the lower half plane $dx/dt < 0$. Observe that $dx/dt = 0$ at exactly one point where each curve in Fig. 25 intersects the horizontal line $dx/dt = 0$. These are the *equilibrium points* of the PTC thermistor! Each curve in Fig. 25 is in fact just the dynamic route we encountered in Fig. 23. It makes sense therefore henceforth to call Fig. 25 as the *family of dynamic routes* associated with the PTC thermistor. Observe that the

[14] We choose the capital letters V and I, instead of the conventional lower case letters v and i to distinguish them from the *H F v-i curve* (acronym for high-frequency *v-i* curve) exhibited by *all* Extended memristors when connected to high-frequency periodic signals.

[15] Commercial simulators, such as various versions of SPICE, are even less reliable because the numerical algorithm it uses is incapable of solving complicated nonlinear equations.

[16] More accurate solutions can be found by using the graphically derived solutions as *initial* guess for numerical softwares.

[17] The range $300 < X_Q < 3000.0008$ in Fig. 24 was chosen upon inspection of Fig. 25.

coordinate (X_Q, V_Q) for each intersection point can be trivially extracted from Fig. 25.

Remark 10.1

The *family of dynamic* routes associated with each memristor contains the coordinate X_Q of a subset of the equilibrium points of any *first - order memristor*.

The range of X_Q in Fig. 25 is approximately $300 < X_Q < 300.0008$. The set of points (X_Q , V_Q) extracted from Fig. 25 can be used to plot the skeleton of a curve relating X_Q as a function of V, as shown in Fig. 26, where we label as $X_Q = \hat{X}_Q(V)$. The larger the number of DC voltages V we pick in Fig. 25, the smoother is the $X_Q = \hat{X}_Q(V)$ curve.

To obtain the DC *V-I* curve of the PTC thermistor, let us substitute $X_Q = \hat{X}_Q(V)$ from Fig. 26 in place of X_Q in Fig. 24; namely,

$$W = W(X_Q)\big|_{X_Q=\hat{X}_Q(V)} = W(\hat{X}_Q(V)) \triangleq \overline{W}(V). \quad (42)$$

The memductance function $W = \overline{W}(V)$ can be trivially obtained using a laptop. It is however, more illuminating, albeit more time consuming and less accurate, by using the *graphical composition method* presented in [24].

Here, the functions $W = W(\hat{X}_Q)$ (from Fig. 24) and $X_Q = \hat{X}_Q(V)$ (from Fig. 26) are plotted in the upper left corner and lower right corner in Fig. 27, respectively. Adding the unit-slope line in the lower-left corner in Fig. 27 allows us to find the coordinate of X_Q for each DC voltage V by simply drawing vertical and horizontal projection lines, as illustrated in Fig. 27 for 2 values of V; namely, $V = 5$ and $V = 15$.

To find the value of X_Q at $V = 5$, we draw a vertical projection line through $V = 5$ in the upper right corner, until it intersects the lower curve $X_Q = \hat{X}_Q(V)$ at (1) point. We next draw a horizontal projection line through point (1) leftward until it intersects the unit-slope line in the lower-left corner at point (2) . Next we draw a vertical line through point (2) upward until it intersects the upper curve $W = W(\hat{X}_Q)$ at point (3). The final step is to draw a horizontal projection line through point (3) rightward until it intersects the initial vertical projection at point (4) . In other words, point (3) with coordinates $(X_Q, W(\hat{X}_Q))$ maps to point (4) with coordinates $(V, \overline{W}(V))$, which is a point in the $W = \overline{W}(V)$ function that we seek.

It remains to plot the DC *V-I* curve by simply multiplying each point on the $W = \overline{W}(V)$ curve by its corresponding value V, as stipulated by the State-Dependent Ohm's Law (12a); namely,

$$I = \overline{W}(V)\, V \triangleq \hat{I}(V) \,. \quad (43)$$

This is shown in Fig. 28, for $V > 0$, and $V < 0$. The red branch is obtained from our rough graphical method using a *coarse* scale, which did not include the green branch depicted in the inset of Fig. 28 for $0 < V < 0.5$ (which can be obtained by the same graphical method with a finer scale near $x = 0$). The *odd-symmetric* blue branch in Fig. 28 comes for free because a careful analysis of (12), (41) and (42) reveals that the DC *V-I* plot of the PTC memristor is an *odd-symmetric* function of V.

Since the DC *V-I Plot* of the PTC thermistor in Fig. 28 is a *single-valued* function of the DC voltage V, we can call this a DC *V-I curve*. In particular, under *Power-OFF* condition ($V = 0$), there is a *unique small-signal conductance* equal to the slope of the curve at $V = 0$, namely,

$$\left.\frac{\delta I}{\delta V}\right|_{V=0} = W(X_Q)\big|_{V=0} = \left[R_{OP} e^{\beta_P (300-300)}\right]^{-1} = \frac{1}{R_{OP}} = 10^{-3} \quad (44)$$

Observe that the above small-signal conductance can be measured by applying a small voltage pulse $\delta v(t)$ and measuring the current response $\delta i(t)$. It is important to understand that this memristor (PTC thermistor) is a *volatile* memory device because *the same* small-signal conductance will be measured no matter what previous signals has been applied across its terminals. This volatility property is due to the fact that the POP of the PTC thermistor has *only one intersection* with the (dx/dt)-axis in Fig. 25.

Example. 10.2 A Shoelace DC V-I Plot

Let us revisit the hypothetical PWL Memristor in (16) of Example 5.6. The POP of this memristor and its associated dynamic route in Fig. 21 shows that when the power is OFF (i. e., $V = 0$) this memristor has 3 equilibrium states $X_{Q_0} = 10$, $X_{Q_1} = 50$ and $X_{Q_2} = 30$ where Q_0 and Q_1 are *asymptotically stable*, while Q_2 is *unstable* in the sense that it is unobservable in practice due to the inevitable presence of circuit noise. This memristor therefore can be used as a *non-volatile binary memory*, where the binary State "0" is coded by the small-signal conductance $G_0 = 100$ S at Q_0, and the binary state "1" is coded by the small-signal conductance $G_1 = 2500$ S at Q_1 (see (37) and Fig. 32 of [5]). We can switch from Q_0 to Q_1 by applying a small positive voltage pulse across the memristor, or from Q_1 to Q_0 with a corresponding negative pulse, as illustrated in Fig. 33 of [5].

The existence of 2 distinct *small-signal conductances* G_0 and G_1 during Power-OFF (i. e., $V = I = 0$) implies that, unlike the PTC thermistor, the *DC V-I* Plot of this memristor must have *at least* 2 branches which cross each other at the origin (V, I) = (0, 0), as depicted in Fig. 32 of [5]. Such a *DC V-I* Plot can no longer be a single-valued curve. What does it look like?

It is shocking that current numerical softwares or emulators are incapable of calculating this *DC V-I* Plot!

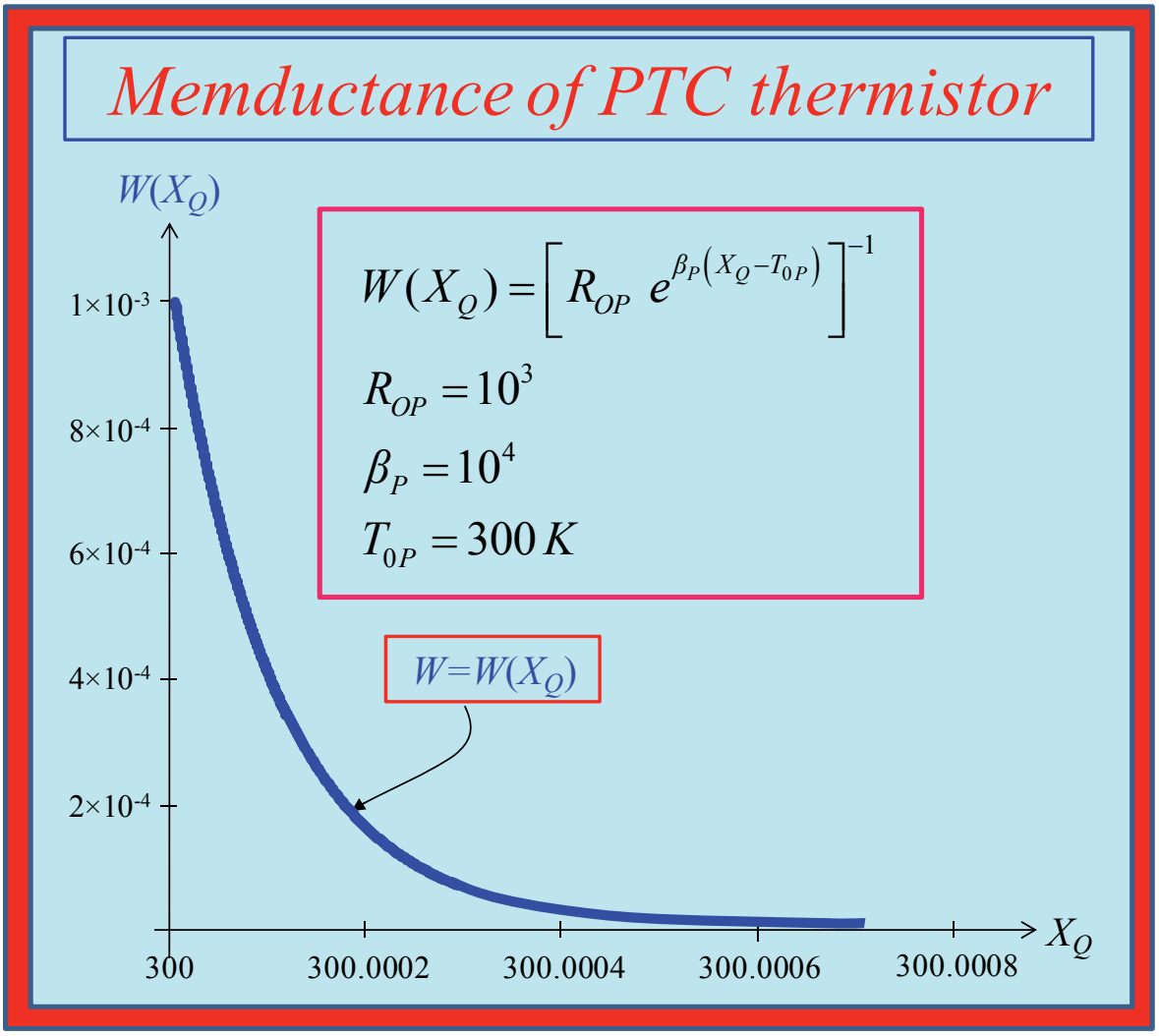


Fig. 24. Plot of X_Q – dependent memductance $W = W(X_Q)$ from the state-dependent Ohm's law of the PTC thermistor.

The following 3 methods however can be used.

DC V-I Plot Method 1: Graphical Composition Method

Repeat the procedure presented in Example 10.1 with the memristor defined by (16), instead of (12).

DC V-I Plot Method 2: Piecewise-Linear Method

Solve the state equation (16b) analytically as 3 separate *linear* differential equations where $f(x)$ is replaced by an affine function representing the extension of the 3 straight lines in Fig. 16. The relevant portion of each solution is then extracted and plotted. The union of these 3 relevant solutions is the *DC V-I* Plot of this PWL memristor.

DC V-I Plot Method 3: Parametric Method [30]

Step 1

Set $(dx/dt) = 0$ in (16b) and recast it (with v and x replaced by their DC symbols V and X) into the following *parametric form*, i.e., as a function $\hat{v}(X)$ of a scalar parameter X:

$$V = -30 + X - |X - 20| + |X - 40| \triangleq \hat{v}(X) \quad (45a)$$

Step 2

Substitute (45a) for v in (16a) (with v, i, and x replaced by their DC symbols V, I, and X) with $G_0 = 1$ and recast it into the following *parametric form*, i. e., as a function $\hat{i}(X)$ of the same scalar parameter X:

$$I = -30X^2 + X^3 - |X - 20|\, X^2 + |X - 40|\, X^2 \triangleq \hat{i}(X) \quad (45b)$$

Step 3

Partition the relevant interval $-20 < X < 80$ of the POP in Fig. 16 into a set

$$\mathcal{X} = \{ X_K : -20 < X_K < 80 \} \quad (46)$$

of uniformly-spaced points, such as

$$\mathcal{X} = \{ -20, -15, -10, -5, 0, 5, 10, 15, 20 \} \quad (47)$$

Step 4

For each $X_K \in \mathcal{X}$, calculate

$$\left.\begin{aligned} V_K &= \hat{v}(X_K) \quad \text{from (45a)} \\ &\text{and} \\ I_K &= \hat{i}(X_K) \quad \text{from (45b)} \end{aligned}\right\} \tag{48}$$

Step 5

For each $X_K \in \mathcal{X}$, plot a point $\left(V_K = \hat{v}(X_K),\ I_K = \hat{i}(X_K)\right)$ in the *I vs. V* plane and draw a smooth arc connecting these points. The resulting loci is the DC V-I Plot of the memristor. The two parametric equations $V_K = \hat{v}(X_K)$ and $I_K = \hat{i}(X_K)$ calculated from (45a) and (45b) are shown in Fig. 29(a) and 29(b), respectively. The loci represented by $\left(\hat{v}(X),\ \hat{i}(X)\right)$ in Fig. 29(c) is the *DC V-I Plot* of the *PWL Memristor* defined in (16) of Example 5.6.

It is important to observe that unlike the numerical approach, both $\hat{v}(X)$ and $\hat{i}(X)$ are *analytical* formulas describing the *DC V-I Plot exactly* [30]. Observe also that

$$\hat{i}(X) = G(X)\,\hat{v}(X)\,. \tag{49}$$

Remark 10.2

The *Parametric Method*, when applicable, gives the *exact analytical equation* for the *DC V-I Plot*. The Parametric Method is applicable whenever the voltage *v* (resp., current *i*) can be recast as a function of *x* in the expression obtained by setting the right-hand side of the *state equation* of a voltage-controlled (resp. current-controlled) memristor to zero.

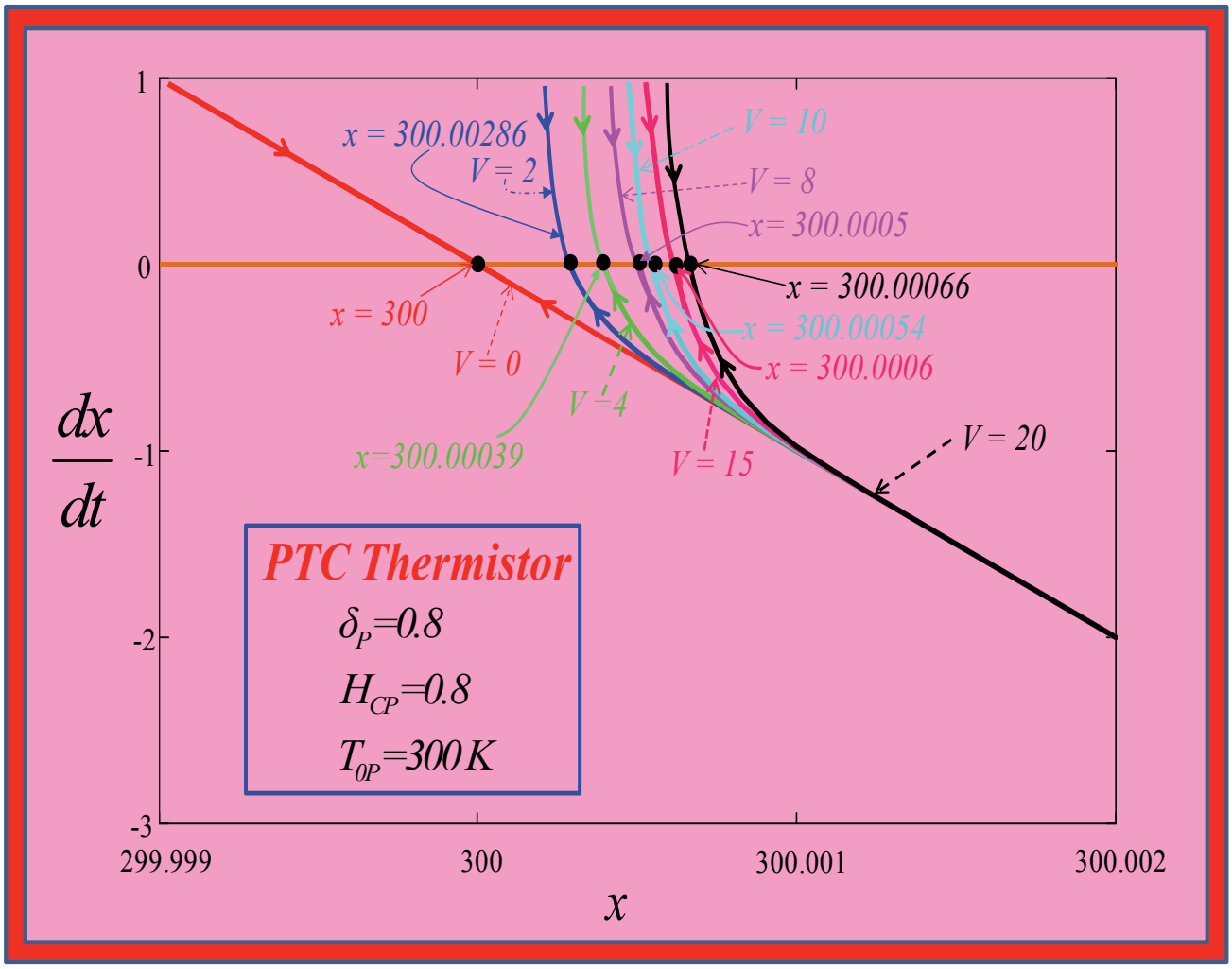


Fig. 25. Graphical Method for Calculating the equilibrium state $x = X_Q$ for each DC voltage V over the range of interest. Each dynamic route is identified with a fixed constant value $v = V$ for $0\ \text{V} \le V \le 20\ \text{V}$ in this plot. Each intersection of a dynamic route at $v = V_K$ with the $(dx/dt) = 0$ axis gives the value $X_Q\,(V_K)$ at $V = V_K$. The coordinates $(V_K,\ X_Q\,(V_K))$ give a point on the voltage-dependent *Equilibrium plot*.

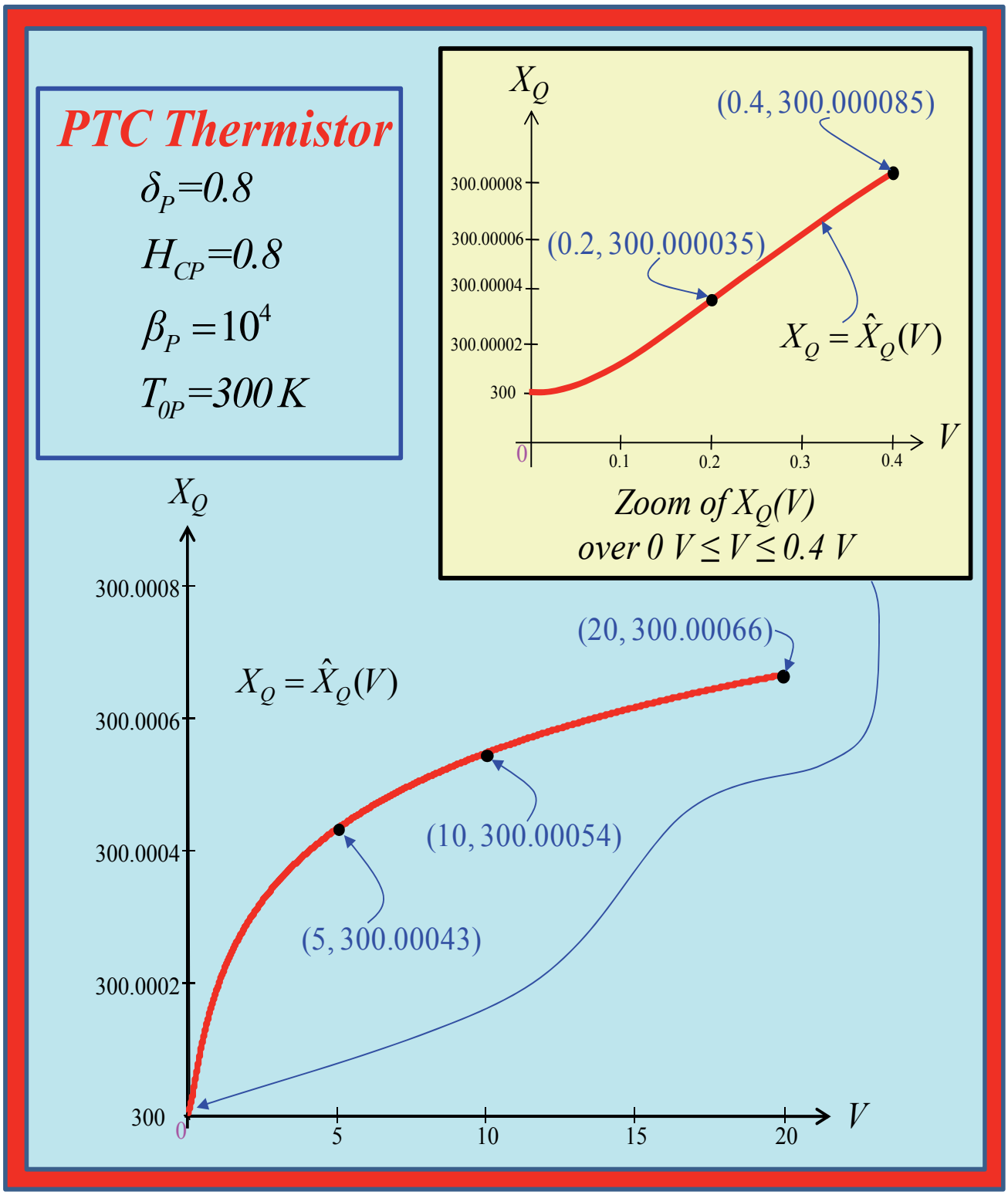


Fig. 26. Voltage-Dependent *Equilibrium Plot* of the PTC thermistor constructed graphically by drawing a smooth curve through the points $(V_K, X_Q(V_K))$ extracted from Fig. 25.

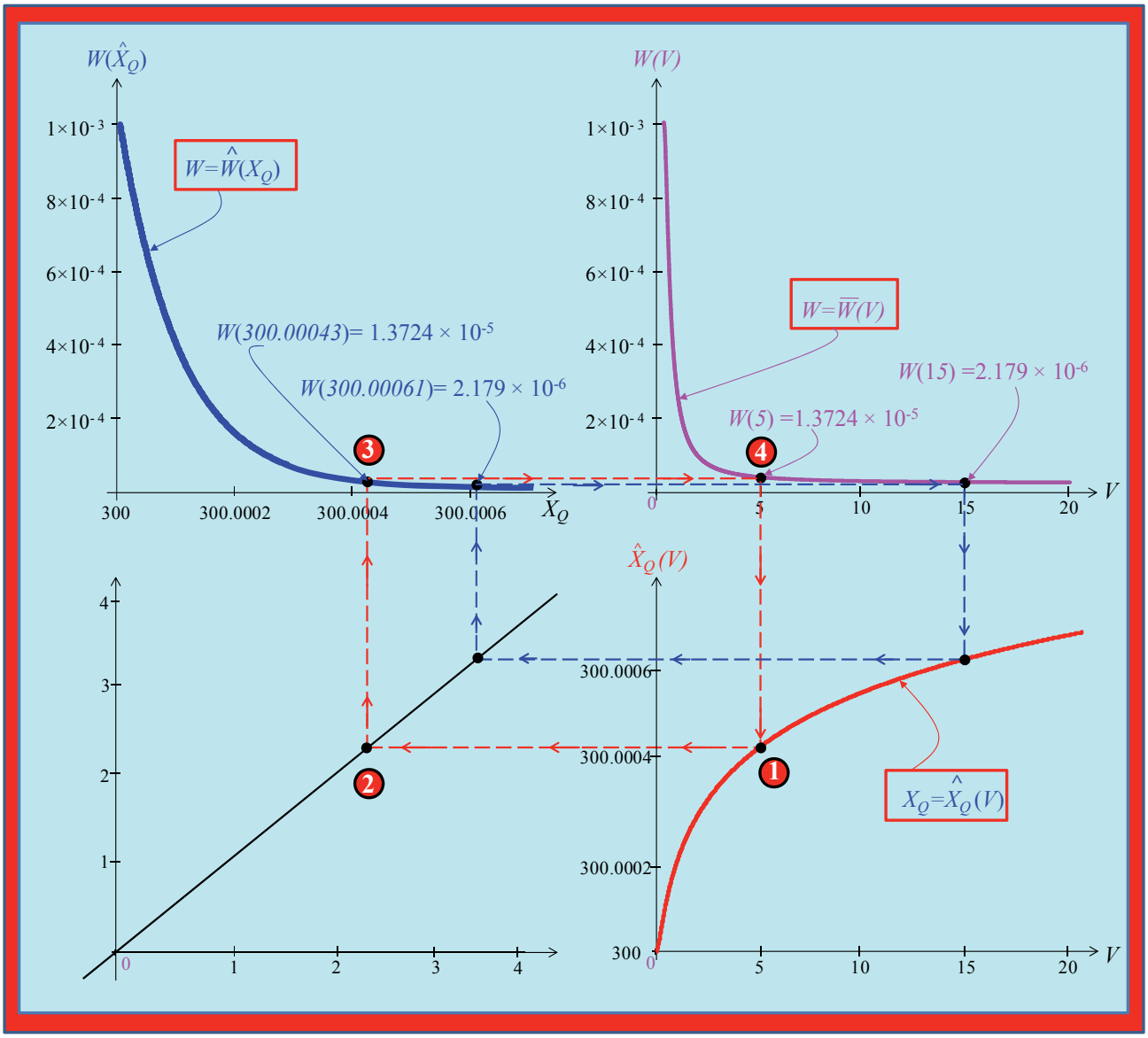


Fig. 27. Graphical method for constructing the memductance $W(X_Q)$ as a function of the DC voltage $v = V$ applied across the PTC thermistor.

10.1 Passive but Locally-Active Memristors

Since X is only a parameter needed to draw the DC V-I Plot, it can be deleted after the plot is drawn to avoid clutter, as shown in Fig. 30, which is an enlarged version of Fig. 29(c), where the coordinates at several intersecting points are printed for future reference. Observe that this memristor (defined in (16b)) is *passive* at *DC* because all points on the plot lie in the 1st and 3rd quadrants (yellow region) where $VI \geq 0$. It is interesting to note that it is *locally active* over the interval $-10\text{ V} < V < -3.334\text{ V}$ where the *small-signal conductance* at DC (defined by the slope $\delta I/\delta V$) is *negative*[18].

10.2 DC V-I Plots May Contain Unobservable Points

The DC V-I Plot of the PWL Memristor in Example 5.6 is *not* a curve, but a set of points representing the V-I coordinates corresponding to all 3 equilibrium points Q_0, Q_1, and Q_2 of the PWL memristor defined in (16), powered by a V-volt battery, for $-15\text{ V} < \text{V} < 15\text{ V}$. The red, blue, and green portions of the plot are associated with the equilibrium points Q_0, Q_1, and Q_2 shown in Fig. 21, respectively.

Since the equilibrium point Q_2, for any voltage

[18] In a future paper, we will design an oscillator by connecting a 7- volt battery (with the positive terminal connected to ground) in series with a positive inductor and the memristor defined by (16). This battery will give rise to an *unstable equilibrium point* located at (–7, –63), thereby spawning a *stable limit cycle* via a super-critical Hopf Bifurcation mechanism [27].

$-10\text{ V} < V < 10\text{ V}$, in Fig. 21 is unstable in the sense that the solution $x(t)$ with any initial state $x(0)$ located arbitrarily near Q_2 will diverge from Q_2 and tend to either Q_0 (if $x(0) < 30$) or Q_1 (if $x(0) > 30$), the green branch of the DC V-I Plot in Fig. 30 can *not* be measured *directly*[19]. Nor can it be calculated by any standard numerical software, or emulator.

Remark 10.3

Not all points on the DC V-I Plot of a locally-active memristor can be observed directly using conventional measurement schemes.

10.3 Two Stable Branches through Origin Imply Non-Volatile Binary Memory

Since the DC V-I Plot in Fig. 30 has 2 *stable* branches (red branch corresponding to stable equilibrium point Q_0 and blue branch corresponding to stable equilibrium point Q_1), for any DC voltage $-10\text{ V} < V < 10\text{ V}$, there are 2 branch points on the plot for each $V = V^*$ which can be used to code a binary "0" and a binary "1" state, by applying a DC voltage $V = V^*$ across the memristor and measuring its corresponding current response. It is natural to pick $V^* = 0$ because it means that by connecting a small voltage signal across the memristor, there are 2 distinct current responses that can be measured, one of which can code for state "0", and the other for state "1". Since no DC battery is needed in this case, the memory state is retained until it is switched via an approximate switching signal, as illustrated in Fig. 33 of [5].

Since only the 2 stable branches near the origin are of interest in *non-volatile memory* applications, we extract only the red and blue branch as shown in Fig. 31(a). Since only a very small signal is needed to identify which branch is retained only the tiny interval shown in Fig. 31(b) is relevant, where slope is equal to the corresponding small-signal conductance.

10.4 Quasi DC V-I Plot

Let us apply a sinusoidal, or triangle voltage signal with *amplitude* A and *frequency* ω across the memristor with the DC V-I Plot shown in Fig. 30. Let us assume $A > 10\text{ V}$ and ω is extremely small so that the voltage source might emulate a *manually tuned* DC voltage power supply. In this case, the measured V-I Plot would be a *pinched hysteresis loop* with 2 *instantaneous* jumps located at $V = -10\text{ V}$, and $V = 10\text{ V}$, respectively. The jumps must take place at these 2 voltages because the memristor has only one equilibrium point for $V < -10\text{ V}$, and $V > 10\text{ V}$, respectively. Because the loci shown in Fig. 32 is not measured with a tunable *DC Voltage Source*, we will henceforth call the measured pinched hysteresis loop a *Quasi DC V-I Plot*.

10.5 A Shoelace DC V-I Plot

We end Sec. 10 with the pin-up portrait of our *DC V-I Plot*, shown in Fig. 33, which resembles the shoelace exhibited in the inset, henceforth christened the *memristor shoelace DC V-I Plot*, or simply the *memristor shoelace plot* for short.

11. Continuum-Memory Memristors

Our final section is devoted to the class of *continuum-memory memristor* whose *POP* (Power-Off Plot) coincides with the x-axis, such as (39) of Example 9.3. Recall the POP of any memristor is derived using *only* the memristor's state equation. Consequently, for each memristor state equations whose POP is the x-axis[20], we can choose *any* state-dependent Ohm's law

$$i = G(x, v)\, v \tag{50a}$$

where the memductance satisfies

$$0 \le G(x, v) < \infty \tag{50b}$$

thereby spawning a *bespoke* continuum-memory memristor.

For sake of clarity let us pick the following simple generic passive memristor[21]:

Generic Continuum-Memory Memristor

State-Dependent Ohm's Law:

$$i = x^2 v \tag{51a}$$

State Equation:

$$\frac{dx}{dt} = \frac{v}{x} \tag{51b}$$

The POP of this memristor is depicted as the red x-axis in Fig. 22. Our goal is to derive the DC V-I Plot of this memristor over the entire DC voltage axis.

So far, we have seen that the DC V-I Plot of a memristor can be a single-valued curve (such as DC V-I curve of the PTC thermistor shown in Fig. 28), or *several* single-valued curves (such as the 3 curves shown in Fig. 39 of [5], each spanning the entire current axis $-\infty < I < \infty$), or a contiguous set of points forming a string intersecting itself with multiple loops (such as the shoelace V-I Plot depicted in Fig. 33). What does the DC V-I Plot of the continuum-memory memristor defined in (51) look like?

[19] It is possible, however, to design an elaborate experimental set-up to observe the unstable green branch in Fig. 30.

[20] Any state equation $dx/dt = g(x, v)$ where $g(x, 0) = 0$, $-\infty < x < \infty$ has a continuum-memory consisting of all points of the x-axis.

[21] Equation (51a) defines a *passive* memristor because its instantaneous power $p(t) = i(t)v(t) = x^2(t)v^2(t) \ge 0$ for any $v(t)$ and for all times t.

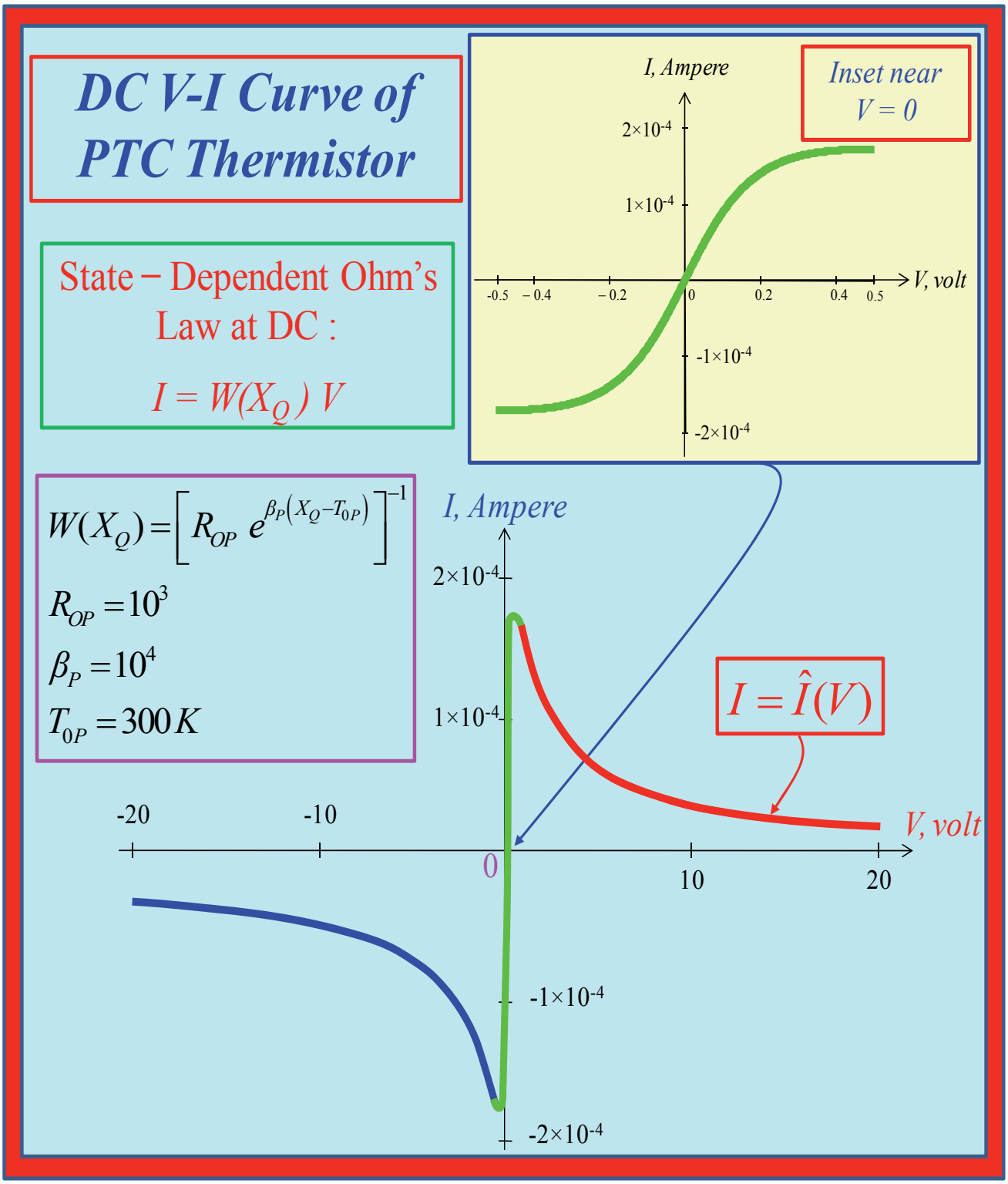


Fig. 28. DC *V-I* plot of the PTC thermistor –20 V < *V* < 20 V. The inset shows the details near origin for –0.5 V < *V* < 0.5 V.

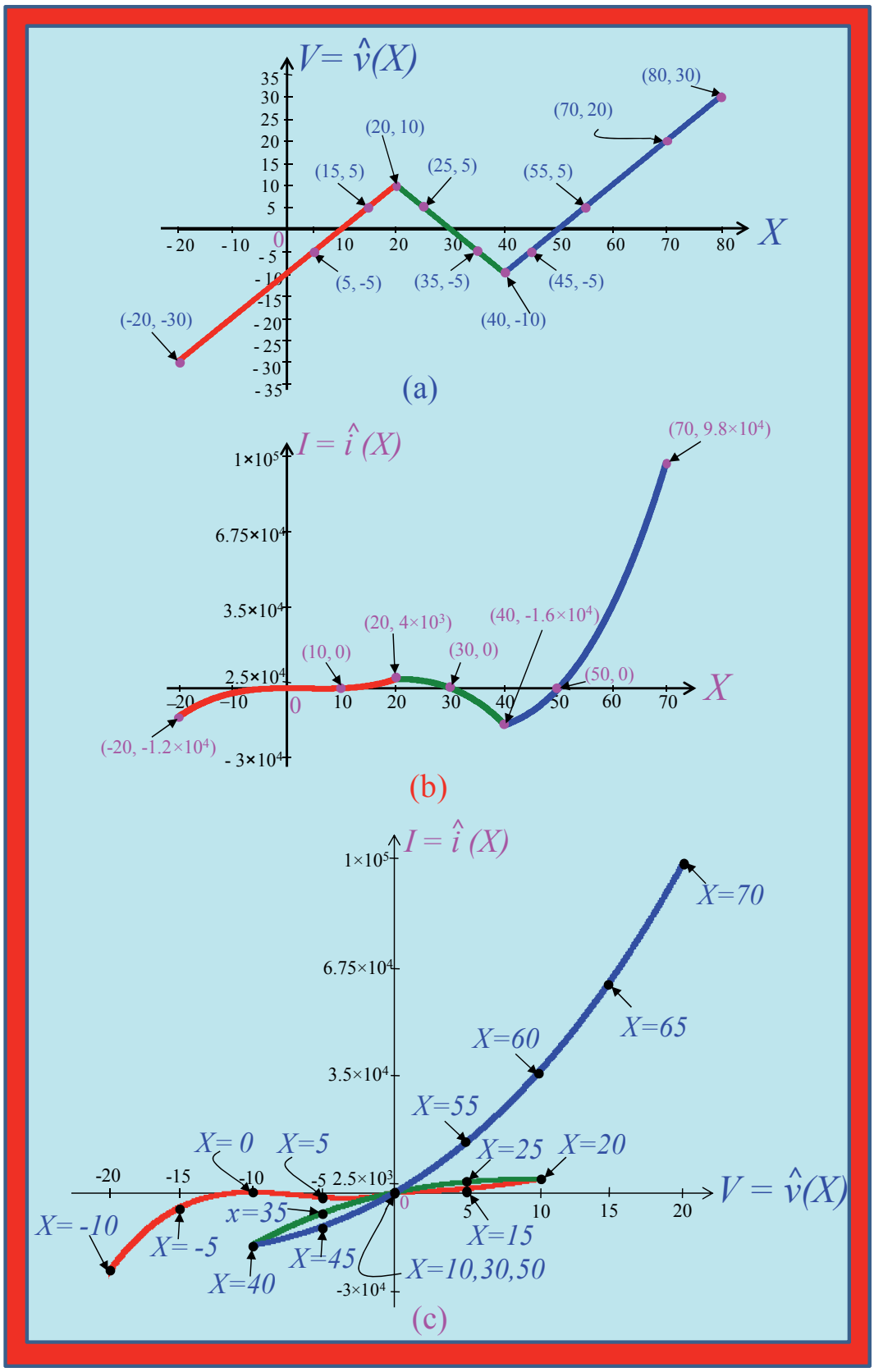


Fig. 29. Plots of the parametric equations (a). $V = \hat{v}(X)$, (b). $I = \hat{i}(X)$, and their loci (c). The red, green, and blue portions of these plots correspond to the left, middle, and right segment of the POP in Fig. 16.

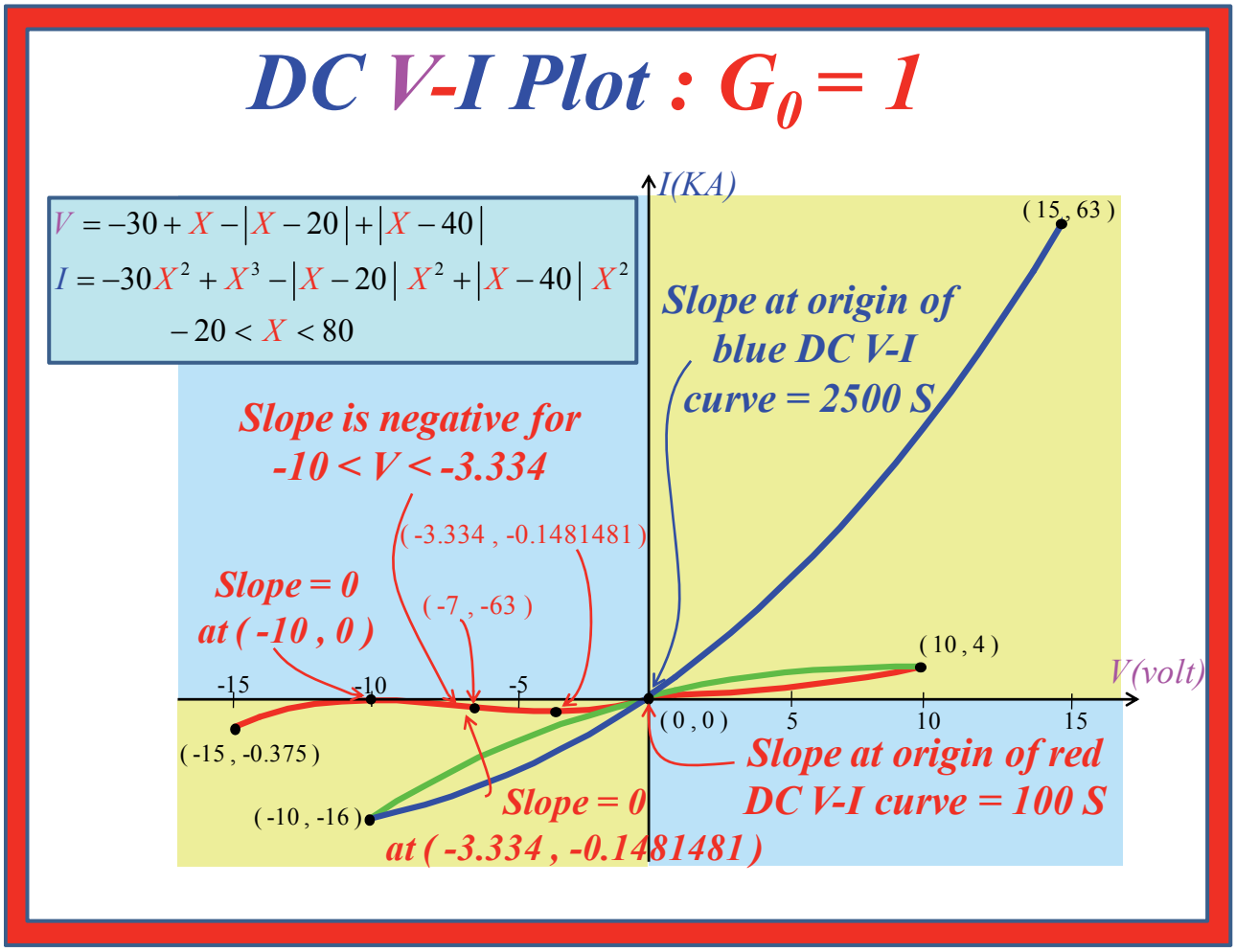


Fig. 30. DC V-I Plot of the memristor defined by (16) in Example 5.6.

To derive the DC V-I Plot of *any* memristor the first step is to set its state equation to zero and solve for the equilibrium state $x = X_Q$ for each DC voltage V, over the entire v-axis, i. e., $-\infty < V < \infty$. Carrying out this procedure in (51b), we obtain

$$\frac{dx}{dt} = \frac{V}{X} = 0 \tag{52}$$

Equation (52) implies that this memristor does *not* have any equilibrium state for any non-zero DC voltage $V \neq 0$! This conclusion can also be derived from Fig. 22 where none of the constant-voltage curve (shown only for $V = 1$ and $V = -1$) $dx/dt = V/X$ intersects the x axis except when $V = 0$.

Observe that for any initial state located in the 1st quadrant $x(t) \to \infty$ as $t \to \infty$ and $x(t) \to -\infty$ for any initial state located in 3rd quadrant. Similarly, $x(t) \to 0$ as $t \to \infty$ for any point $(dx/dt, x)$ located in 2nd, or the 4th quadrant. In other words, the motion from *any* initial state located outside of the x-axis *never comes* to rest except at $t = \infty$.

Observe also from Fig. 22 that if one connects a battery of voltage $V = E > 0$ across this memristor, and if $x(0) > 0$ (1st quadrant), then the memristor would quickly burn out because $i(t) \to \infty$ in view of (51a). If $x(0) > 0$ and $V < 0$ (4th quadrant), $i(t) \to 0$, only at $t = \infty$, at least in principle.

It follows that the DC V-I Plot of the Continuum-Memory Memristor defined in (51) consists of *only one point* namely, the origin.

Though bizarre, a 2-terminal circuit element whose v-i relationship defined by $v = 0$, $i = 0$ has been proposed in the literature [31] – it is called a *Nullator*[22].

11.1 Pinched Hysteresis Loop at Extreme Low Frequencies

What happens if we connect a voltage source with a very low frequency sinusoidal, or triangular signal $v(t)$?

Fig. 34 shows the Lissajous figure of $(v(t), i(t))$ plot-

[22] It is possible to build a *nullator* using an op-amp. Indeed, if one connects a resistor from the negative input terminal of an op-amp to its output terminal, then 2 op-amp input terminals becomes a *virtual short circuit*, where $v = 0$ and $i = 0$!

ted in the *i vs. v* plane calculated from (51) with $v(t) = A \sin \omega t$ with amplitude $A = 1$ and $x(0) = 1$, for 4 frequencies $\omega = 1$, 0.1, 0.01, and 0.001. They are *pinched hysteresis loops*, as expected for all memristors. It can be proved that for the periodic signal $v(t) = A \sin \omega t$, there is no transient component in the current response $i(t)$. For $\omega << 1$, one might be tempted to call the pinched hysteresis loop a DC V-I Plot. However, since the correct DC V-I Plot for this memristor is a *singleton*, namely, the point $(V, I) = (0, 0)$, it is necessary to use another name for low-frequency pinched hysteresis loops, such as *Quasi V-I Plots*.

Observe that the area of each lobe of the Quasi-DC V-I Plots increases at an exponential rate as ω decreases. A plot of the maximum point $I^*(1)$, $I^*(0.1)$, $I^*(0.01)$ and $I^*(0.001)$ identified in Fig. 34 shows $I^*(\omega)$ increases exponentially as ω tends to zero, as shown in Fig. 35. It follows that this memristor will burn out when the frequency ω is too small.

11.2 Quasi DC V-I Plot Is Not DC V-I Plot!

The phenomenon described in the preceding section is based entirely on numerical simulations of the memristor equation (51) with $v = A \sin \omega t$. In general, the numerical approach is the only option for analyzing a *continuum-memory memristor* because a mathematical theory of *non-autonomous* differential equations[23] does *not* exist. But such numerically derived observations are questionable because they do *not* explain how rapidly the expanding pinched hysteresis loop collapses to a singleton at $\omega = 0$.

To overcome the above objections, we have designed the *bespoke* continuum-memory memristor equation (51b) which has an exact analytical solution. Indeed, let us recast (51b) as follow

$$x\, dx = v\, dt \,. \tag{53}$$

Integrating both sides of (53) from $t = 0$ with initial state $x(0)$, we obtain the following *exact* solution:

$$\begin{aligned} x(t) &= \sqrt{\overline{X} - \overline{A}\cos \omega t}\,, \quad \text{if } x(0) \geq 0 \\ &= -\sqrt{\overline{X} - \overline{A}\cos \omega t}\,, \quad \text{if } x(0) \geq 0 \\ \text{where} \quad \overline{A} &\triangleq \frac{2A}{\omega}, \quad \overline{X} \triangleq x^2(0) + \overline{A}. \end{aligned} \tag{54}$$

Observe that the analytical solution $x(t)$ in (54) is well-defined for all times $t \geq 0$ if, *and only if*, $\omega \neq 0$. In other words, the continuum-memory memristor equation (51) does *not* have a mathematical solution when $v(t) = A \sin \omega t$ when $\omega \rightarrow 0$!

Fig. 36 shows the loci of (dx/dt) *vs.* $x(t)$, for $x(0) = 1$, $A = 1$, and $\omega = 1$, 0.1, 0.01, and 0.001, respectively. Observe that as $\omega \rightarrow 0$, the *egg-shape* loops are compressed (albeit never touching each other) towards the x-axis, but with its leftmost point pinned at $x = x(0)$. Observe that for $x(0) \geq 0$, the loci are confined to the right half plane $x \geq 0$. Those for $x(0) \leq 0$ are confined to the left half plane $x \leq 0$. *No loci* can cross the vertical wall located at $x = 0$.

Observe that while the egg-shaped loci in Fig. 36 formed contiguous loops for all $\omega \neq 0$, and hence are in a periodic *steady state* regime, the corresponding loci with a DC input voltage $V = 1$ (resp., $V = -1$), will tend to $+\infty$ (resp., 0) as $t \rightarrow \infty$, but *never arriving* at a steady state, as depicted in Fig. 36! It follows that even at *extreme – low frequencies*, the *Quasi* DC V-I Plots of the Continuum-memory memristor defined in (51) are *not* the same as the unique DC V-I Plot of the memristor, which consists of only one point $V = I = 0$.

12. Concluding Remarks

All of the questions posed in Sec. 1 have now been answered. We end this paper with Tab. 5, which provides four simple tests to identify whether a set of Lissajous figures in the voltage-current plane obtained by applying a *periodic* voltage source, or current source (with zero mean) over a range of frequencies, across a 2-terminal device is a memristor, and if so, which class it belongs to.

There are 3 classes of memristors; namely, *ideal memristors*, *generic memristors*, and *extended memristors*. They are distinguished by the form of their defining equations. A sub class of generic memristors exhibits *identical* properties as ideal memristors and is therefore called *ideal generic memristors*. Since ideal generic memristors can be transformed to an ideal memristor via a *one-to-one* mathematical transformation, it is called a sibling of the ideal memristor parent.

We have clarified what a *non-volatile* memristor means and showed that not all memristors are non-volatile. In particular a memristor is non-volatile if, and only if, it exhibits at least 2 distinct *small-signal resistances* measured by applying a small *sensing* signal, without a DC component, across the memristor, and such that any one of its distinct small-signal resistances can be set upon applying some appropriate control signals. Moreover, once set, the small-signal resistance will be retained indefinitely (in principle) even after its value has been measured via some small sensing signals.

This paper contains many fundamental new results. They include the concepts of *Continuum-memory memristor*, *POP* (acronym for Power-Off Plot), *DC V-I Plot*, and *Quasi DC V-I Plot*, whose characteristics are unique in the kingdom of memristors. Among many colorful pictures the *shoelace DC V-I Plot* stands out as both stunning and illustrative. Even more impressive is that this bizarre *shoelace* plot has an e*xact analytical* representation via 2 *explicit* functions of the state variable, derived by a novel *parametric approach* invented by the author.

[23] An ordinary differential equation $d\mathbf{x}/dt = f(\mathbf{x}, t)$ is said to be *non-autonomous* when the time variable t appear explicitly in the equation, such as the case when the memristor is driven by non-constant voltage source.

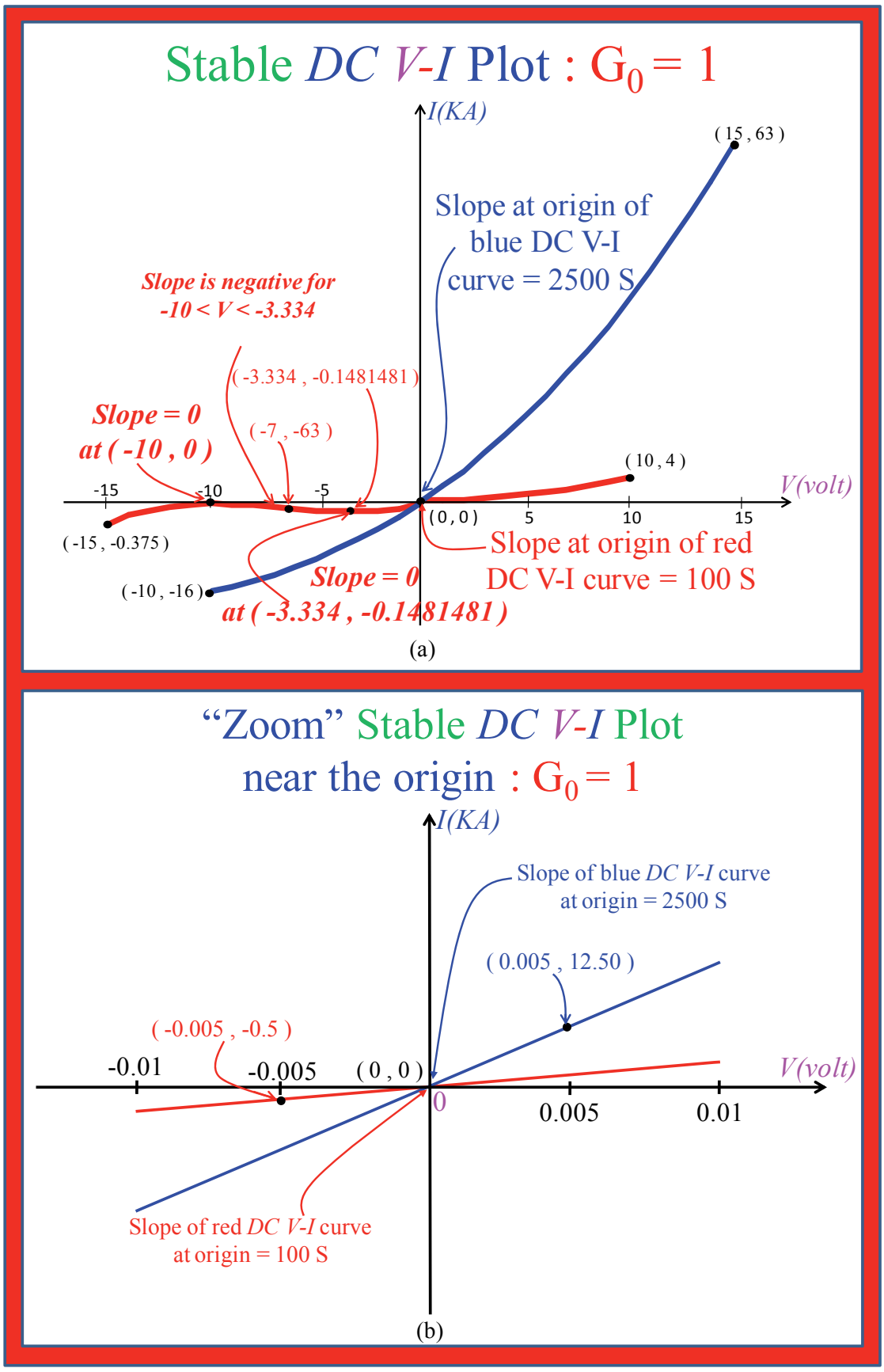


Fig. 31. Enlargement of the two stable branches of DC V-I Plot near the origin. (a). –15 V < *V* < 15 V, (b). –0.01 V < *V* < 0.01 V.

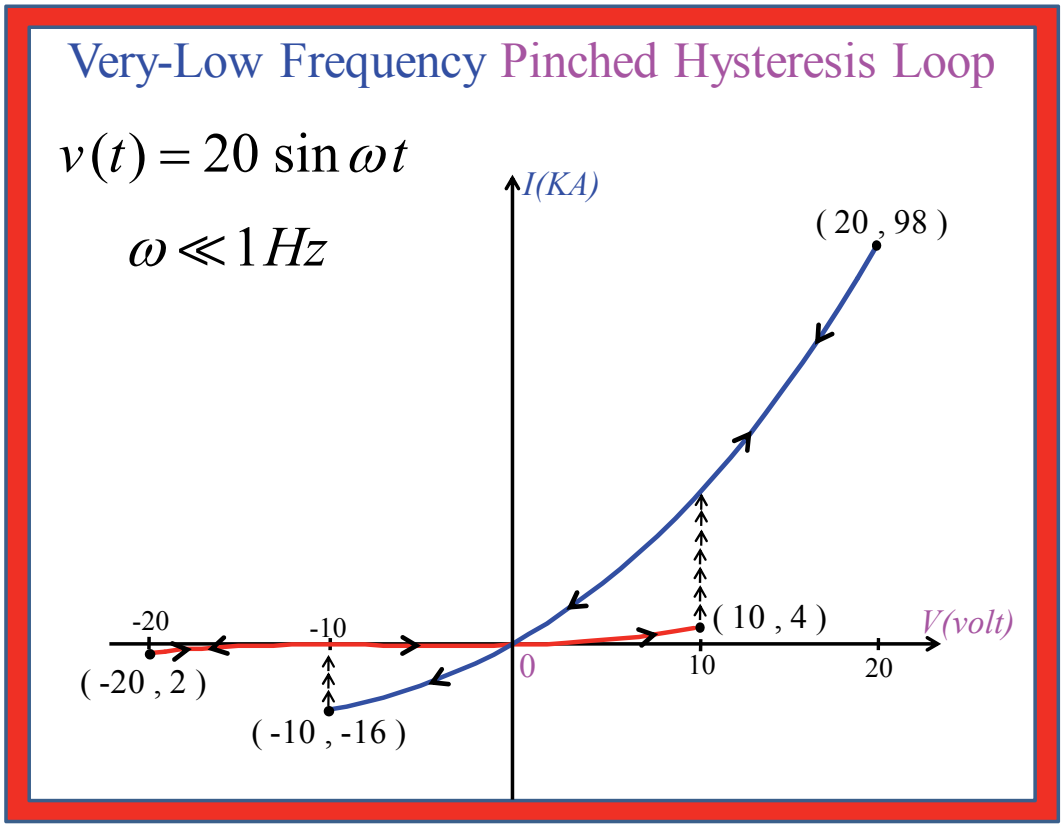


Fig. 32. Quasi DC V-I Plot associated with the DC V-I Plot in Fig. 30.

Fig. 33. The memristor shoelace plot.

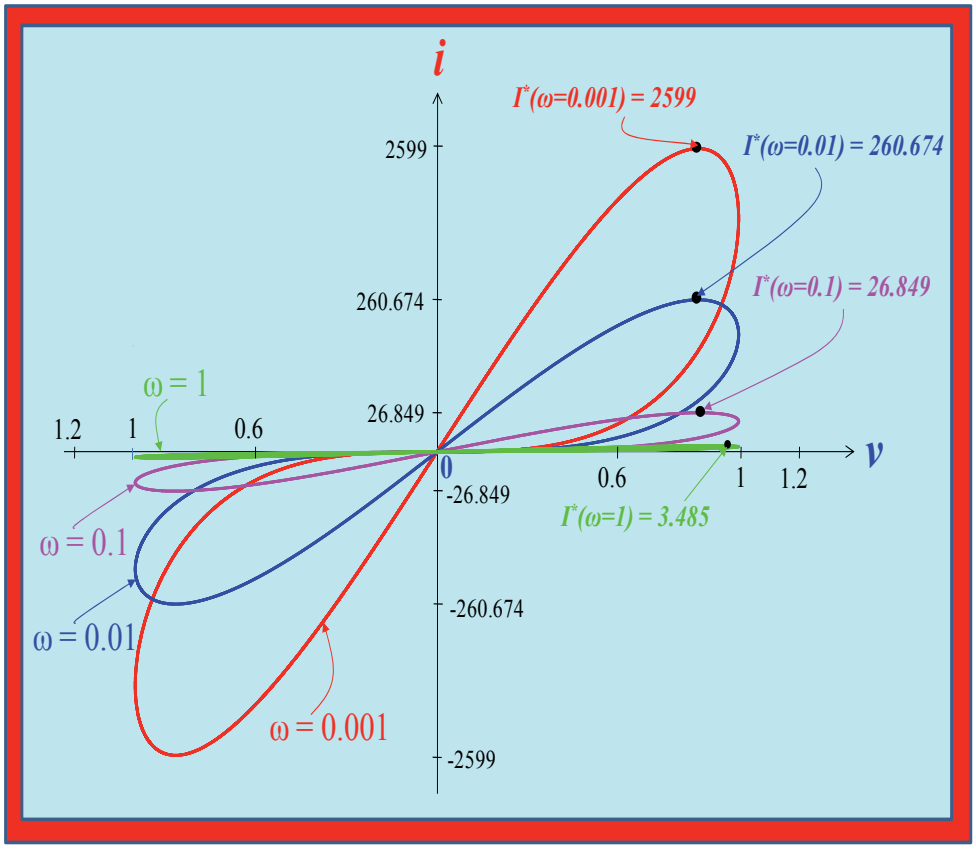


Fig. 34. Pinched hysteresis loops from the Continuum-memory memristor defined in (51), with $v = A \sin \omega t$, $A = 1$, $x(0) = 1$, for $\omega = 1$, 0.1, 0.01, and 0.001, respectively.

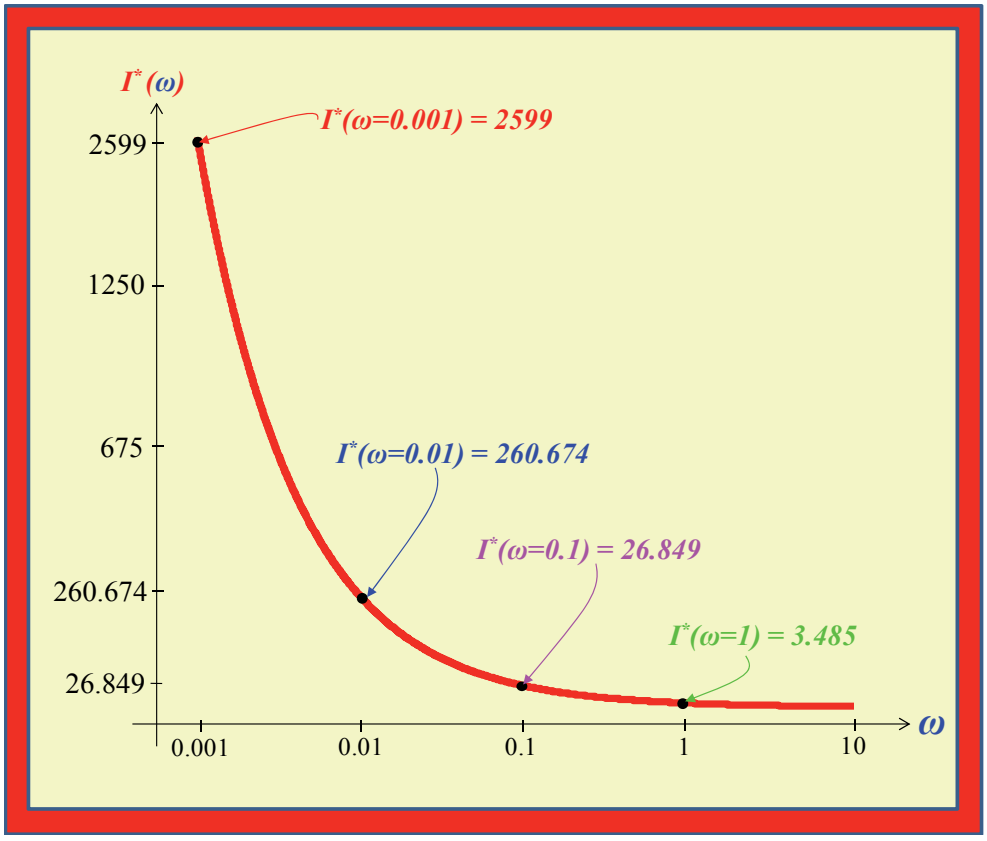


Fig. 35. Graph of the peak current I^* as a function of ω.

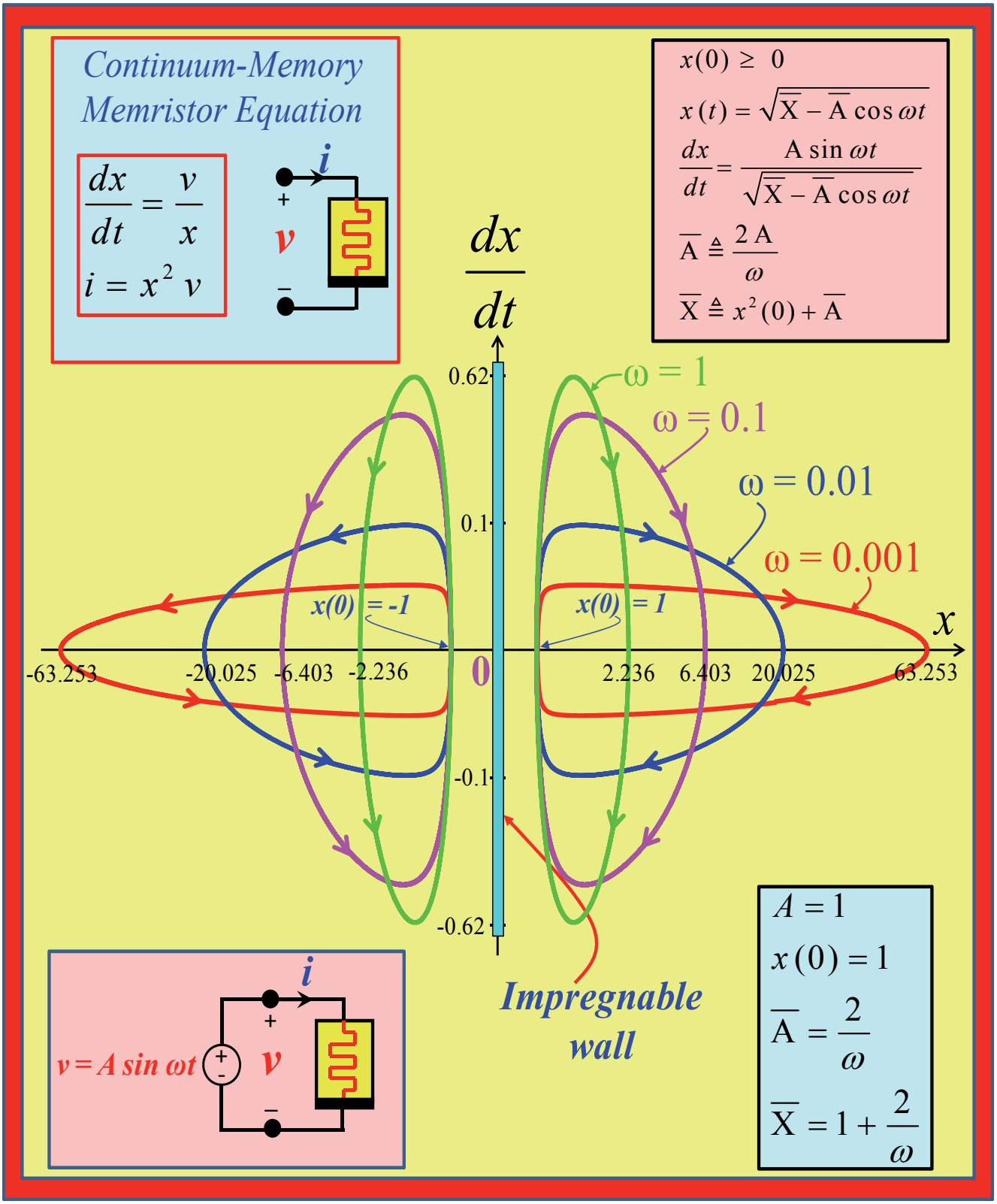
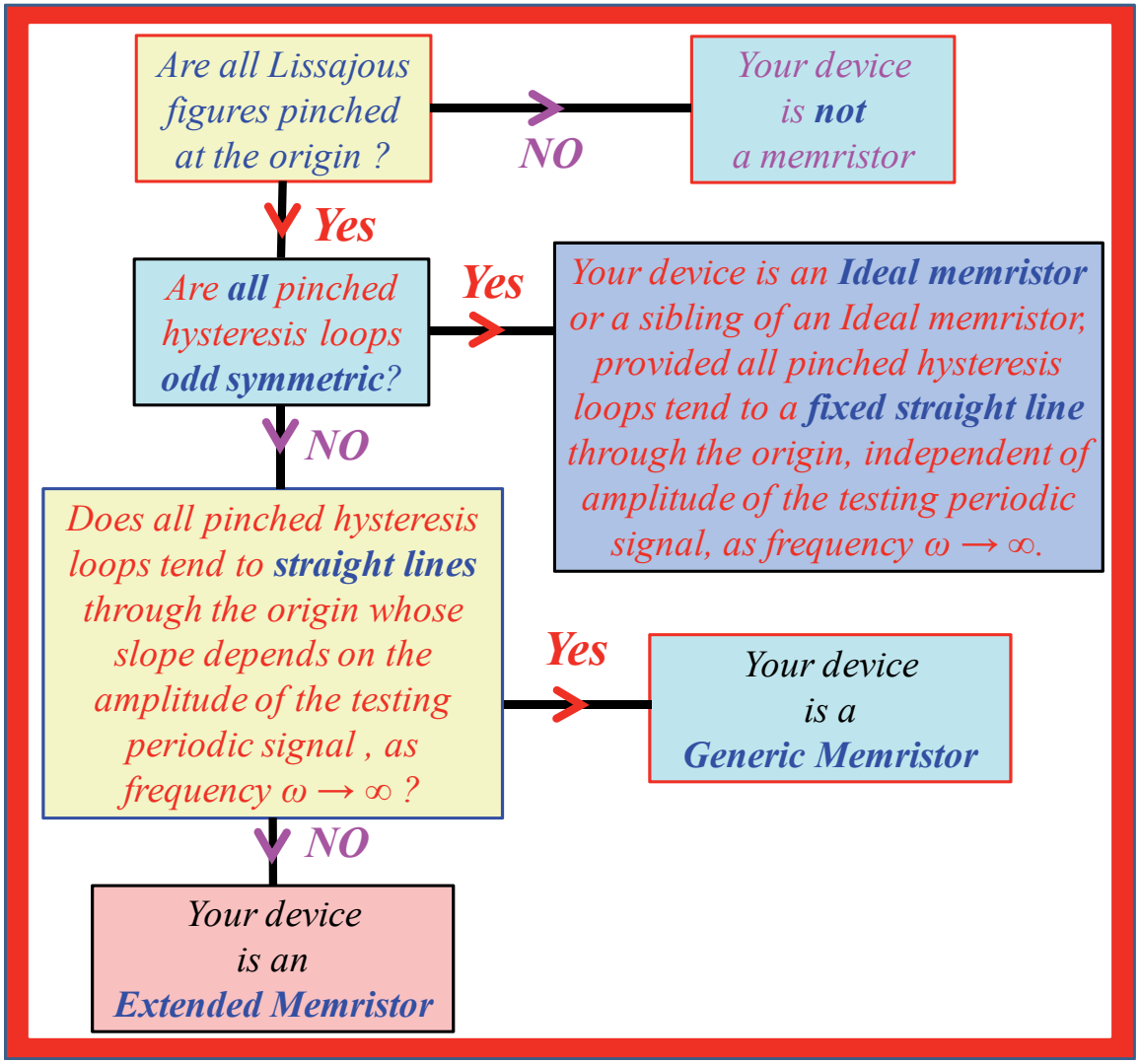


Fig. 36. Loci of (dx/dt) *vs.* $x(t)$ continuum-memory memristor (51) driven by a sinusoidal voltage source $v(t) = A \sin \omega t$, $A = 1$, $x(0) = 1$, for $\omega = 1$, 0.1, 0.01, and 0.001.The loci on the right are for $x(0) > 0$, while those on the left are for $x(0) < 0$.



Tab. 5. Four simple tests to identify and classify memristors.

Acknowledgments

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Appendix

Since nonlinear algebraic, or differential equations in general have no analytical solutions, they are usually solved by numerical methods, via standard softwares, or circuit simulators, such as SPICE. Unfortunately, numerical softwares are not foolproof, and cannot find all solutions if the equation has more than one solution. Piecewise-linear (PWL) methods are the best tools in such situations. In order to apply PWL methods, it is often desirable to represent a PWL curve by a PWL equation whose only nonlinearities are the *absolute-value* function $y = |x|$, and the *signum function* sgn x, defined in Fig. B.

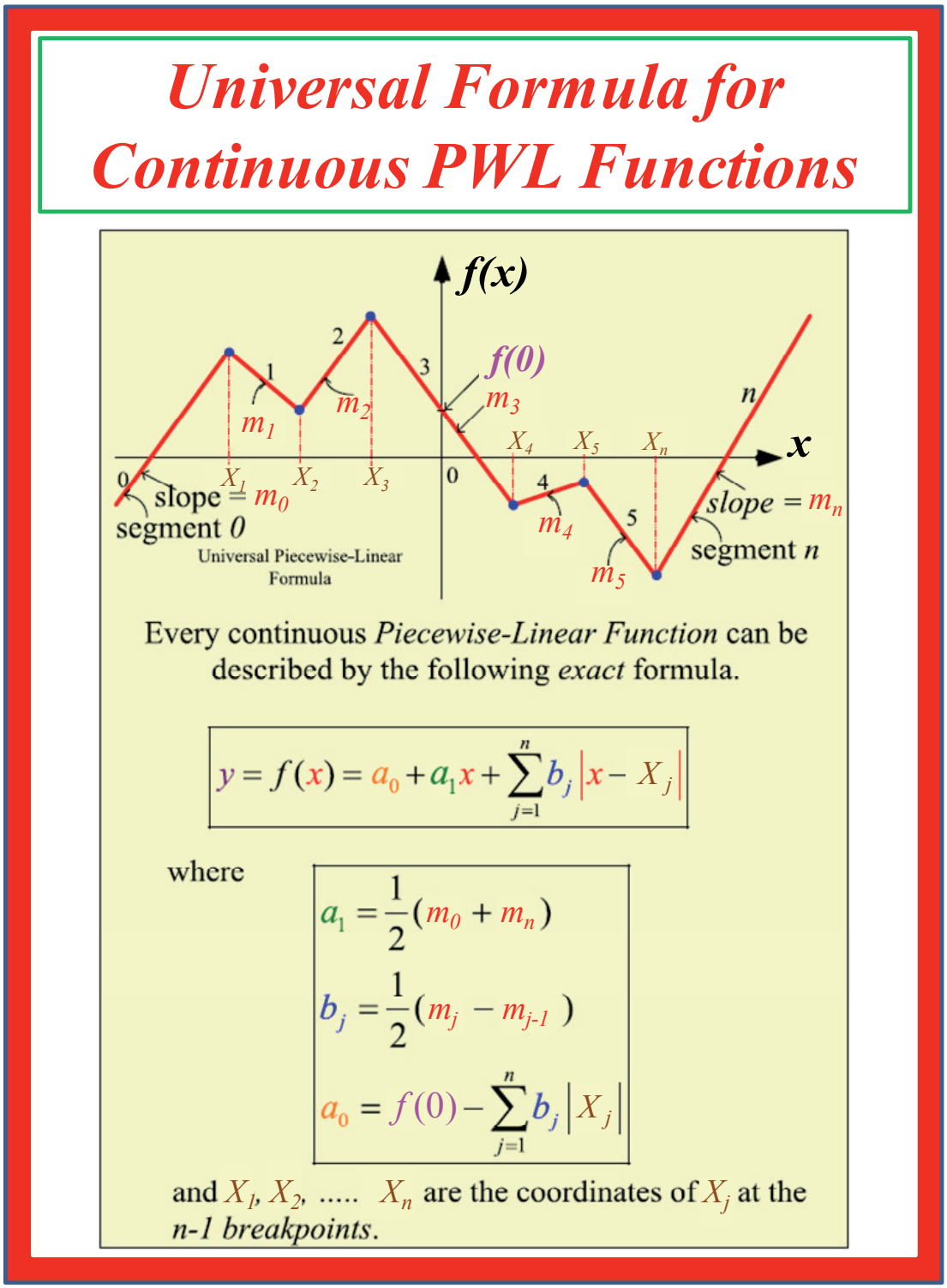
The good news is that unlike other nonlinear basis functions, the coefficients associated with the PWL formula presented in the following Tab. A, needed to specify any continuous PWL function can be obtained by inspection of the PWL curve! Simply label the the *segment number* consecutively from left to right, as segment 0, 1, 2,...,n, for an $(n+1)$-segment PWL curve, with corresponding slope $m_0, m_1, \ldots, m_n$. Label the x-coordinate of each corresponding *breakpoint* as $X_1, X_2, \ldots, X_n$. Any continuous PWL curve has a unique PWL formula (shown in Tab. A), with 2 coefficients a_0, a_1; n coefficients $X_1, X_2, \ldots, X_n$, and n coefficients $b_1, b_2, \ldots, b_n$.

The coefficient X_j is equal to the x-coordinate of breakpoint j. The coefficient a_1 is equal to half the sum of

the slope m_0 and m_n of the leftmost segment 0 and the rightmost segment n, respectively.

The coefficient b_j is equal to half the difference between the slope m_j and $m_{(j-1)}$ of segment j and segment $(j-1)$, respectively. The coefficient a_0 is chosen such that y is equal to the vertical intercept $f(0)$ of the PWL curve when $x = 0$ (see Tab. A).

All of these coefficients can be reconstructed from the following mnemonic rule: *Half Sum Half Difference then Null*.



Tab. A. Half Sum Half Difference Then Null PWL Formula

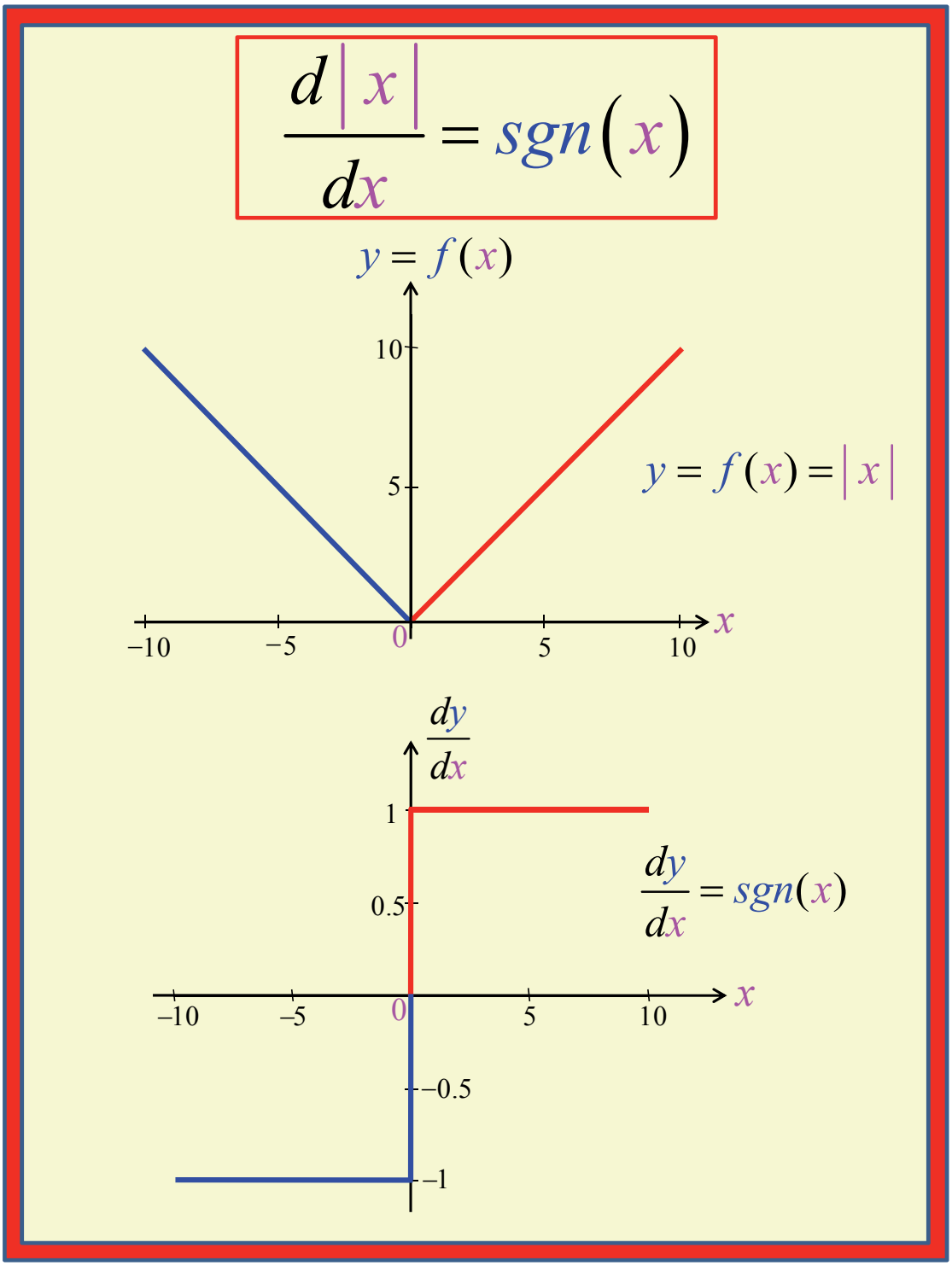


Fig. B. Graph of the *absolute-value function* of x, $|x|$, and the *signum function* of x, *sgn x*. They are the *basic functions* (building blocks) of *all* PWL functions.

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