A Memristor as Multi-Bit Memory: Feasibility Analysis

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Abstract. *The use of emerging memristor materials for advanced electrical devices such as multi-valued logic is expected to outperform today's binary logic digital technologies. We show here an example for such non-binary device with the design of a multi-bit memory. While conventional memory cells can store only 1 bit, memristor-based multi-bit cells can store more information within single device thus increasing the information storage density. Such devices can potentially utilize the non-linear resistance of memristor materials for efficient information storage. We analyze the performance of such memory devices based on their expected variations in order to determine the viability of memristor-based multi-bit memory. A design of read/write scheme and a simple model for this cell lay grounds for full integration of memristor multi-bit memory cell.*

Keywords

Memristor, multi-bit memory, noise margin

1. Introduction

The quest for yet higher performance, energetic efficiency and market growth for information storage pushes the boundaries of existing complementary metal oxide semiconductor (CMOS) technology to its physical limits [1], [2]. The predicted end of roadmap for CMOS set grounds for other candidate technologies that are expected to emerge. The fundamental studies of material physics overlap with this emerging field of beyond-CMOS technologies, where novel paradigms are set for providing new concepts and materials for the foundation of nano-electronics technology beyond the era of silicon. Among such emerging technologies are materials that feature a non-linear resistance trace that can also be "programmed" to store their resistive state. These materials are known as memristors, and their existence was predicted by Leon Chua in 1971 [3], and they were further analyzed theoretically by Sung Mo Kang [4]. Memristor devices were fabricated by HP labs for the first time [5]. Since 2008, this type of devices has sparked vast interest in the scientific community. Memristive devices hold a strong promise for producing low voltage ReRAM memories [7], [8], [9] since they require low power and can be easily integrated within standard fabrication process. However, some challenges remain for the advancement of viable memristor-based technologies, including the architecture of memristor arrays [7], [10].

One important and promising application of these technologies is the realization of multi-bit random access memory [11–17]. Inspired by the success of multi-bit flash memory, that proved to be highly efficient in high memory density, there have been several recent attempts to fabricate such multi-bit cells with memristors [18–24]. The main questions remaining for understanding the potential of memristors are their physical limitations and reliability in storing information, and how many bits per cell can be stored?

Herein, we develop a methodology to analyze the upper bound of information density of memristor multi-bit cells (MBC). Based on the TiO_2 prototypical system we consider variations in electron mobility, process related physical dimensions, concentration and diffusion coefficient of oxygen vacancy. These variations are taken into account for estimating the overall uncertainty in the expected resistivity response of a memristor memory cell and therefore can be mapped into a general form of noise level restricting the number of resistance values to be used for representing information stored in the device. Achieving an understanding of the potential and limitations of such multi-valued memories is imminent for the advancement of memristor technologies.

The physical mechanism on which memristive materials such as TiO_2 and other metal oxides change their resistivity is yet fully understood. The most common model for this phenomenon is related to the diffusion of oxygen vacancies in response to electron current flow, enabling the resistivity non-linearities of the material. Throughout this work we use the Pickett's model [25] that is considered as the reference model for memristors [26].

2. Memristor as Multi-bit Memory

2.1 Basic Concept

A realization of the redox memristor as an analog memory cell, can be achieved by mapping the continuously varying resistance of the memristor material into more than two resistance states, thus defining the multi-bit nature of the memory. For example, a 2 bit memory will introduce 4 states, i.e. the first state is the Low Resistance State (LRS) (see Fig. 1(d)) and 2 more intermediate states are defined between the LRS and High Resistance State (HRS). However, there are remaining challenges for quantizing the resistance of the memristor into discrete states at standard conditions. Deviations from the programmed resistance value are expected mostly due to temperature effects [27]. An ensemble of memristor devices is expected to produce even higher level of variations due to uncertainty in device critical dimensions and due to other small variations between (presumably identical) devices. The resistance space is then divided into discrete values for representing the stored data (i.e. information bits), each value has its own noise margins. The noise margin indicates the uncertainty in resistance signal i.e., the values of which cannot be associated with stored information.

One should note that while the span of a memristor's resistance typically covers the values $10^2\,\Omega \le R \le 10^5\,\Omega$, it is challenging to use the full range of resistance values. Since the typical operating voltage and currents for programming memristors are 1–3 V and 100 μA [5], the resistivity values are limited to smaller than $10^4\,\Omega$. Another aspect of the resistance range is related to the read/write (R/W) speed of devices with varying resistivity (mediated by their RC) and retention time [28]. Yet, an advantage of the discrete levels method is that a memristor can be treated as digital entity and consequently all noises can easily be corrected, even under process variations that cause for device mismatch, or if exist, memristor programming mismatch.

2.2 Interfacing the Memory Cell

As the main requirement from such memory cells is the ability to read and write stored information, herein we discuss a simple mechanism for interfacing the memristor multi-bit memory (see Fig. 2), taking into account the physical mechanism of such memristor devices. The presented R/W mechanism shows feasibility of the discretization concept of a memristors, taking into account the noise margins and thereby bit density per cell and constitutes a foundation for such technology, as shown in the next section.

Reading process: Interfacing memristors requires the use of analog to digital conversion (ADC). A possible implementation of such conversion is illustrated schematically in Fig. 2. Here, a current source drives a memristor

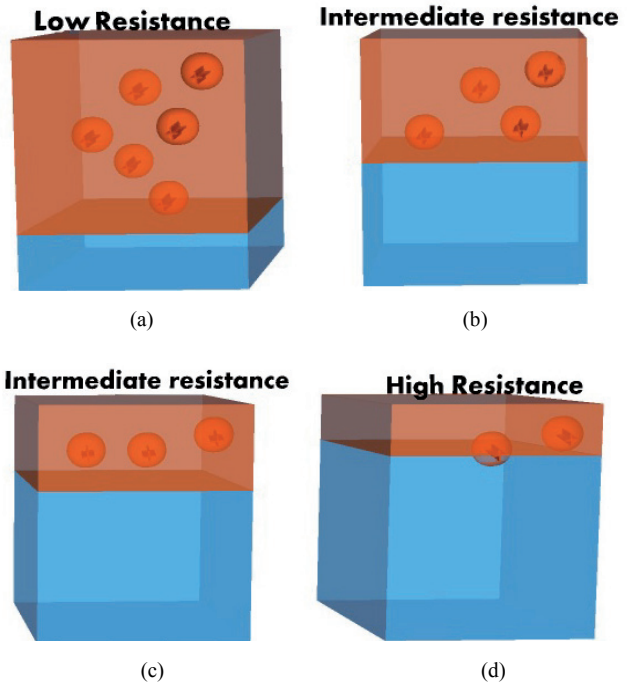

Fig. 1. Resistance field of the memristor. Blue color represents the depletion layer (oxygen vacancies shown as positive atoms).

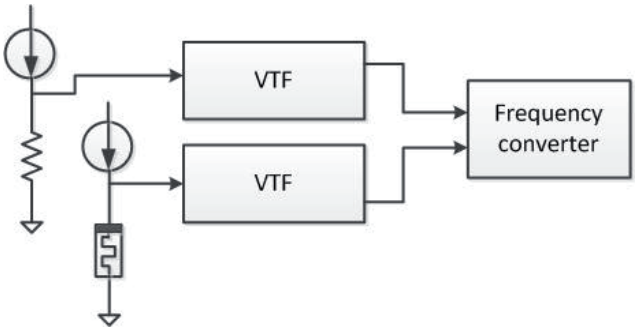

Fig. 2. Possible implementation of an interface for reading memristor device using ADC.

and a reference current is input into a known reference resistance. The two voltages can be converted into frequency and then the pulse trains can be counted and divided resulting in a digital number, as was reported in detail in ref [29–31].

Writing process: In general, there are two ways to program a memristor for multi valued resistivity:

1. Reading the memristor value prior to its programming.

2. Reset the memristor before writing to its initial state.

The first option is slower since it requires reading the value of the memristor. In addition, it requires having more than one writing current (at least 8 different currents), since moving the resistance is typically non-symmetric in respect to the two directions. In this paper our analysis assumes the second approach with one current for programming. We thus consider this option as the worst-case scenario for noise margin.

3. Memristor Noise Margin (MNM)

In principle, one could define an infinite number of resistance states in an ideal device. However, as the number of resistance states increases, the relative noise and errors in the read/write process increase accordingly. Here we ask: what is the maximum number of such discrete states that would still allow a correct operation of the memory device. It is therefore essential to define the noise margins.

The development of the memristor predictive physical model is not yet available for memristor devices except to the regression model of reference [5]. We analyze the expected noise margin that can be fitted to empirical data, using this model. Furthermore, the analysis we performed using the nonlinear resistance model is general, and can be easily applied to other models. The nonlinear resistance model we use:

$$\frac{dw(t)}{dt}=\begin{cases} f_{off}\sinh\left(\dfrac{i}{i_{off}}\right)\exp\left(-\exp\left(\dfrac{w-a_{off}}{w_c}-\dfrac{|i|}{b}\right)-\dfrac{w}{w_c}\right) & i>0 \\ f_{on}\sinh\left(\dfrac{i}{i_{on}}\right)\exp\left(-\exp\left(-\dfrac{w-a_{on}}{w_c}-\dfrac{|i|}{b}\right)-\dfrac{w}{w_c}\right) & i<0 \end{cases} \tag{1}$$

where f_{on}, f_{off}, i_{on}, i_{off}, a_{on}, a_{off}, b and w_c are empirical parameters deduced from the regression [5].

We analyze the transformation of the depletion region area to resistance with the linear and non-linear model [6]. Both known models are shown. The non-linear model, shown in (2) and the linear model in (3) are given below. The linear resistance model was slightly modified in order to take account for the device depletion region at all resistance values. Equation (3) represents the modified linear model.

$$R=R_{on}e^{\frac{\lambda}{(w_{off}-w_{on})}(w-w_{on})},\lambda=\ln(\frac{R_{on}}{R_{off}}) \tag{2}$$

$$R=R_{off}\frac{(w-w_{on})}{w_{off}-w_{on}}+R_{on}\left(1-\frac{w-w_{on}}{w_{off}-w_{on}}\right) \tag{3}$$

where R_{on} and R_{off} are the resistance minimum and maximum values, w_{on} and w_{off} is the depletion layer widths, and w is the updated position of the depletion layer.

Using the nonlinear model, we derive the margins for a general variable p_i:

$$\frac{\partial R}{\partial p_i}=\frac{\partial R}{\partial w}\frac{\partial w}{\partial p_i}=\frac{\lambda R_{on}}{(w_{off}-w_{on})}e^{\frac{\lambda(w-w_{on})}{(w_{off}-w_{on})}}\frac{\partial w}{\partial p_i}, \tag{4}$$

$$w=\int_{-\infty}^{t0}\frac{dw(t)}{dt}dt$$

where $p_1=a_{\text{on}}$ (or a_{off}), $p_2=i_{\text{on}}$ (or i_{off}), $p_3=f_{\text{on}}$ (or f_{off}). $dw(t)/dt$ is given in (1) and can be evaluated numerically. The maximum resistance variation is therefore:

$$\begin{aligned} dR=&\frac{\partial R}{\partial a_{on/off}}\Delta a_{on/off}+\frac{\partial R}{\partial i_{on/off}}\Delta i_{on/off} \\ &+\frac{\partial R}{\partial i(t)}\Delta i(t)+\frac{\partial R}{\partial f_{on/off}}\Delta f_{on/off} \end{aligned} \tag{5}$$

A direct expression for w is inaccessible; however, an implicit dependence of the highest possible variation of the resistivity on the set of parameters $\{p\}$ is obtained via estimation of their time period [5]. We, therefore, derive dR/dp as a function of time and remove the time dependence by taking the highest possible variation for all variables $\{p\}$ as:

$$dR=dR_{\max}=\sum_i\max\left(\frac{\partial R(t)}{\partial p_i}\right)\Delta p_i\,. \tag{6}$$

In (6) we calculate the allowed resistance variations dR considering the worst case scenario. Equation (6) accounts for the resistance variations within one discretized resistance level and thus does not account for the accumulated error (since the error produced by a specific parameter is directional). Therefore, the more general expression for the overall noise margins is provided with (7) below:

$$\begin{aligned} &dR_{allowed}=(dR_n-\delta R_i)-dR_{n-1}, \\ &\delta R_i=\max(p_i)\big|_{dR>0} \end{aligned} \tag{6}$$

where $\max(p_i)$ will be the maximum total reversed error (or in our case the parameter b). Equation (7) states that the allowed resistance variations, $dR_{allowed}$, depend on the resistance variations of neighboring resistance levels, dR_n, dR_{n-1}.

4. Simulation Results - MNM Analysis

In order to perform the MNM analysis, we assumed variations of the HP memristor model, with parameter values, shown in Tab. 1 [5] additionally to the reported barrier width change (1 nm – 2 nm).

Variable	a_{off} [nm]	f_{off} [μm/s]	i_{off} [μA]	b [μA]	w_{C} [pm]
Values	1.20 ± 0.02	3.5 ± 1	115 ± 4	500 ± 70	107 ± 4

Tab. 1. Parameters values that were used for the case of for $i>0$.

Equation (1) was solved using a high-order finite difference expansion of w on a uniform grid of time-step Δt. This method is well suited for numerically solving differential equations on regular grids. [32–33] The smoothness of the numerical results was achieved by convergence of the order of the expansion. In this scheme, the value of the function derivative at some grid point is calculated based on the value of this function on neighboring grid points. Specifically for this work we used an initial condition to the solution, from which we derived the solution on the time grid at third-order expansion. At grid points close to the grid boundary we used a lower order. w was solved for an applied current pulse of a half sinusoidal waveform at

frequency of 2 MHz (see Fig. 4). By keeping the time period of the current pulse constant and varying its amplitude, we search for a current amplitude which will change the resistance to the lowest distinguishable value in the range of kΩ (see Fig. 3(a) and (b)). This scheme is designed to provide highest possible resistance steps with minimum noise margins. Since the resistance curves are asymmetric, the transition from LRS to HRS is more gradual than the transition from HRS to LRS. We found that such desirable gradual transition can be achieved by amplitude of 2.3 mA, providing the steps shown in Fig. 3 below. This can also be seen in Fig. 4 where we used a range of current amplitudes and calculated their corresponding steady state resistance values.

In order to simulate the margins, we used a base resistance of 100 Ω and a R_{off}/R_{on} ratio of 500 and evaluated the parameters variation, dR. The noise margins corresponding to the parameters of (1) are evaluated based on the resistance steps of Fig. 3. (The resistance values of the steps are 100 Ω, 986 Ω, 1521 Ω, 1952 Ω corresponding to w = 1 nm, 1.368 nm, 1.438 nm, 1.478 nm, respectively).

While this analysis is in principle mathematically correct, it can be improved by casting physical arguments to some of the parameters in use. One can note that the variations listed in Tab. 2 and 3 are large and in principle they should indicate that multi-bit memory applications are infeasible. However, we argue here that the activation energy for oxygen vacancy diffusion should remain independent and we therefore assume that errors associated with the parameter i_{off} can be ignored as it assumed to be constant. Furthermore, the parameter w_c can be regarded as normalizing constant in spite of its large contribution to the overall resistance variation. Moreover, it shows a constant variation in relation to the initial conditions of the depletion area.

variable	w = 1 nm	w = 1.368 nm	w = 1.438 nm	w = 1.478 nm
a_{off}	-66.1	-67.9	-58.7	-54.7
f_{off}	-603	-330	-259	-220
i_{off}	1.76e4	1.76e4	1.76e4	1.76e4
B	46.3	85.6	105	117
w_C	-1.81e4	1.8e4	-3.61e3	-1.79e4
$dR_{Allowed}$	800.4	430	314	
dR[1]	668.7	397.9	318.2	274.7

Tab. 2. The resistance variations as a function of [5] parameters deviations assuming the linear model of (3).

variable	w = 1 nm	w = 1.368 nm	w = 1.438 nm	w = 1.478 nm
a_{off}	-26.1	-22.1	-17.7	-7.74
f_{off}	-388	-272	-235	-204
i_{off}	1350	1110	990	886
b	37	81.9	99.8	115
w_C	-668	-582	-537	-495
$dR_{Allowed}$	849	453.2	331	
dR[1]	-414.1	-294.1	252.7	211.74

Tab. 3. Resistance variations as a function of parameter values assuming the nonlinear resistance model of (2).

[1] This value was obtained without the error contribution from the parameter i_{off} and w_c.

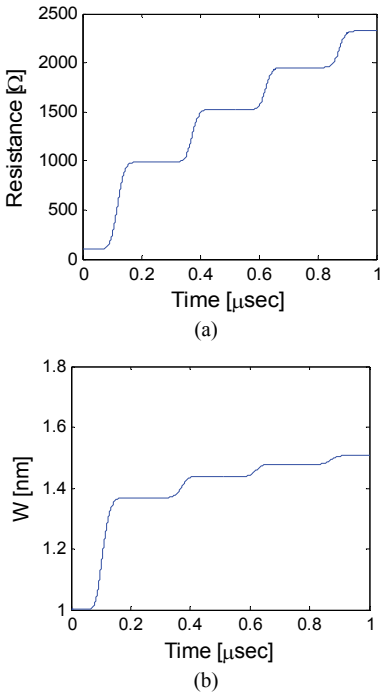

Fig. 3. Memristor (a) resistance, (b) depletion layer width as a function of time for 4 half sin pulses.

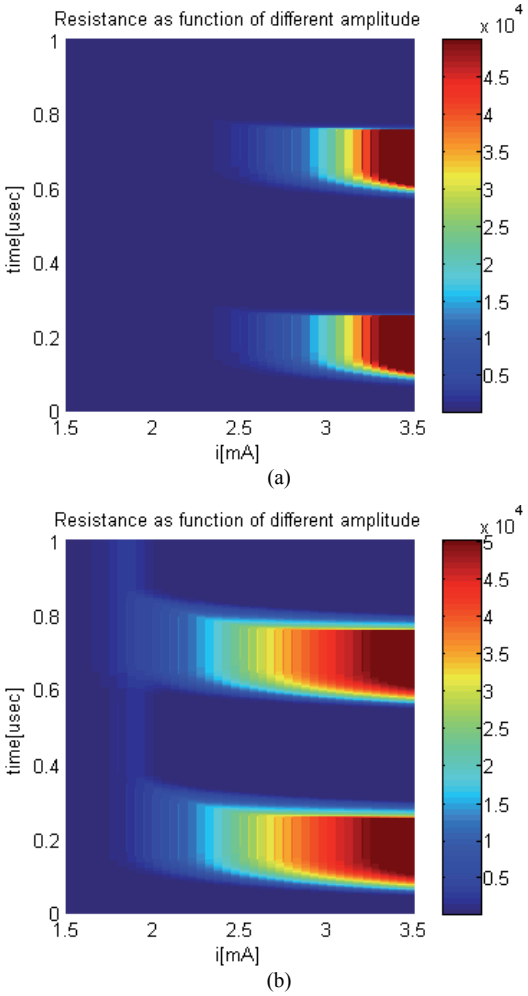

Fig. 4. $i(t)$ with changing amplitude: (a) linear resistance model, (b) nonlinear model.

5. Conclusions and Discussion

This work provides a method for evaluating the noise margins of memristor-based memory devices. Using this method we performed a numerical analysis of multi-bit memristor. This analysis evaluates the noise margins associated with physical variations of devices. We find that the linear model predicts larger resistance variations compared to the nonlinear model. However, even with the larger variations of the linear model we find the multi-bit memory feasible.

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References

[1] BERNSTEIN, K., CAVIN, R. K., POROD, W., SEABAUGH, A., WELSER, J. Device and architecture outlook for beyond CMOS switches. *Proceedings of the IEEE*, Dec. 2010, vol. 98, no. 12, p. 2169–2184. DOI: 10.1109/JPROC.2010.2066530

[2] STRUKOV, D. B., STEWART, D. R., BORGHETTI, J., LI, X., PICKETT, M., RIBEIRO, G. M., ROBINETT, W., SNIDER, G., STRACHAN, J. P., WU, W., XIA, Q., YANG, J. J., WILLIAMS, R. S. Hybrid CMOS/memristor circuits. In *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2010, p. 1967–1970. DOI: 10.1109/ISCAS.2010.5537020

[3] CHUA, L. O. Memristor – the missing circuit element. *IEEE Transactions on Circuit Theory*, 1971, vol. 18, no. 5, p. 507–519. DOI: 10.1109/TCT.1971.1083337

[4] CHUA, L. O., KANG, S. M. Memristive devices and systems. *Proceedings of the IEEE*, Feb. 1976, vol. 64, no. 2, p. 209–223. DOI: 10.1109/PROC.1976.10092

[5] PICKETT, M. D., STRUKOV, D. B., BORGHETTI, J. L., YANG, J. J., SNIDER, G. S., STEWART, D. R., WILLIAMS, R. S. Switching dynamics in titanium dioxide memristive devices. *Journal of Applied Physics*, Oct. 2009, vol. 106, no. 7, p. 074508–1 to 074508–6. DOI: 10.1063/1.3236506

[6] KVATINSKY, S., FRIEDMAN, E. G., KOLODNY, A., WEISER, U. C. TEAM: ThrEshold Adaptive Memristor model. *IEEE Transactions on Circuits and Systems I: Regular Papers,* Jan. 2013, vol. 60, no. 1, p. 211–221. DOI: 10.1109/TCSI.2012.2215714

[7] LINN, E., ROSEZIN, R., KÜGELER, C., WASER R. Complementary resistive switches for passive nanocrossbar memories. *Nature Materials*. 2010, vol. 9, no. 5, p. 403–406. DOI: 10.1038/nmat2748

[8] AKINAGA, H., SHIMA, H. Resistive Random Access Memory (ReRAM) based on metal oxides. *Proceedings of the IEEE*, Dec 2010, vol. 98, no. 12, p. 2237–2251. DOI: 10.1109/JPROC.2010.2070830

[9] HO, Y., HUANG, G. M., LI, P. Nonvolatile memristor memory: Device characteristics and design implications. In *IEEE/ACM International Conference on Computer-Aided Design - Digest of Technical Papers, ICCAD*. 2009, p. 485–490. ISSN: 1092-3152

[10] NIU, D., CHEN, Y., XU, C., XIE, Y. Impact of process variations on emerging memristor. In *47th ACM/IEEE Design Automation Conference (DAC)*. 2010, p. 877–882. ISSN: 0738-100X

[11] CHAE, D., HAN, J. Flash memory devices having multi-bit memory cells therein with improved read reliability. *US Patent 20110197015*, 11-Aug-2011. Available at: http://www.google.tl/patents/US20110197015

[12] PARK, J. W. Integrated circuit memory devices having reconfigurable nonvolatile multi-bit memory cells therein and methods of operating same. *US Patent 5862074*, 19-Jan-1999. Available at: http://www.google.com.ar/patents/US5862074

[13] KIM, M., KIM, M., LEE, J. W., TIWARI, S. Multi-bit functional NOR type SONOS memories. In *Device Research Conference*. 2008, p. 63–64. DOI: 10.1109/DRC.2008.4800735

[14] YANG, J. Y. M., WU, Y. Multi-bit silicon nitride charge-trapping non-volatile memory cell. *US Patent 6897533*, 24-May-2005. Available at: http://www.google.com/patents/US6897533

[15] SUGIZAKI, T., KOBAYASHI, M., ISHIDAO, M., MINAKATA, H., YAMAGUCHI, M., TAMURA, Y., SUGIYAMA, Y., NAKANISHI, T., TANAKA, H. Novel multi-bit SONOS type flash memory using a high-k charge trapping layer. In *Symposium on VLSI Technology, Digest of Technical Papers*. 2003, p. 27–28. DOI: 10.1109/VLSIT.2003.1221069

[16] SOHN, J. I., CHOI, S. S., MORRIS, S. M., BENDALL, J. S., COLES, H. J., HONG, W.K., JO, G., LEE, T., WELLAND, M. E. Novel nonvolatile memory with multibit storage based on a ZnO nanowire transistor. *Nano Letters,* Nov. 2010, vol. 10, no. 11, p. 4316–4320. DOI: 10.1021/nl1013713

[17] WU, C. Y. Scalable multi-bit flash memory cell and its memory array. *US Patent 6605840*, 12-Aug-2003. Available at: http://www.google.tl/patents/US6605840

[18] YANG, X., CHEN, A. B. K., CHOI, B. J., CHEN, I. W. Demonstration and modeling of multi-bit resistance random access memory. *Applied Physics Letters*, Jan. 2013, vol. 102, no. 4, p. 043502-1–043502-4. DOI: 10.1063/1.4790158

[19] DURAISAMY, N., MUHAMMAD, N. M., KIM, H. C., JO, J. D., CHOI, K. H. Fabrication of TiO_2 thin film memristor device using electro-hydrodynamic inkjet printing. *Thin Solid Films*, May 2012, vol. 520, no. 15, p. 5070–5074. DOI: 10.1016/j.tsf.2012.03.003

[20] KAVEHEI, O., CHO, K., LEE, S., KIM, S. J., AL-SARAWI, S., ABBOTT, D., ESHRAGHIAN, K. Fabrication and modeling of Ag/TiO_2/ITO memristor. In *IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2011, p. 1–4. DOI: 10.1109/MWSCAS.2011.6026575

[21] KUMAR, A., RAWAL, Y., BAGHINI, M. S. Fabrication and characterization of the ZnO-based memristor. In *International Conference on Emerging Electronics (ICEE)*. 2012, p. 1–3. DOI: 10.1109/ICEmElec.2012.6636244

[22] PRODROMAKIS, T., MICHELAKIS, K., TOUMAZOU, C. Fabrication and electrical characteristics of memristors with TiO_2/TiO_{2+x} active layers. In *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2010, p. 1520–1522. DOI: 10.1109/ISCAS.2010.5537379

[23] VERRELLI, E., TSOUKALAS, D., NORMAND, P., KEAN, A. H., BOUKOS, N. Forming-free resistive switching memories based on titanium-oxide nanoparticles fabricated at room temperature. *Applied Physics Letters,* Jan. 2013, vol. 102, no. 2, p. 022909. DOI: 10.1063/1.4775760

[24] RAJACHIDAMBARAM, J. S., MURALI, S., JR, J. F. C., GOLLEDGE, S. L., HERMAN, G. S. Bipolar resistive switching in an amorphous zinc tin oxide memristive device. *Journal of Vacuum Science & Technology B Microelectronics and Nanometer Structures,* Jan. 2013 vol. 31, no. 1, p. 01A104. DOI: 10.1116/1.4767124

[25] ABDALLA, H., PICKETT, M. D. SPICE modeling of memristors. In *IEEE International Symposium on Circuits and Systems (ISCAS)*. Rio de Janeiro (Brazil), 2011, p. 1832–1835. DOI: 10.1109/ISCAS.2011.5937942

[26] ASCOLI, A., CORINTO, F., SENGER, V., TETZLAFF R. Memristor model comparison. *IEEE Circuits*, 2013, vol. 13, no. 2, p. 89–105, 2013. DOI: 10.1109/MCAS.2013.2256272

[27] WALCZYK, C., WALCZYK, D., SCHROEDER, T., BERTAUD, T., SOWINSKA, M., LUKOSIUS, M., FRASCHKE, M., WOLANSKY, D., TILLACK, B., MIRANDA, E., WENGER, C. Impact of temperature on the resistive switching behavior of embedded-based RRAM devices. *IEEE Transactions on Electron Devices,* Sep. 2011, vol. 58, no. 9, p. 3124–3131. DOI: 10.1109/TED.2011.2160265

[28] HA, S. D., RAMANATHAN, S. Adaptive oxide electronics: A review. *Journal of Applied Physics*, Oct. 2011, vol. 110, no. 7, p. 071101-1–071101-20. DOI: 10.1063/1.3640806

[29] KESTER, W., BRYANT, J. Voltage-to-frequency converters. *MT-028 Tutorial*, 2009. Available at: http://www.analog.com/media/cn/training-seminars/tutorials/MT-028.pdf

[30] TANIGUCHI, K., SAKAI, T. A new voltage to frequency converter. *IEEE Transactions on Computers*, Oct. 1975, vol. 24, no. 10, p. 1035–1036. DOI: 10.1109/T-C.1975.224122

[31] SHOR, J., LURIA, K., ZILBERMAN, D. Miniaturized BJT-based thermal sensor for microprocessors in 32- and 22-nm technologies. *IEEE Journal on Solid-State Circuits,* Nov. 2013, vol. 48, no. 11, p. 2860–2867. DOI: 10.1109/JSSC.2013.2280039

[32] FORNBERG, B. Generation of finite difference formulas on arbitrarily spaced grids. *Mathematics Computation*. 1988, vol. 51, p. 699-706. DOI: 10.1090/S0025-5718-1988-0935077-0

[33] NAVEH, D., KRONIK, L., TIAGO, M. L., CHELIKOWSKY, J. R. Real-space pseudopotential method for spin-orbit coupling within density functional theory. *Physical Review B*. October 2007, vol. 76, p. 153407. DOI: 10.1103/PhysRevB.76.153407

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