High-Precision CMOS Analog Computational Circuits Based on a New Linearly Tunable OTA

Ali NADERI SAATLO

Dept. of Electrical-Electronics Engineering, Urmia Branch, Islamic Azad University, Urmia, Iran

a.naderi@iaurmia.ac.ir

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Abstract. *Implementation of CMOS current-mode analog computational circuits are presented in this paper. A new Linearly Tunable OTA is employed in a modified structure as a basic building block for implementation of the circuits either linear or nonlinear functions. The proposed trans-conductance amplifier provides a constant G_m over a wide range of input voltage which allows the implementation of high precision computational circuits including square rooting, squaring, multiplication and division functions. Layout pattern of the proposed circuit confirms that the circuit can be implemented in 102 μm × 69 μm active area. In order to verify the performance of the circuits, the post layout simulation results are presented through the use of HSPICE and Cadence with TSMC level 49 (BSIM3v3) parameters for 0.18 μm CMOS technology, where under supply voltage of 1.8 V, the maximum relative error of the circuits within 500 μA of input range is about 11 μA (2.2 % error) and the THD remains as low as 1.2 % for the worst case. Moreover, the power dissipation of the complete structure is found to be 0.66 mW.*

Keywords

Computational circuits, trans-conductance circuit, analog design, current mode

1. Introduction

Analog computational circuits are very useful building blocks finding various applications in the signal processing domain. These circuits realize several functions such as multiplication, division, squaring, square rooting and etc. which are widely used in disk drives [1], hearing aids [2], medical equipment [3], modulators [4], artificial neural networks [5] and fuzzy control systems [6]. There are a lot of techniques to implement analog functional circuits [7–18] which can be roughly categorized in three main groups.

The first group is based on the trans-linear (TL) principle introduced in [7]. This group is also classified in two subgroups including BJT and MOS trans-linear circuits. In bipolar transistors, it employs the exponential characteristic of current and voltage [7], [8]. In this method the cause of error originates from the nonzero values of the base currents and of the temperature dependence of the bipolar transistor parameters (the thermal voltage is linearly increasing with temperature and the saturation current has an exponential dependence on temperature). In CMOS technology, TL principle relies on the exploiting of loop transistors operating either in weak inversion [9], [10] or strong inversion [11], [12]. For weak inversion, although it leads to circuits offering low power consumption, the dynamic range and the operation speed turn out to be limited. For the TL principle in strong inversion, the body effect is a serious problem in a way that this effect causes mismatch in the threshold voltages which in turn, influences the linearity and accuracy of the circuits, however in some studies this effect was properly discussed and a few techniques were proposed [13], [14].

The most important aspects of computational circuits include power consumption, operation speed, design cost, simplicity and area efficiency. Although in practice, most of these parameters trade with each other and several design techniques have been proposed [15], [16] to satisfy the compromise between these characteristics, but the main challenge in designing computational circuits is how to implement with minimal effort a large number of these functions [17]. One possible technique to do this is to design a multifunctional computational structure which is based on the possibility of a multiple use of the same structure as a core of the design. On the basis of this technique, if the design effort being mainly focused on the improving of the core performances, all of the functions which will be implemented through the use of the core structure will automatically be improved. From this point of view, the second and third groups can be also classified.

The second group emphasizes on the use of piecewise linear approximation method [18–20], expansion of the functions using Taylor series [21], [22] and presenting a new approximation [23], [24] in which each term of the approximated series is realized using a current-mode [18–21], [23], [24] or voltage-mode [22] basic building block. In order to make the realization of the functions simple, some of these approximations have used only second-order [21], [22] or third-order [18], [24] terms which

leads to low-precise implementation of computational circuits. Following this, the higher order approximations [20], [23] have been proposed to achieve higher accuracy at the expense of complex structure and consequently higher consumption of power. The complex structures reported in [25], [26], but not based on the piecewise linear approximation method or expansion of Taylor series or not CMOS-based circuits can be located in this group, owing to the fact that they also consume more power.

The third group deals with the structure based on the Operational Trans-conductance Amplifier (OTA). Although these structures can implement slightly less functions rather than the second group, but the advantages of reconfigurability, lower power consumption and higher accuracy encourage the designers to utilize this method. There are limited number of literatures on the use of OTAs for designing these circuits [27–30], while some of them do not allow multifunctional operation [27], [28] and some others suffer from having constant trans-conductance and not having entire linearity over the input range [29], [30]. This problem in turn influences the performance of the implemented computational circuits in terms of accuracy and efficiency.

The objective of this paper is to examine the applicability of a new Linearly Tunable OTA (LTOTA) as a basic building block which is employed in a modified structure to implement computational circuits either linear or nonlinear functions. The proposed trans-conductance amplifier provides a constant G_m over a wide range of input voltage which allows the implementation of high precision computational circuits. In addition, the proposed LTOTA behaves as a bipolar OTA in which its trans-conductance is linearly tuned by the bias current, therefore all of the bipolar based OTA configurations can be easily replaced by the CMOS LTOTA, while their performance nearly remains the same. Due to the simple and compact structure, the power consumption of the implemented circuits is comparatively low.

2. Circuit Description

In order to realize computational circuits, a CMOS based trans-conductance circuit is employed as a basic building block of the design. The proposed structure is shown in Fig. 1, where I_{in} is the input current. The trans-conductance gains of OTA_1 and OTA_2 can be varied by adjusting an external DC bias current of I_1 and I_2, respectively. According to the figure, the input current of I_{in} is injected into the OTA_1, which is employed as a current controlled grounded resistor. The voltage across the OTA_1 is then utilized as the input voltage for the OTA_2. Considering G_{m1} and G_{m2} as the trans-conductance gains of the OTA_1 and OTA_2 respectively, one can find the input-output relationship as follows:

$$\left.\begin{aligned} G_{m1}V_X &= I_{in} \\ G_{m2}V_X &= I_{out} \end{aligned}\right\} \Rightarrow I_{out} = \frac{G_{m2}}{G_{m1}} I_{in} . \qquad (1)$$

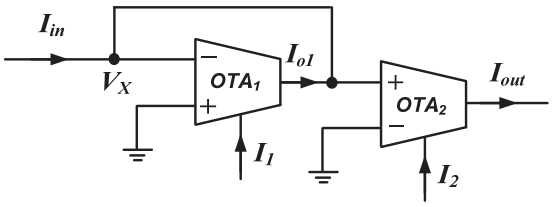


Fig. 1. Proposed structure for implementation of computational circuits.

If the trans-conductance of OTA_2 (G_{m2}) has the square-root proportion to its current, by keeping I_{in} and G_{m1} constant, the square-rooter circuit can be achieved. In the case of direct proportion of G_{m1} and G_{m2} to the current, the multiplier and divider circuits will be obtained. Also if $I_{in} = I_{Gm2}$ the squaring circuit is implemented. The implementation of these functions will be thoroughly discussed in Sec. 3.

2.1 Proposed CMOS OTA Circuit

Figure 2 shows the trans-conductance circuit which is the basic building block to implement computational circuits. The differential input voltage of V_{in} is applied in the form of $V_{in} = V_1 - V_2$, and I_a and I_{ss} represent the bias and tail currents, respectively. The operation of circuit is as follows:

Since the drain current of M_1 is constant ($I_{DS1} = I_a$), neglecting the body effect, V_{GS1} also has to remain constant; as a result any variation in the voltage of V_1, will be reflected to the source terminal (V_A) level-shifted by V_{GS1}. Supposing M_1 operates in saturation region, the voltage of this node is given by:

$$I_a = K(V_1 - V_A - V_{TH})^2 , \qquad (2)$$

$$V_A = V_1 - V_{TH} - \sqrt{\frac{I_a}{K}} \qquad (3)$$

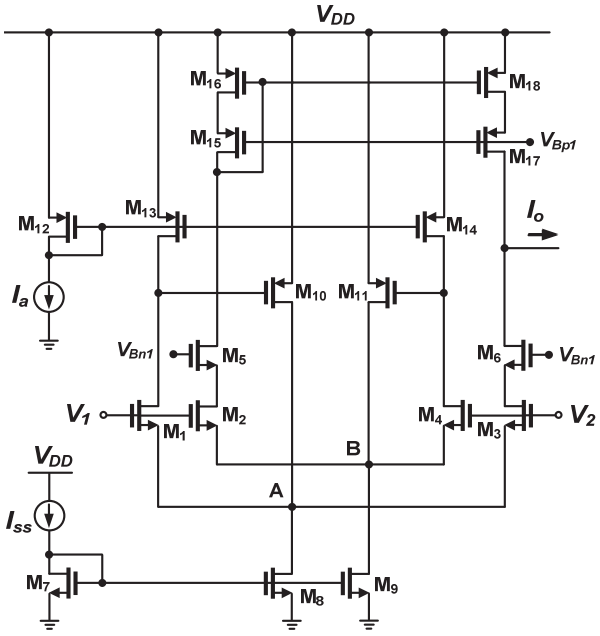


Fig. 2. Proposed OTA circuit.

where $K = 0.5\,\mu_0 C_{OX}(W/L)$ is related to trans-conductance parameter and V_{TH} is the threshold voltage of MOS transistor. The transistor M_3 works in saturation region as well, thus its current can be written as:

$$I_{DS3} = K(V_2 - V_A - V_{TH})^2 . \quad (4)$$

Replacing (3) in (4) yields:

$$I_{DS3} = K(V_2 - V_1 + \sqrt{\frac{I_a}{K}})^2 . \quad (5)$$

Similarly, one can find the current of transistor M_2 as:

$$I_{DS2} = K(V_1 - V_2 + \sqrt{\frac{I_a}{K}})^2 . \quad (6)$$

Transistors M_{10} and M_{11} sink extra currents of nodes A and B, respectively. This is due to the fact that I_{DS2} and I_{DS3} change with input voltage and since M_1 and M_4 have the constant current of I_a, in order to prevent M_2 and M_3 being in linear region, M_{10} and M_{11} are considered. Also M_5 and M_6 are employed as a cascode stage to provide high output impedance at the output node. V_{Bn1} is chosen in which these transistors operate in the saturation region.

The transistors M_{15}-M_{18} act as a current sub-tractor which form the output current as follows:

$$I_o = I_{DS2} - I_{DS3} = 4\sqrt{KI_a}\,(V_1 - V_2) \quad (7)$$

or:

$$I_o = 4\sqrt{KI_a}\,V_{in} . \quad (8)$$

From (8), it is obvious that G_m of the circuit is $4\sqrt{0.5\mu_0 C_{ox}(W/L)_{2,3} I_a}$ which can be adjusted via the bias current of I_a and also aspect ratio of transistors M_2 and M_3. In addition, it implies that I_a has the square root proportion with the trans-conductance gain. In order to have linearly tunable OTA, a current squaring circuit is employed in which its output will be applied as the bias current of the proposed OTA. Therefore, the next section will deal with current squaring circuit.

2.2 Current Squaring Circuit

The modified current squaring circuit which is based on the Translinear Loop (TL) principle is shown in Fig. 3 [31]. Supposing trans-conductance parameters of all transistors are well matched, considering translinear loop composed of M_1 to M_4, we have:

$$\sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} . \quad (9)$$

Writing KCL at nodes C and D:

$$I_{DS3} = \frac{I_{SQ}}{4} + I_x + I_b , \quad (10)$$

$$I_{DS4} = \frac{I_{SQ}}{4} - I_x + I_b \quad (11)$$

where I_b is bias current and I_x and I_{SQ} represent input and output currents, respectively. Considering $I_{DS1} = I_{DS2} = I_b$, substituting (10) and (11) into (9) and squaring both sides twice, the output current is given by:

$$I_{SQ} = \frac{I_x^2}{I_b} . \quad (12)$$

It is seen that the squaring of I_x is appeared at the output. Note that the bias current of I_b recognizes the input range of the circuit ($I_x \leq 2I_b$) as thoroughly discussed in [31].

2.3 Proposed Linearly Tunable OTA

The complete circuit of LTOTA is shown in Fig. 4, where the right side (M_1-M_{18}) specifies trans-conductance circuit where its G_m can be adjusted via I_{SQ} fed to transistors M_{13} and M_{14}. Transistors M_{s1}-M_{s4} form the core of squaring circuit and M_{19}-M_{36} provide required signals in a way that M_{19}-M_{24} produce the current of $2I_x$ and M_{25}-M_{36} yield $I_x + I_b$. Finally, the squaring current is mirrored through M_{12}-M_{14} to the trans-conductance circuit. Considering (12) and (8) as the output of squaring and trans-conductance circuits respectively, the final output can be written as:

$$I_{out} = 4I_x\sqrt{\frac{K}{I_b}}V_{in} . \quad (13)$$

Equation (13) indicates that the trans-conductance gain can be linearly tuned by the current of I_x, while K and I_b are constant values. Note that this linear relationship is the same as the trans-conductance gain in the bipolar-based OTA which is very useful in many applications [32]. Since the proposed LTOTA is realized by MOS transistors all in saturation region, therefore it is very suitable and efficient for fabricating in CMOS process.

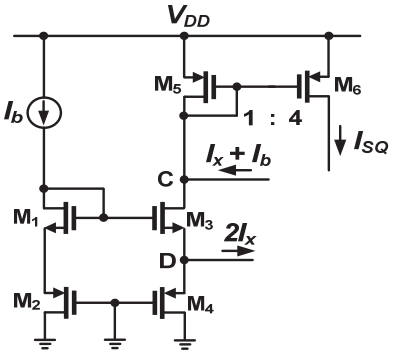


Fig. 3. Modified current squaring circuit.

3. Post Layout Simulation Results

In this section, post layout simulation results of the proposed circuits and their applications are presented through the use of HSPICE and Cadence with TSMC level 49 (BSIM3v3) parameters for 0.18 μm CMOS technology

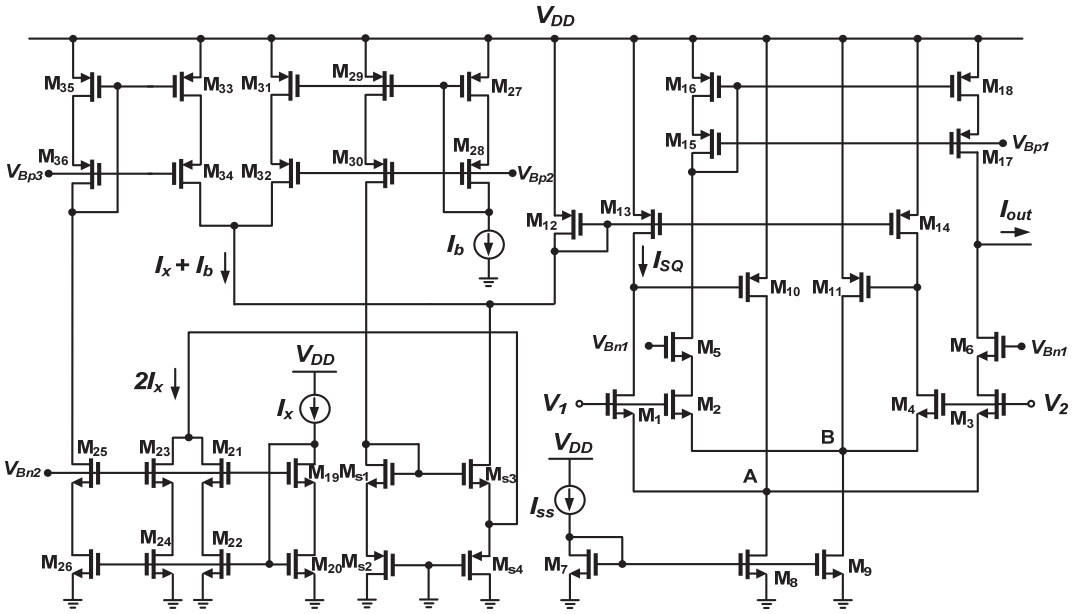


Fig. 4. Complete schematic of LTOTA circuit.

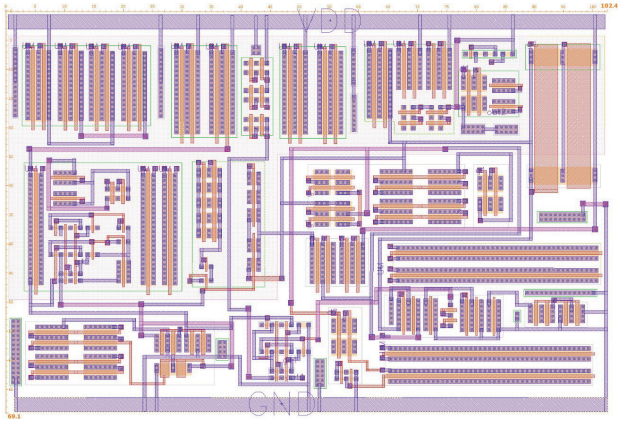


Fig. 5. Layout pattern of the proposed LTOTA.

so as to verify the performance of the circuits. Layout pattern of the proposed LTOTA is illustrated in Fig. 5 which confirms that the circuit can be implemented in 102 µm × 69 µm active area. The aspect ratios of transistors are given in Tab. 1 and the power supply voltage is set to $V_{DD} = 1.8$ V.

Figure 6 shows the linear output current resulted from subtraction of two nonlinear input currents (I_{DS2} and I_{DS3}) which were formulated in (5), (6) and (8). The constant G_m in the corresponding range of the input voltage is shown in the figure as well. For this simulation, the bias current of I_a which determines the trans-conductance is 100 µA and the tail current of I_{ss} is set to 300 µA. It should be pointed out that the high linearity of G_m comes from symmetrical configuration of the circuit which provides the symmetric currents of I_{DS2} and I_{DS3} as proved in (5) and (6), in which their subtraction is entirely linear.

Figure 7(a) shows the simulated transfer characteristic of the OTA of Fig. 2 in which I_a sweeps from 10 µA to 200 µA and I_{ss} is kept constant as 300 µA. The plots of the output current versus the differential input voltage ($V_1 - V_2$) show that by changing the DC bias current of I_a, the OTA can linearly convert the input voltage in the range of −1 V to 1 V into output current with nonlinearity less than 1%. Figure 7(b) proves the high linearity of the OTA circuit where the constant value of trans-conductances are clearly shown.

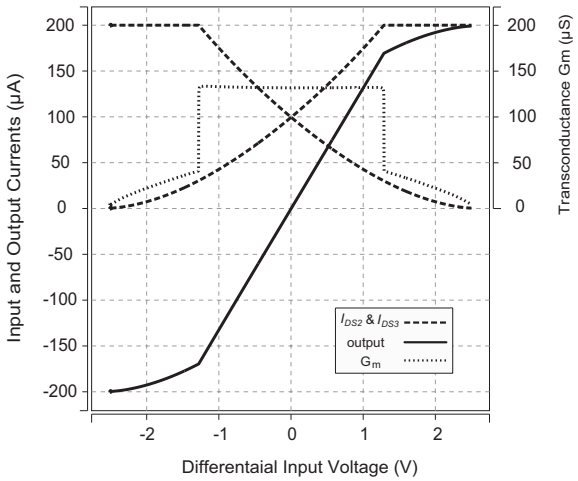


Fig. 6. Input and output currents along the trans-conductance characteristic of OTA for a typical value of parameters.

Transistor name	W/L (µm/µm)
M_1, M_2, M_3, M_4	20/0.18
M_5, M_6	5/0.18
M_7, M_8, M_9	3/0.18
M_{10}, M_{11}	8/0.18
M_{12}, M_{13}, M_{14}	7/0.18
M_{15}, M_{16}, M_{17}, M_{18}	10/0.18
M_{19}, M_{20}, M_{21}, M_{22}, M_{23}, M_{24}, M_{25}, M_{26}	2/0.18
M_{27}, M_{28}, M_{29}, M_{30}, M_{31}, M_{32}, M_{33}, M_{34}, M_{35}, M_{36}	6/0.18
M_{s1}, M_{s2}, M_{s3}, M_{s4}	4/1.8

Tab. 1. Transistors aspect ratio for LTOTA circuit.

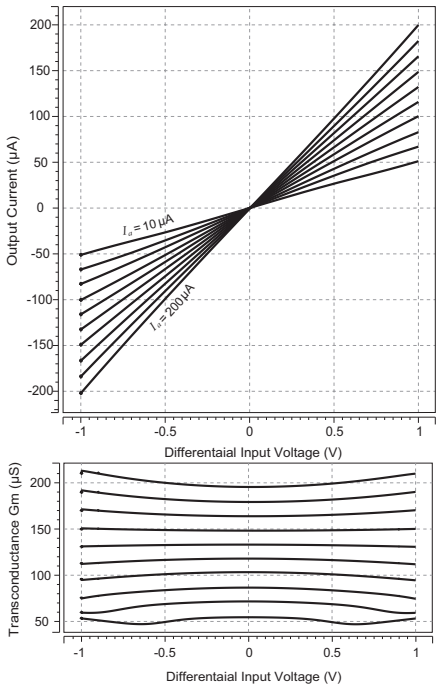


Fig. 7. (a) The output currents of OTA when I_a sweeps from 10 μA to 200 μA. (b) Trans-conductance characteristic.

The plot of the relation between the trans-conductance gain and the bias current of I_a in the circuits of Fig. 2 and 4 are simultaneously measured by fixing V_{in} = 100 mV and changing I_a from 0 to 100 μA where the simulated conversion error found to be 1.3%. The simulation results are shown in Fig. 8 in which for the circuit of Fig. 2 since $G_m = 4\sqrt{0.5\mu_0 C_{ox}(W/L)_{2,3} I_a}$, so the trans-conductance changes with the square-root proportion of I_a, while for the LTOTA circuit because $G_m = 4I_a\sqrt{K/I_b}$, therefore G_m linearly varies by changing the bias current of I_a.

In order to demonstrate the feasibility of the designed OTA and LTOTA, they are employed in the structure of Fig. 1 for realization of some functional circuits. Replacing LTOTA in the structure leads to implement a multiplier/divider circuit. Since the bias current has a linear relation with G_m we have:

$$I_{out} = \frac{G_{m2}}{G_{m1}} I_{in} = \frac{I_2}{I_1} I_{in} . \tag{14}$$

Considering I_{in} and I_2 as the input currents and I_1 as the normalized current (I_{norm}), so the multiplier function is achieved. Also, supposing I_2 and I_1 as the input currents namely I_{num} and I_{den} respectively and I_{in} as the normalized current, the output current will be proportional to I_{num}/I_{den}. Thus the structure performs as a divider circuit.

Figure 9 shows how the structure works as a multiplier circuit. The figure depicts DC transfer characteristic of the analog multiplier, where the output current swings between –250 μA to +250 μA and the normalized current is set to 125 μA. The simulation result of the structure when it employs as a divider circuit is depicted in Fig. 10. The characteristic between I_{out} and denominator current (I_{den})

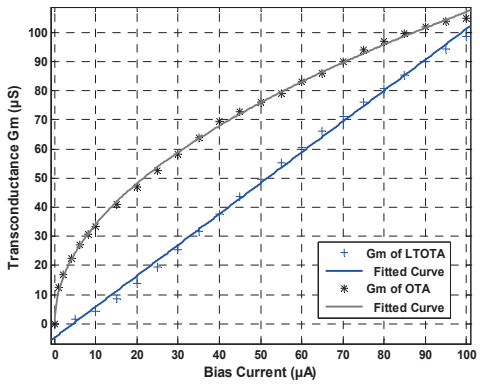


Fig. 8. Relation between the trans-conductance gain and the bias current in OTA and LTOTA circuits.

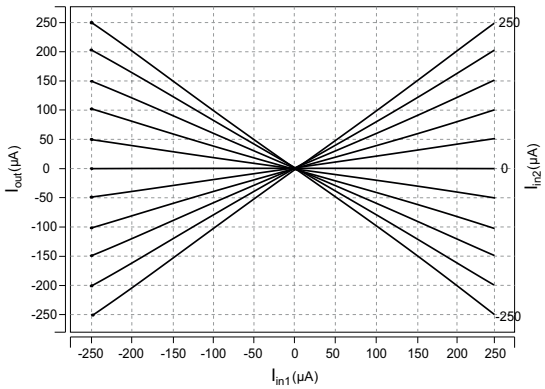


Fig. 9. Simulation result for DC transfer characteristic in the multiplier circuit.

for swept currents of numerator (I_{num}) between +125 μA and –125 μA with 50 μA per step is plotted while I_{norm} is set to 125 μA.

$$I_{out} = \frac{I_{num}}{I_{den}} I_{norm} . \tag{15}$$

In the case that I_{in} and I_2 are equal and I_1 being considered as a normalized current, a squaring function will be realized. In this case, the output current is given by:

$$I_{out} = \frac{I_{in}^{\,2}}{I_{norm}} . \tag{16}$$

By applying a triangle waveform with the frequency of 100 kHz to the input, the squaring function as well as the error value are appeared at the output (Fig. 11). It can be clearly seen that the simulated result is in a close agreement with the expected output, and the maximum error is 173 nA.

Let us consider the structure of Fig. 1. Replacing the OTA in this structure, one can find the output current as:

$$I_{out} = \sqrt{\frac{I_2}{I_1}} I_{in} . \tag{17}$$

In the case that $I_1 = I_{in}$, we have:

$$I_{out} = \sqrt{I_1 I_2} . \tag{18}$$

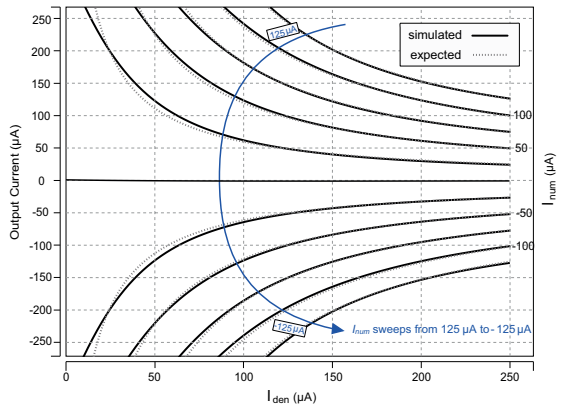


Fig. 10. DC transfer characteristic of the divider circuit.

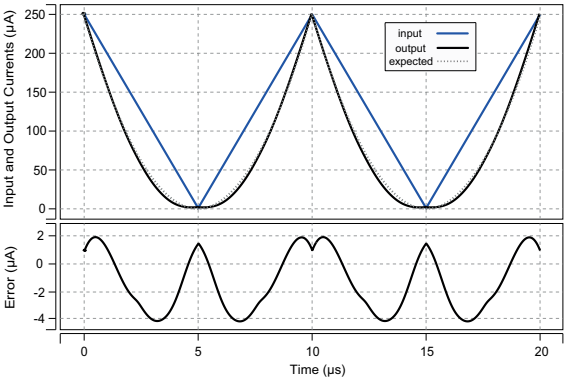


Fig. 11. Transient response of the squaring circuit and its error.

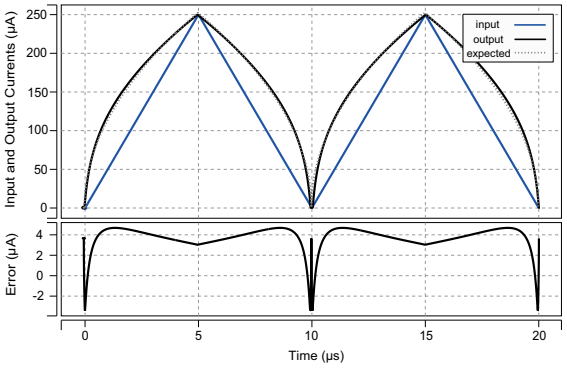


Fig. 12. Simulated transient response of square-rooting circuit and its error.

Considering I_1 as the input current, by applying $I_2 =$ 125 μA as a normalize current the square-rooter function is implemented. To prove the efficiency of the circuit, a triangle waveform similar to the squaring circuit is applied; then the output current is achieved as shown in Fig. 12.

In order to examine the effect of temperature variation on the circuit, threshold voltage variation in the presence of temperature which is the most important parameter for this issue is considered which can be derived as [33]:

$$\frac{\partial V_{\mathrm{T}}}{\partial T} = \frac{\partial \phi_{\mathrm{ms}}}{\partial T} + 2\frac{\partial \phi_{\mathrm{F}}}{\partial T} + \frac{\gamma}{\sqrt{2\phi_{\mathrm{F}}}}\frac{\partial \phi_{\mathrm{F}}}{\partial T} \qquad (19)$$

where ϕ_{ms} is the gate-substrate contact potential, γ is a body effect constant and ϕ_{F} is the Fermi energy.

Considering NMOS and PMOS current mirrors in the circuit (M_7-M_9 and M_{12}-M_{36}), because they work on the principle that identical transistors with equal gate-to-source and drain-to-source voltages carry equal drain currents and since these voltages of corresponding transistors are equal in all conditions, any variations in the threshold voltage are automatically compensated. Therefore, probable temperature variations do not affect the performance of the current mirrors. For the complete circuit and also rest of the transistors, the simulations are carried out based on the conditions of Fig. 6 in different temperatures for transconductances, and relative errors are shown in Fig. 13(a) where the maximum error occurred at –40 °C with 0.63%.

Moreover, the body effect and channel length modulation affect the threshold voltage of the transistors [33]. Considering the mismatch for equality of threshold voltages in pair transistors of M_1 and M_3 and also M_2 and M_4 and subsequently rewriting (5) and (6) we have:

$$I'_{\mathrm{DS2}} = K(V_1 - V_2 + \sqrt{\frac{I_{\mathrm{a}}}{K}} + V_{\mathrm{TH4}} - V_{\mathrm{TH2}})^2, \qquad (20)$$

$$I'_{\mathrm{DS3}} = K(V_2 - V_1 + \sqrt{\frac{I_{\mathrm{a}}}{K}} + V_{\mathrm{TH1}} - V_{\mathrm{TH3}})^2. \qquad (21)$$

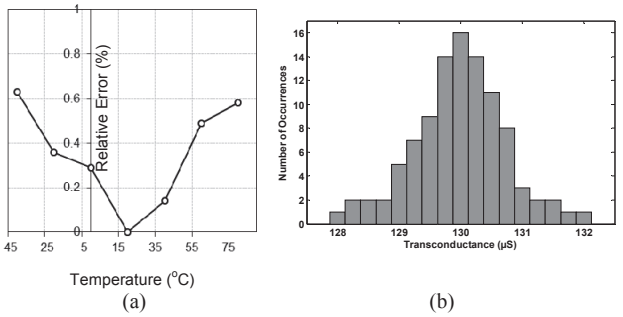
Supposing $V_{\mathrm{TH1}} - V_{\mathrm{TH3}} = \Delta V_{\mathrm{T1}}$ and $V_{\mathrm{TH4}} - V_{\mathrm{TH2}} = \Delta V_{\mathrm{T2}}$, ignoring the terms of $\Delta V_{\mathrm{T1}}{}^2$ and $\Delta V_{\mathrm{T2}}{}^2$ (since ΔV_{T1}, $\Delta V_{\mathrm{T2}} << 1$), the output current can be derived as:

$$I'_{\mathrm{o}} = K\left[(4\sqrt{\frac{I_{\mathrm{a}}}{K}} + 2\Delta V_{\mathrm{T1}} + 2\Delta V_{\mathrm{T2}})(V_1 - V_2) + 2\sqrt{\frac{I_{\mathrm{a}}}{K}}(\Delta V_{\mathrm{T2}} - \Delta V_{\mathrm{T1}})\right]. \qquad (22)$$

From (22), the mismatch values are subtracted in the second term ($\Delta V_{\mathrm{T1}} - \Delta V_{\mathrm{T2}}$), and consequently they cancel each other or minimize the error quantity. Considering the first term of the equation, the mismatch leads to a small DC offset in the output current which can be regarded as an error in the bias current of I_{a} or a DC compensated current at the output. In order to show the effects of these non-idealities, Monte Carlo analysis is carried out by applying ±5% Gaussian distribution at $\pm 3\sigma$ level in the variation of threshold voltage and the result is shown in Fig. 13(b).

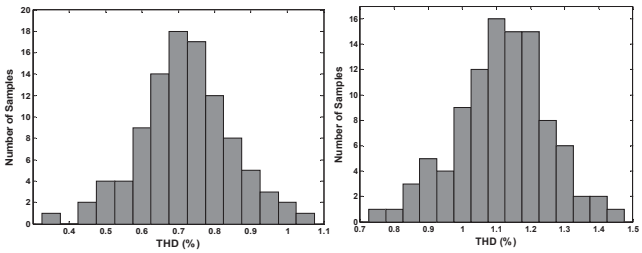
The Monte Carlo analysis for total harmonic distortion (THD) is shown in Fig. 14. The same conditions and distribution of simulations in Fig. 13 are applied for both of OTA and LTOTA circuits. The results show that most of the samples occur in the ranges of 0.6% to 0.8% and 1.0% to 1.2% for OTA and LTOTA circuits, respectively.

Distortion analysis of the OTA circuit is carried out for different input amplitudes as well as signal frequency. The amplitude dependency of HD3 and IM3 are plotted in Fig. 15(a). In the worst case, HD3 and IM3 components are –68 dB and –67 dB for 2 $V_{\mathrm{p\text{-}p}}$ differential input voltage at 10 MHz signal frequency. Variation of distortion components with frequency are also simulated and plotted in Fig. 15(b).



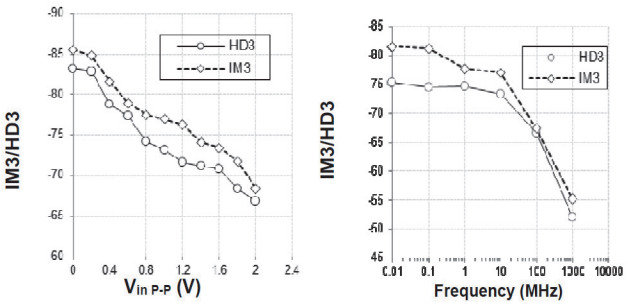
(a) (b)

Fig. 13. a) Relative error of the circuit vs. different temperatures. b) Transconductance variations from Monte Carlo simulations for threshold voltage.



(a) (b)

Fig. 14. Monte Carlo simulation for THD of (a) OTA circuit and (b) LTOTA circuit for 2 $V_{p\text{-}p}$ 1 MHz sine wave.



(a) (b)

Fig. 15. IM3 and HD3 vs. a) peak to peak input voltage at 10 MHz, b) with 2 $V_{p\text{-}p}$ input differential voltage.

	[12]	[28]	[29]	[30]	This Work
Functions	MLTP SQ SQRT	MLTP DVR	MLTP SQ	MLTP	MLTP[a] SQ[b] SQRT[c] DVR[d]
Power dissipation (mW)	0.31	20	0.588	3.5	0.66
Relative error (%)	4	12	1.6	1	2.2
-3 dB Bandwidth (MHz)	200	155	3960	120	670
THD (%)	3.1	0.25	NA	NA	1.2
Supply voltage (V)	3.3	±10	±1	±5	1.8
Input Range	±0.1 V	±1 mA	±0.1 V	±200 µA	±250 µA
Technology (µm)	0.25	0.5	0.18	2	0.18

a: Multiplier, b: Squaring, c: Square-rooter, d: Divider

Tab. 2. Comparison and performance summery of the circuit.

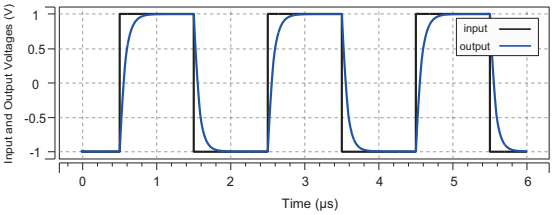


Fig. 16. Step response of the OTA for slew rate simulation.

A 2 $V_{p\text{-}p}$ step waveform is applied to unity-gain closed loop OTA whose response shown in Fig. 16. I_{ss} and I_a are set to typical values of 400 µA and 150 µA respectively, and the output load is a capacitance with 10 pF capacity.

Measuring the slope of output response gives both positive and negative slew rate as 5.7 V/µs. The comparison of the proposed circuit with previous works is shown in Tab. 2.

4. Conclusion

The major intention of this paper was to present a new method to implement computational circuits using linearly tunable CMOS OTA circuit. The proposed method enjoyed these attractive features: 1. Use of CMOS transistors, compatible with the current digital signal processing CMOS technology; 2. New tunable OTA proposed which could be linearly tuned by a bias current, therefore could be used as a bipolar OTA; 3. Could realize several linear and nonlinear functions with high precision performance; 4. The bipolar based OTA configurations could be easily replaced by the CMOS LTOTA; 5. Current-mode realization provided simple and intuitive configuration.

It should be pointed out that the main objective of the paper was that multiplier, divider, squarer and square-rooter functions could be simultaneously available using two designed OTA. Although each function could be separately found in the literature, without the new proposed OTA, they cannot be realized by one circuitry.

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About the Author ...

Ali NADERI SAATLO was born in Urmia, Iran, in 1982. He received his B.Sc. degree in Communication Engineering from Urmia Azad University, in 2005, the M.Sc. degree in Electrical Engineering from Urmia University, Urmia, Iran in 2008, and the Ph.D in Electronics Engineering from Istanbul Technical University, Istanbul, Turkey in 2014. Since 2011, he has been a faculty member of the Electrical Engineering Dept., Urmia Azad University. His research interests are analog and digital integrated circuit design for fuzzy applications, fuzzy sets and systems, high performance analog circuits, and digital signal processing.