A Low-Dropout Voltage Regulator with a Fractional-Order Control

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Abstract. *This paper presents a 5 V / 50 mA low-dropout voltage regulator (LDO). The LDO uses a fractional-order control for its regulation loop to achieve a high DC gain (for a tight DC regulation) while avoiding (for a good stability) a high gain at high frequency. No compensation zeros are needed. The unity gain frequency of the regulation loop also changes adaptively with the output current to maintain it below the frequency of non-dominant poles. The LDO is stable with any external capacitance larger than 50 nF, and is expected to operate in a harsh automotive environment, with junction temperature ranging from –40°C to 170°C and with supply voltage from 7 V to 36 V. The operation of the LDO has been verified by realizing it in the 350 nm I3T50 ON Semiconductor technology.*

Keywords

Fractional-order control, error amplifier, RC ladder, low-dropout regulator, frequency compensation

1. Introduction

This section presents classical LDO concepts and their trade-offs of DC regulation error and regulation loop stability, and how the fractional-order control solves them.

1.1 Classical LDO Concepts

A low-dropout voltage regulator is a linear voltage regulator which can maintain a nearly constant output voltage even if the supply (input) voltage is very close to the output voltage. LDOs are the most popular class of linear voltage regulators [1], [2], [3], [4], [5], [6].

The principal LDO topology is shown in Fig. 1. The transconductor g_{m1} monitors the output (the pin OUT) voltage via the resistive voltage divider R_3-R_4 and controls the gate of the end stage transistor M_2 to set the current delivered to the output from the input (the pin IN) in order to maintain the output voltage at the desired value (according to the reference voltage at the REF pin). The resulting regulation loop is negative, with two poles: the internal pole (formed by the RC circuit R_1-C_1) and the
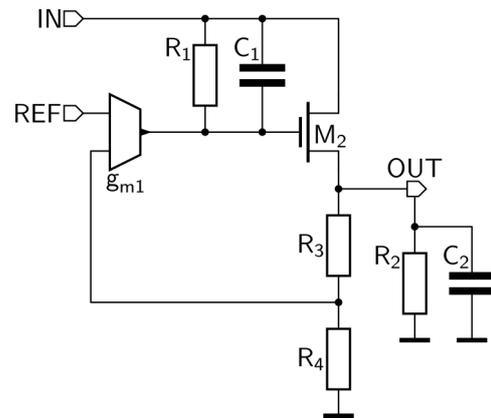

Fig. 1. Principal LDO topology.

external pole (formed by the load capacitance C_2 with the parallel combination of the load resistance R_2, the resistance of the voltage divider R_3-R_4 and the dynamic output resistance of the transistor M_2).

In general, there are three LDO concepts, depending on which poles are dominant and which are non-dominant. Dominant poles set the UGF (unity gain frequency) of the regulation loop, while the non-dominant poles do so in a minor way only and their frequency is preferably above the UGF.

The first concept has both the internal and the external pole dominant – the open-loop gain of the regulation loop attains the slope of –40 dB/dec. Acceptable stability of the regulation loop requires a compensation zero (with a frequency below or near the UGF) to reduce the slope. An advantage is that the internal dominant pole implies a (nearly) integrative regulation, resulting in a very low DC regulation error.

The second concept makes the internal pole to be non-dominant and the external pole dominant. The load capacitance is required to be above certain value; its ESR and ESL (equivalent series resistance and inductance) are usually limited to prevent the resultant parasitic zeros from affecting the UGF. An advantage is that the maximum load capacitance is unlimited and its ESR can be zero (for an improved response to load current transients). A proportional regulation and a non-zero DC regulation error are implied by the internal pole being non-dominant.

The third concept makes the internal pole dominant and the external pole non-dominant. Making the external pole non-dominant entails pushing it to a high frequency, (this concept is suitable for the end stage transistor M_2 being a voltage follower) and possibly placing an upper bound on the load capacitance C_2. An advantage is a very low DC regulation error.

The first concept enjoys a large popularity because of a low DC regulation error, with many methods for creating the compensation zero described in the literature. In Fig. 4 of [1], the zero is formed by the current-controlled current source. In Fig. 1 of [2], the zero is created by the ESR of the external capacitor and by the capacitor C_{f2}. In Fig. 5 of [3], the zero results from a parallel signal path formed by the current amplifier and the capacitor C_f; in [4], the parallel signal path results from the connection of the CFA to the output of the LDO; in [5], the parallel signal path passes through the capacitor C_c. In Fig. 5 of [6], the compensation zero of the output buffer is created by the ESR of the internal on-chip output capacitor.

This paper focuses on the LDO topology in Fig. 2, which is suitable for the first and the second concept. The topology is composed of the end stage current mirror M_1-M_2, driven by the controller, which consists of the voltage divider R_1-R_2 and the transconductor (an error amplifier with the transconductance $G_e(s)$).

The regulation loop should have a high DC gain for a tight DC regulation and its UGF should not be too high in order to prevent parasitic poles (or possibly zeros) from affecting its stability. One parasitic pole, p_m, is formed by the transconductance of the transistor M_1 with the gate capacitance C_{pm} of the end stage mirror. A parasitic zero can be the zero resulting from the ESR (R_{ESRext}) of the external capacitor C_{ext}. The external dominant pole p_{out}, created at the output (OUT) by the external capacitance C_{ext}, increases the slope of the open-loop gain of the regulation loop at most by –20 dB/dec.

It should be noted that the term "output current" $I_{OUT}(s)$ implies only the current drawn from the output pin (OUT), while "load current" $I_{load}(s)$ also includes the current sourced by the external capacitor C_{ext}.

There are several approaches for choosing the transfer function $G_c(s)$ of the controller.

The first approach implements the first LDO concept, making the controller a first-order integrator. An advantage is a very low DC regulation error. The open-loop gain of the regulation loop (VFB – "voltage feedback") reaches the slope of –40 dB/dec., as shown by the characteristic (a) in Fig. 3. A disadvantage is that stability of the regulation loop requires a compensation zero z_{comp} to reduce the slope around its UGF.

The second approach implements the second LDO concept by making the controller a proportional system (with a frequency-independent transconductance at frequencies below and near the UGF). The regulation loop has
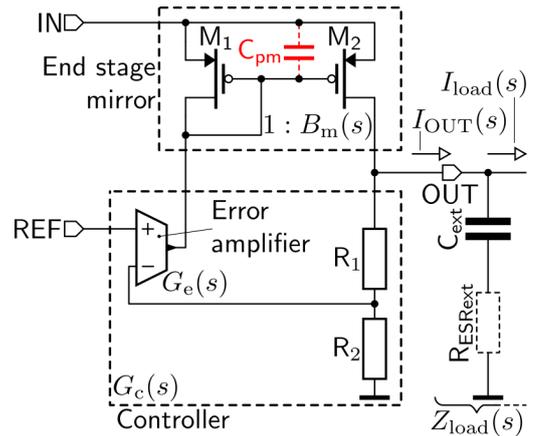

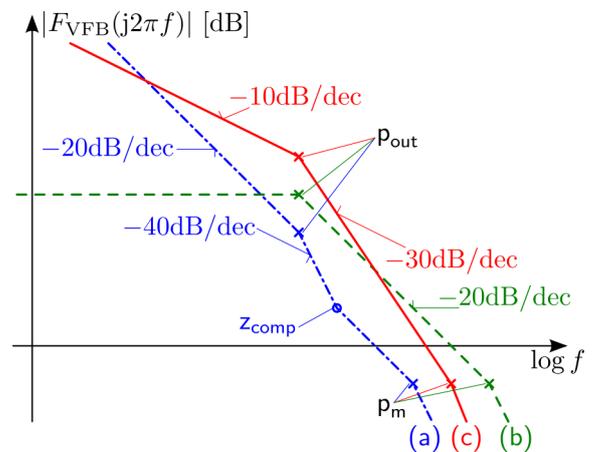**Fig. 2.** LDO topology with an external dominant pole.

Fig. 3. Open-loop voltage gain of the regulation loop of an LDO with an external dominant pole: (a) – internal pole is dominant, (b) – internal pole is non-dominant, (c) – fractional-order control.

a single dominant pole (p_{out}); other poles (e.g. p_m) are non-dominant and should be, as shown by the characteristic (b) in Fig. 3, above the UGF to prevent them from degrading the stability of the regulation loop. A disadvantage is that a tight DC regulation implies a high UGF, making a good stability difficult to achieve.

With the approaches above, a low DC regulation error entails a high UGF or a compensation zero.

1.2 Proposed LDO Approach

We propose a third approach to choosing the transfer function of the controller of the LDO topology in Fig. 2. This approach is between the first and the second one.

The controller in the first approach can be seen as a "zero-order" voltage-to-current integrator with a transfer function of (where G_{C0} is its transconductance)

$$G_C(s) = G_{C0}s^0 \qquad (1)$$

while in the second approach it is a first-order integrator with a transfer function of (G_{CI} is the integrator gain)

$$G_C(s) = G_{CI}s^{-1}. \qquad (2)$$

We propose the controller being an integrator with the order of 0.5 (a so-called fractional order), as given by the characteristic (c) in Fig. 3 and by the transfer function

$$G_C(s) = G_{CF}s^{-0.5} \tag{3}$$

where G_{CF} is the integrator gain. Such a controller has a gain with the slope of –10 dB/dec. and the phase of –45°. With the external capacitance contributing the slope of at most –20 dB/dec., the magnitude of the gain of the regulation loop has a slope of at most –30 dB/dec. The largest phase shift is –135° (there are no right-hand zeros), leaving at least 45° as a phase margin.

Advantages of this approach are high DC gain (a tight DC voltage regulation) and not too high UGF (ensuring a good stability of the regulation loop). Another advantage is that no compensation zero is needed. The external capacitance has a specified minimum, but the maximum is unlimited (while its ESR and ESL are limited).

The pole p_m of the end stage mirror should have a frequency above the UGF to prevent it from degrading the phase margin of the regulation loop.

The response of an LDO with a fractional-order control to a step change of the load current is given by the Mittag-Leffler function [7] and can be described as an exponential decay with an elongated settling (as if its time constant increased with time). A general introduction to a fractional-order control can be found in [7] or [8].

2. Fractional-Order Impedance

This section describes how to approximate a fractional-order impedance, which defines the frequency characteristic of the error amplifier of the controller.

An impedance $Z(s) = Z_F s^{-\alpha}$ with a positive gain Z_F and a fractional order α between 0 and 1 can be approximated with an infinite RC ladder shown in Fig. 4 [9], [10].

The impedance of the infinite RC ladder is [9]

$$Z_{frac}(s) = \frac{1}{\displaystyle\sum_{k=-\infty}^{+\infty}\frac{1}{Z_k(s)}} = \frac{1}{\displaystyle\sum_{k=-\infty}^{+\infty}\frac{1}{R_k + \dfrac{1}{sC_k}}} \tag{4}$$

where $Z_k(s)$ is the impedance of the k-th series RC circuit. The resistances R_k and capacitances C_k form separate decreasing geometric series [9], [10]

$$\begin{aligned} R_k &= q_R^k R_0, \quad 0 < q_R < 1, \\ C_k &= q_C^k C_0, \quad 0 < q_C < 1. \end{aligned} \tag{5}$$

The operation of the infinite RC ladder is explained by Fig. 5. Assume the common ratios q_R and q_C are identical ($q_R = q_C = q$); the cutoff frequency of the k-th series RC circuit is proportional to $(1/q^k)^2$, while its impedance at its cutoff frequency is proportional to $1/q^k$ [9]. As a result, the
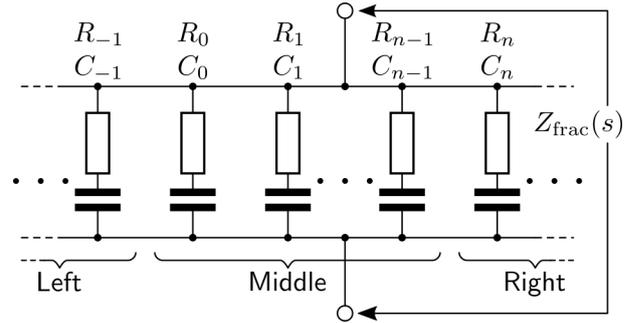

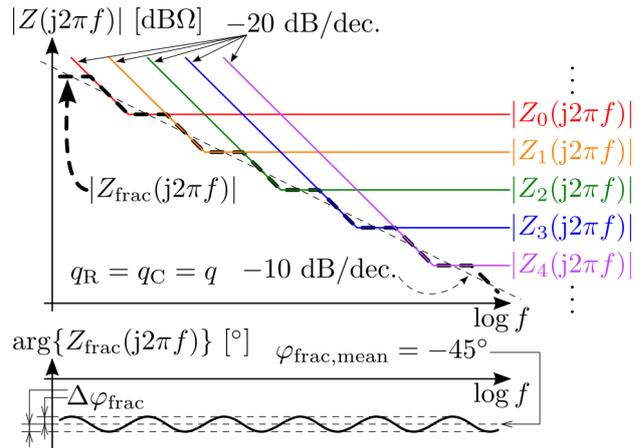**Fig. 4.** Infinite RC ladder approximating a fractional-order impedance.

Fig. 5. Explanation of approximating a fractional-order impedance with the infinite RC ladder.

magnitude of the impedance $Z_{frac}(s)$ of the infinite RC ladder attains on average half the slope, i.e. –10 dB/dec.

The phase of the frequency characteristic of the impedance $Z_{frac}(s)$ oscillates with the ripple of $\Delta\varphi_{frac}$ around the phase $\varphi_{frac,mean}$ of the impedance $Z_F s^{-\alpha}$ being approximated; the similar applies to the magnitude. Choosing the common ratios q_R and q_C closer to 1 reduces the ripple. The ratio $\log(q_R)/\log(q_C)$ sets the order α of the impedance being approximated.

Only the series RC circuit whose cutoff frequency is near some frequency contributes to the fractional-order behavior at this frequency, as shown in Fig. 5 of [9].

The infinite RC ladder cannot be realized in practice, but can be divided into the following three sections. The middle section approximates the fractional-order impedance in the frequency band of interest, while the left and
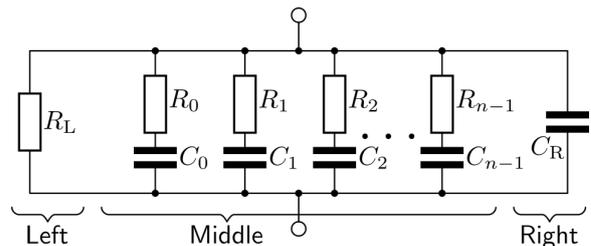

Fig. 6. Bilaterally terminated finite RC ladder approximating a fractional-order impedance.

the right sections "terminate" the RC ladder. This allows reducing the infinite RC ladder to the bilaterally terminated finite RC ladder shown in Fig. 6.

The left section is approximated by a left-terminating resistance R_L, given by evaluating a geometric series [9] (as the left section is assumed to behave mostly resistively in the frequency band of interest)

$$
\begin{aligned}
R_L &\approx \frac{1}{\displaystyle\sum_{k=-\infty}^{-1}\frac{1}{q_R^k R_0}} = \frac{1}{q_R\displaystyle\sum_{k=-\infty}^{0}\frac{1}{q_R^k R_0}} = \\
&= \frac{1}{q_R\displaystyle\sum_{k=0}^{+\infty}\frac{q_R^k}{R_0}} = R_0\left(\frac{1}{q_R}-1\right).
\end{aligned}
\tag{6}
$$

Similarly, the right section is assumed to behave mostly capacitively and is approximated by a right-terminating capacitance of [9]

$$
C_R \approx \sum_{k=n}^{+\infty}C_0 q_C^k = q_C^n\sum_{k=0}^{+\infty}C_0 q_C^k = C_0\frac{q_C^n}{1-q_C}.
\tag{7}
$$

Without the terminating resistance and capacitance, the frequency range where the bilaterally-terminated RC ladder exhibits an acceptable fractional-order behavior would be narrower [9]. The term "termination" is a loose analogy to a termination of a transmission line (to stabilize its frequency response). The bilaterally-terminated finite RC ladder achieves the frequency characteristic sketched by the characteristic (b) in Fig. 7.

Here, a left-terminated finite RC ladder from Fig. 8 is used instead of the bilaterally-terminated one. The role of the right-terminating capacitance C_R is filled by parasitic poles of the LDO, and an additional phase margin of the regulation loop is gained. Without any parasitic poles, the left-terminated RC ladder has the frequency characteristic (c) sketched in Fig. 7.

Section 5 of [9] demonstrates the RC ladder is largely insensitive to individual (mismatch) component variation; simultaneous variation (process spread) causes only scaling of its impedance without affecting the order α.
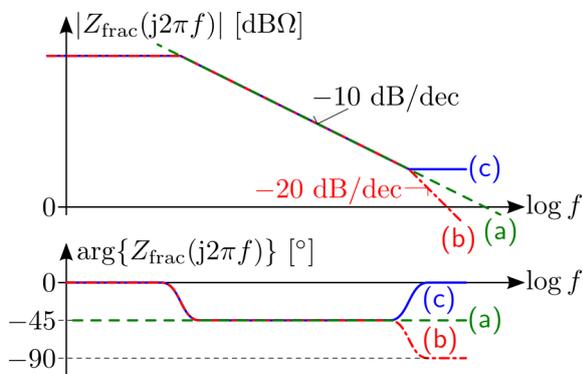

Fig. 7. Comparison of the impedances $Z_{\text{frac}}(s)$ of the described RC ladders: (a) – infinite, (b) – bilaterally-terminated, (c) – left-terminated.
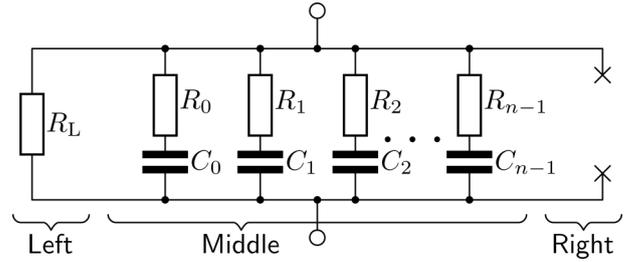

Fig. 8. Left-terminated finite RC ladder approximating a fractional-order impedance.

3. Fractional-Order Control

The fractional-order behavior of the proposed LDO resides in the error amplifier, whose schematic is in Fig. 9. The error amplifier senses the output voltage via the feedback resistive voltage divider. The difference between the actual and the target voltage manifests as the current I_{FB}, causing the action voltage V_{ACT} to be adjusted accordingly. The error amplifier behaves like a transimpedance amplifier, whose transimpedance

$$
Z_e(s) = -\frac{V_{\text{ACT}}(s)}{I_{\text{FB}}(s)}
\tag{9}
$$

approximates a fractional-order transimpedance.

The transimpedance of the error amplifier is set mostly by the RC ladder (of the left-terminated finite type), since the transconductance of the OTA (operational trans-
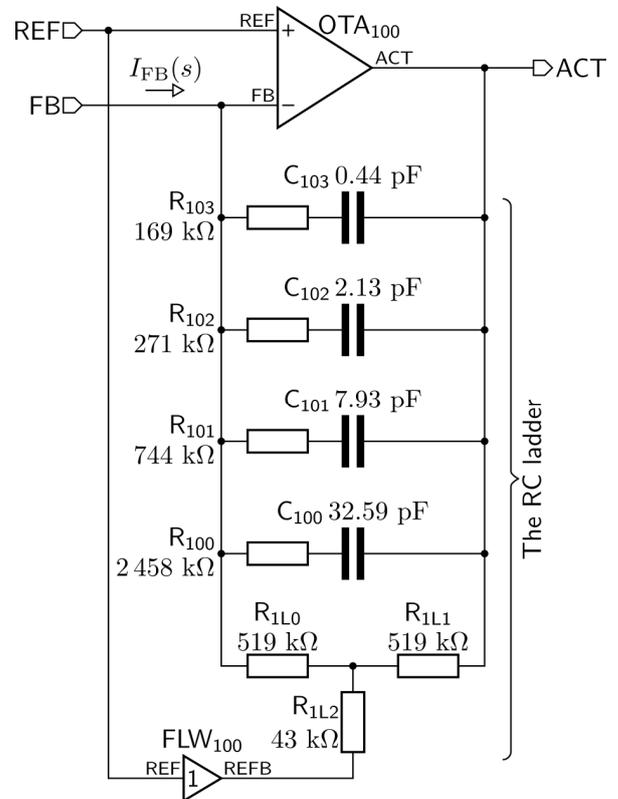

Fig. 9. Schematic of the error amplifier with a fractional order.

conductance amplifier) exceeds the admittance of the RC ladder. The exception is very high frequencies, where the parasitic poles of the OTA dominate.

The T-circuit R_{1L0}-R_{1L1}-R_{1L2} has a transconductance (from the ACT output to the FB input of the OTA) identical to an equivalent left-terminating resistance of

$$R_{10L} = R_{1L0} + R_{1L1} + \frac{R_{1L0}R_{1L1}}{R_{1L2} + R_{FLW}} \doteq 6.084 \text{ M}\Omega. \quad (10)$$

The T-circuit replaces a resistor with such a large resistance, reducing the occupied chip area. The virtual ground for the T-circuit is provided by the voltage follower FLW_{100}, which has the nominal output DC resistance R_{FLW} of 10.38 kΩ (a value that can be met even by a follower-connected single-stage amplifier).

The error amplifier has a low sensitivity to the voltage offset of the follower, since the sum of the resistances of the resistors R_{1L0} and R_{1L2} surpasses the output resistance of the voltage divider of the LDO.

For the design of the RC ladder, we have chosen its impedance $Z_{frac}(s)$ to approach the order of $\alpha = 0.5$ with the phase ripple of $\Delta\varphi_{frac} = 2.5°$ (a compromise between too long ladder and a worst-case degradation of the phase margin of the regulation loop). Using (20) from [9], the phase ripple sets the product of the common ratios of

$$q_R q_C \approx \frac{0.24}{1 + \Delta\varphi} = \frac{0.24}{1 + 2.5} \doteq 0.0686. \quad (11)$$

The product is broken into the individual components [9]

$$q_R = 10^{\alpha \log_{10}(q_R q_C)} = 10^{0.5 \log_{10}(0.0686)} \doteq 0.262, \quad (12)$$

$$q_C = \frac{q_R q_C}{q_R} = \frac{0.0686}{0.262} \doteq 0.262. \quad (13)$$

The equivalent left-terminating resistance R_{10L} is designed along with the DC transconductance G_{v0} of the voltage divider by (16) and (17), where Z_{eF} is given by a simulation of the RC ladder. Utilizing (6), the resistance R_{100} of the first series RC circuit is calculated from R_{10L} as

$$R_{100} = \frac{R_{10L}}{\frac{1}{q_R} - 1} = \frac{6.084 \cdot 10^6}{\frac{1}{0.262} - 1} \doteq 2.158 \text{ M}\Omega \quad (14)$$

while its capacitance C_{100} is chosen to occupy the same layout area as the resistance R_{100} (a combination achieving the lowest layout area, given the same cutoff frequency). The other resistances and capacitances are calculated from (5) and summarized in Tab. 1.

The actual values of the resistors and the capacitors of the RC ladder were, as Tab. 1 documents, optimized manually according to simulation results to account for their parasitic capacitances and to compensate for the effect of distant parasitic poles of the LDO.

Parameter	Value calculated from (5)	Actual value (manual optimization)
R_{10L}	6.084 MΩ	
R_{100}	2.158 MΩ	2.458 MΩ
R_{101}	0.565 MΩ	0.744 MΩ
R_{102}	0.148 MΩ	0.271 MΩ
R_{103}	0.039 MΩ	0.169 MΩ
C_{100}	32.59 pF	
C_{101}	8.53 pF	7.93 pF
C_{102}	2.23 pF	2.13 pF
C_{103}	0.59 pF	0.44 pF

Tab. 1. Typical component values of the RC ladder of the error amplifier – a comparison of the calculated values and the actual values obtained by manual optimization.

Despite having large values, the components of the RC ladder can be realized well in an analog CMOS (complemenatry MOS) technology: capacitors as a MOS structure, resistors as an unsilicided polysilicon strip.

An example of a use and a different implementation of a fractional-order control can be found in [11].

4. LDO Description

The fractional-order error amplifier has been utilized in an LDO, whose schematic is in Fig. 10. The LDO consists of the controller, whose output driving current $I_{DRV}(s)$ is amplified by the end stage mirror into the output current $I_{OUT}(s)$. In the controller itself, the driving current $I_{DRV}(s)$ is generated by the driving stage, which is controlled by the action voltage $V_{ACT}(s)$, outputted by the error amplifier, that monitors the output voltage of the LDO via the voltage divider. The error amplifier and other low-voltage blocks are supplied from the low-voltage supply, VDD (voltage V_{DD}), provided by another on-chip voltage regulator.
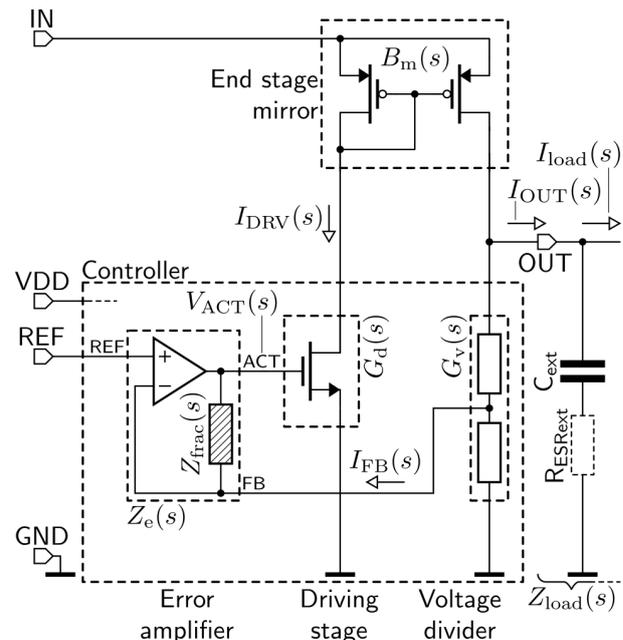

Fig. 10. Top-level schematic of the presented LDO.

The small-signal AC model of the regulation loop of the LDO is shown in Fig. 11. The magnitude frequency characteristics of the blocks of the LDO are in Fig. 12. The transimpedance $Z_e(s)$ of the error amplifier resembles the impedance of the bilaterally-terminated RC ladder described in Sec. 2.

The open-loop voltage gain of the regulation loop is

$$F_{\text{VFB}}(s) = -G_v(s) Z_e(s) G_d(s) B_m(s) Z_{\text{load}}(s). \quad (15)$$

Both the end stage mirror (current gain $B_m(s)$) and the driving stage (transconductance $G_d(s)$) have at least one parasitic pole, as shown by the small-signal AC model of the regulation loop in Fig. 11 and by Fig. 12. The parasitic poles move to lower frequencies with the decreasing output current of the LDO. The cause is a reduction of transconductances of the respective transistors due to lower drain currents, while their parasitic capacitances remain nearly the same.

To keep the frequencies of the parasitic poles above the UGF of the regulation loop in order to prevent them from reducing its phase margin, the transconductance $G_d(s)$ of the driving stage decreases automatically with the decreasing output current of the LDO. This ensures the UGF decreases as well, preserving its distance from frequencies of the parasitic poles. We call this process the adaptive UGF adjustment.

With the impedance $Z_{\text{load}}(s)$ of the load, the regulation loop has the gain $F_{\text{VFB}}(s)$ with a slope at most -30 dB/dec. above its UGF, resulting in a phase margin of at least 45°.

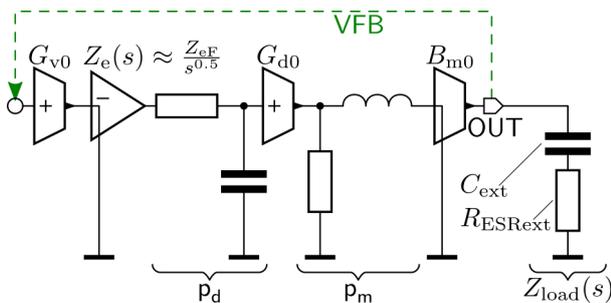Key parameters of the blocks of the LDO are summarized in Tab. 2.

Fig. 11. Small-signal AC model of the regulation (VFB) loop of the presented LDO.

Parameter		Typical value for $I_{\text{load}} = 50$ mA
Name	Symbol	
DC transconductance of the voltage divider	G_{v0}	8.918 µS
DC transimpedance of the error amplifier	Z_{e0}	$R_{10L} = 6.084$ MΩ
Gain of the transimpedance of the error amplifier	Z_{eF}	252.2 MΩ·Hz$^{1/2}$
DC transconductance of the driving stage	G_{d0}	1.635 mS
DC current gain of the end stage mirror	B_{m0}	206.5

Tab. 2. Key parameters of the blocks of the proposed LDO.
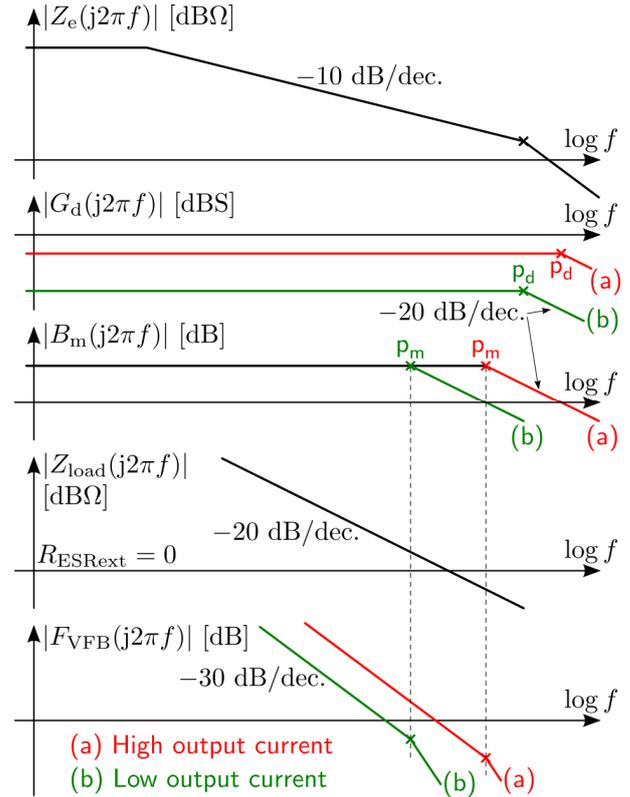

Fig. 12. Magnitude frequency characteristics of the blocks of the presented LDO.

Using the parameters in Tab. 2, the DC dynamic output resistance r_{OUT} and the UGF of the regulation loop with the external capacitance C_{ext} of 50 nF are calculated as (both are typical values for 50 mA load current)

$$r_{\text{OUT}} = \frac{1}{G_{v0} Z_{e0} G_{d0} B_{m0}} = 54.6\,\text{m}\Omega, \quad (16)$$

$$\text{UGF} \approx \frac{1}{2\pi} \sqrt[\frac{3}{2}]{\frac{G_{v0} Z_{eF} G_{d0} B_{m0}}{C_{\text{ext}}}} = 0.976\,\text{MHz}. \quad (17)$$

For comparison, the single-pole models in Fig. 11 of the driving stage and of the end stage mirror have cutoff frequencies of 125.6 MHz and 26.1 MHz, respectively.

5. Simulation Results

The operation of the presented LDO has been verified by simulations of the designed circuit in the ON Semiconductor I3T50 technology (350 nm smart power technology) across the corners listed in Tab. 3, i.e. combinations of extremes of the operating conditions and the process spreads of the components ("slow" means a low transconductance, a low gate capacitance and a high threshold voltage of MOS transistors, while "fast" means the opposite). Each simulation has a nominal run, which sets typical process parameters and operating conditions ($V_{\text{IN}} = 8$ V, $V_{\text{DD}} = 3.3$ V, $I_{\text{load}} = 50$ mA, $C_{\text{ext}} = 50$ nF, zero ESR and ESL of the external capacitor and the temperature of 27°C). In the plots, the nominal run uses a thick solid black

Swept parameter	Freq. char. of the reg. loop	DC load characteristic	Step response
NMOS, capacitor	slow, fast	slow, fast	slow, fast
PMOS	slow, fast	slow, fast	slow, fast
Resistor	min, max	min, max	min, max
Input voltage V_{IN}	7 V, 36 V	7 V, 36 V	7 V, 36 V
Low-voltage supply V_{DD}	3.0 V	3.0 V, 3.6 V	3.0 V
Load current I_{load}	0, 1 mA, 50 mA	-	-
Ext. capacitance C_{ext}	50 nF	-	50 nF
(ESR of C_{ext}, ESL of C_{ext})	(0 Ω, 0 nH), (0.7 Ω, 5 nH)	-	(0 Ω, 0 nH), (0.7 Ω, 5 nH)
Temperature	−50°C, 200°C	−50°C, 200°C	−50°C, 200°C

Tab. 3. Corners (combinations of operating conditions and process spreads) for simulations of the presented LDO.

line, the low-temperature runs use thin solid lines of cold (blue) colors and the high-temperature runs use thin dashed lines of warm (red, orange and yellow) colors.

The open-loop voltage gain, plotted in Fig. 13, of the regulation (VFB) loop of the LDO demonstrates the fractional-order behavior, since there is a wide region with the phase of 45°. At low frequencies, the phase increases due to the left termination of the RC ladder and due to the external pole having a little effect there. At high frequencies, the phase increases (due to the ESR and the ESL) or decreases (due to parasitic poles). The UGF varies highly due to the adaptive UGF adjustment.
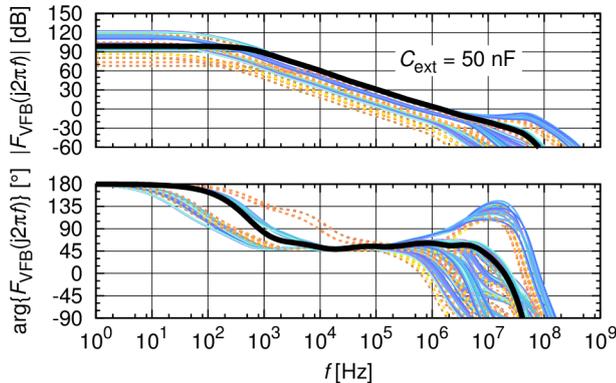

Fig. 13. Simulated open-loop voltage gain of the regulation (VFB) loop of the presented LDO.
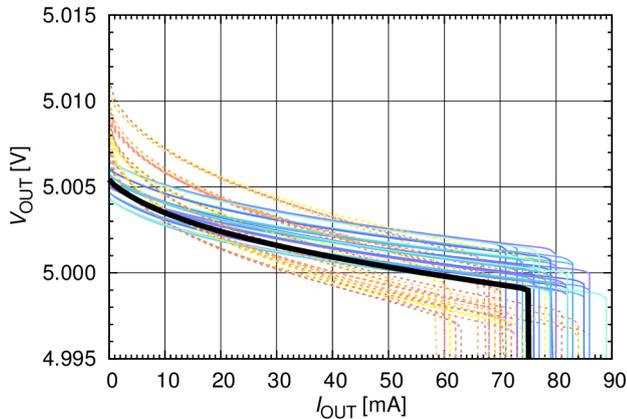

Fig. 14. Simulated DC load characteristic of the presented LDO.

The DC load characteristic, plotted in Fig. 14, shows a very tight DC regulation (a low dynamic output resistance) of the LDO – a benefit of the error amplifier being a (fractional-order) integrator. The characteristic is convex (having a larger dynamic output resistance at low output currents) because of the adaptive UGF adjustment.

If component mismatch is included (by a mismatch Monte-Carlo analysis or a sensitivity analysis), the output voltage ranges from 4.936 V to 5.073 V (6 sigma interval) across zero to full (50 mA) load current.

The response of the LDO to the step increase of the load current from 0 mA to 50 mA is plotted in Fig. 15; the response to the step decrease of the load current from 50 mA to 0 mA in Fig. 16 (the triangular portion is caused by the external capacitor being first charged by the overshoot of the output voltage and then gradually discharged by the load current; the LDO cannot sink any considerable current from its output). The settling part of the responses (excluding the triangular portion) is nearly monotonous, suggesting a sufficient phase margin of the regulation loop, and the shapes agree with the Mittag-Leffler function (i.e. their initially fast decay is more prolonged than it would be for an exponential function).
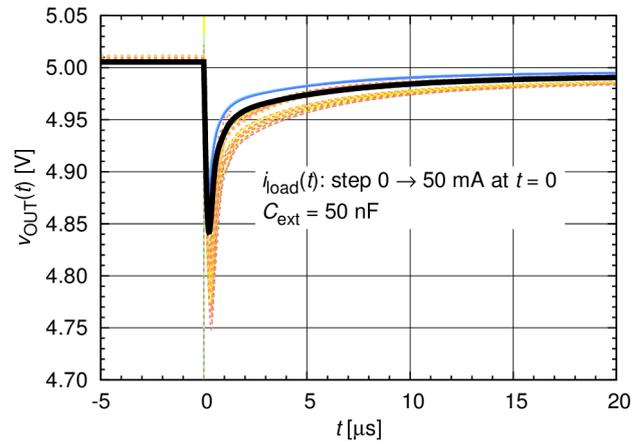

Fig. 15. Simulated transient response of the presented LDO to the step increase of the load current.
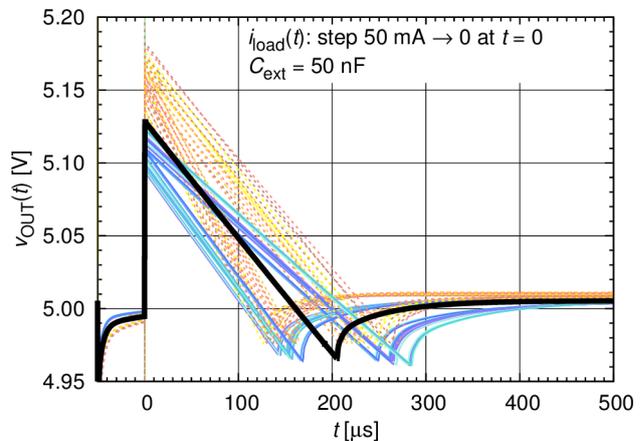

Fig. 16. Simulated transient response of the presented LDO to the step decrease of the load current.

6. Measurements

The presented LDO has been realized as a functional block in a complex mixed-signal application-specific integrated circuit. The layout of the LDO is shown in Fig. 17.

The measurements have been performed at a room temperature on a sample whose process parameters are close to being typical. The input voltage V_{IN} is set to 7 V to reduce self-heating, but to still guarantee a correct operation of the LDO. The output voltage (V_{OUT}, v_{OUT}) was measured directly on the bond pads (GND, OUT) to eliminate a voltage drop on leads and bond wires.

The measured DC load characteristic of the LDO is shown in Fig. 18. The measured characteristic has a larger
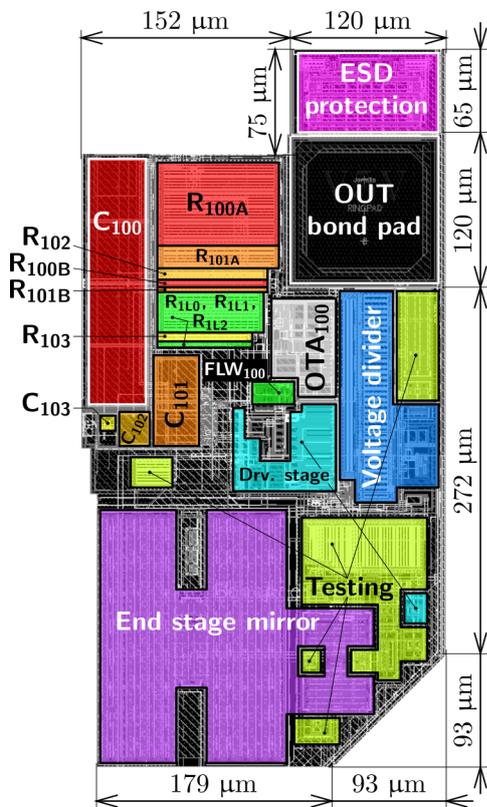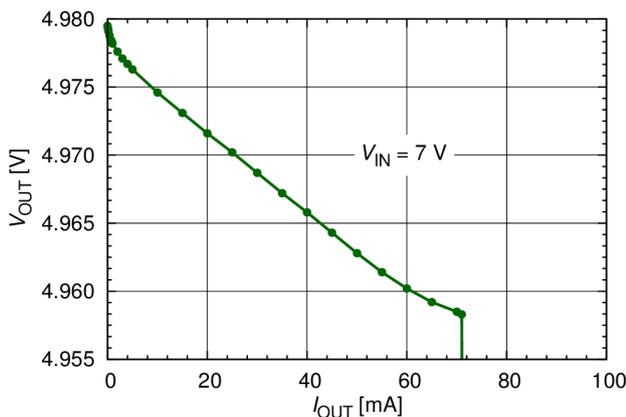
Fig. 17. Layout of the presented LDO.

Fig. 18. Measured DC load characteristic of the presented LDO.
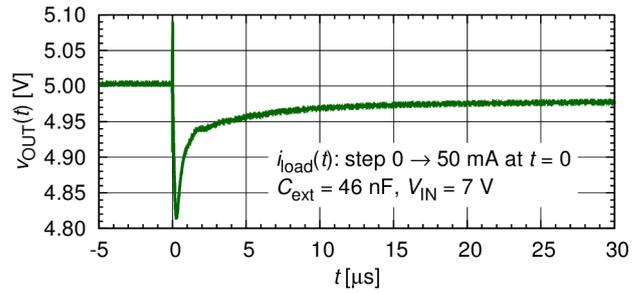
Fig. 19. Measured transient response of the presented LDO to the step increase of the load current.
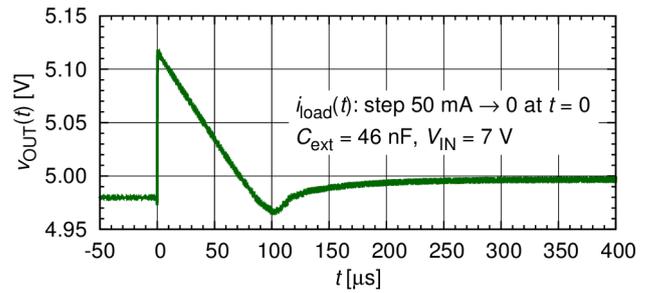
Fig. 20. Measured transient response of the presented LDO to the step decrease of the load current.

slope than the simulated one in Fig. 14. This is caused by an internal ground shift, whose effect is not eliminated even by a measurement on bond pads and which is not accounted for in the simulation. The measured dynamic output resistance is around 300 mΩ.

The response to the step increase of the load current from 0 mA to 50 mA, captured in Fig. 19, shows a voltage drop of less than 200 mV, which settles mostly in around 10 μs. The step decrease from 50 mA to 0 mA causes a peak lower than 150 mV, captured in Fig. 20, nearly settling in 200 μs.

All the measurements agree with the simulations.

7. Conclusions

A low-dropout voltage regulator using a fractional-order control was presented. Accurate voltage regulation with a low dynamic output resistance of approximately 300 mΩ was achieved while maintaining a good stability of the regulation loop, without requiring compensation zeros. An arbitrary large external capacitor can be used without limitation for its minimum required ESR. The LDO is intended to provide a precise supply voltage for analog circuits in a harsh automotive environment.

A comparison of the presented LDO to other selected LDOs is shown in Tab. 4.

The fact the error amplifier is an active circuit enabled the use of the T-circuit R_{1L0}-R_{1L1}-R_{1L2} in Fig. 9 to avoid a left-terminating resistor with a very large resistance. Future work can focus on an advanced use of active elements in approximating a fractional-order impedance in order to further reduce the layout area occupied by the RC ladder of the error amplifier.

LDO	Concept (Sec. 1)	Output voltage [V]	Output current [mA]	Max. input voltage [V]	Tech-nology [μm]	Layout area [mm²]
[1]	1 (ZE)	2.8	100	3.3	0.50	?
[2]	1 (ZI)	1.3	100	4.5	0.60	0.30
[3]	3 (ZI)	2.8	50	3.0	0.35	0.12
[4]	1 (ZE)	2.0	50	2.5	0.25	0.25
[5]	1 (ZE)	1.8	200	5.5	0.35	0.264
[6]	1 (ZE)	0.9	100	1.2	0.09	0.008
This	F (E)	5.0	50	36	0.35	0.119

Tab. 4. Comparison of the presented LDO with the selected other LDOs: "F" – fractional-order control, "I" – internal output capacitor, "E" – external output capacitor, "Z" – compensation zero.

Acknowledgements

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