Novel CMOS Bulk-driven Charge Pump for Ultra Low Input Voltage

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Abstract. *In this paper, a novel bulk-driven cross-coupled charge pump designed in standard 90 nm CMOS technology is presented. The proposed charge pump is based on a dynamic threshold voltage inverter and is suitable for integrated ultra-low voltage converters. Due to a latchup risk, bulk-driven charge pumps can safely be used only in low-voltage applications. For the input voltage below 200 mV and output current of 1 μA, the proposed bulk-driven topology can achieve about 10 % higher efficiency than the conventional gate-driven cross-coupled charge pump. Therefore, it can be effectively used in DC-DC converters, which are the basic building blocks of on-chip energy harvesting systems with ultra-low supply voltage.*

Keywords

Charge pump, CMOS, bulk-driven, low-power, energy harvesting

1. Introduction

Recent trends in the development of integrated systems include the energy savings, total size reduction and the reliability enhancement. The most effective way towards reduction of energy consumption is focusing on this parameter right at the design phase of integrated electronic system development. However, low power design might not be sufficient for some applications. The other option is supplying the electronic system from alternative energy sources [1], [2]. Nevertheless, renewable energy sources require voltage power converters (DC/DC converters or AC/DC converters). The role of a power converter is also the stabilization of variable input voltage or generation of the required output voltage value. Usually, linear and switching regulators are used for the voltage stabilization. Additionally, some of switching regulators can also convert the input voltage to a higher output voltage value. One type of such switching regulators are so-called Charge Pumps (CP), which are based on switched capacitors technique.

CP are widely used to generate voltages higher the nominal supply range, e.g. in DC-DC converters and DC voltage regulators or in EEPROMs, Flash memories to generate high voltages for programming and erasing the floating gate [3]. These circuits are only made of capacitors and switches realized with transistors (or diodes), thereby allowing direct on-chip integration. Despite the fact that charge pumps have relatively low efficiency and high area requirements, they also find application in the power supplies of smart power integrated circuits and systems [4].

From the design point of view, switches used in charge pumps should have a low value of switch-on resistance in order to achieve high efficiency. On the other hand, charge pumps are usually designed using gate-driven MOS switches. In such cases, the minimum input voltage of a CP is limited by the threshold voltage of MOS transistors (V_{th}). To overcome this limitation, it is necessary to look for new approaches and topologies able to work with low input voltage. Bulk-driven technique was introduced by Guzinski [5]. Recently, this technique has been used for design of basic building blocks of analog and digital integrated circuits (IC), e.g. operational amplifier [6], [7], current mirrors [8], [9], current converter [10], [11], operational transconductance amplifier (OTA) [6], [12], voltage follower [13], [14], voltage to current converter [15], voltage controlled oscillator [16], phase locked loop (PLL) [17], etc.

In this paper, a cross-coupled CP based on the dynamic threshold voltage CMOS inverter [18], [19] is presented. The proposed topology, based on the bulk-driven technique, allows the input voltage below the threshold voltage of MOS transistors. Preliminary work in presented in Sec. 2. Analysis of different types of CP topologies in terms of efficiency and value of the output voltage is done in the Sec. 3. In the Sec. 4, the proposed bulk-driven topology of cross-coupled CP is presented and compared to the conventional gate-driven cross-coupled CP described in [20], [21]. In this section, an optimization process for proposed bulk-driven charge pump in terms of chip area and current consumption is described. Achieved results are presented in the Sec. 5. In the last section, the efficiency of the proposed CP in terms of the obtained results is discussed.

2. Background

In electronic circuits, voltage converters are usually used to ensure a stable (regulated) value as well as proper polarity of the supply voltage. Actually, there are three basic types of voltage converters: linear voltage regulators, charge pumps and switching regulators. Comparison of basic properties of different voltage converters are summarized in Tab. 1 [22], [23].

Property	LDO	Charge Pump	Switching Regulator
Efficiency	*Poor*	*Good*	*Best*
Cost	*Best*	*Moderate*	*Most expensive*
Difficulty in design	*Easy*	*Harder*	*Most difficult*
(PCB) Area	*Very small*	*Small*	*Large*
Output ripple	*Very low*	*Moderate*	*Moderate*
EMI	*Very low*	*Low*	*Moderate*
Load capability	*Moderate* up to 150 mA	*Moderate* up to 250 mA	*Best* up to 500 mA
Transformation type	*Step down*	*Step up, Step down, Inverter,*	*Step up, Step down, Inverter*

Tab. 1. Comparison of voltage converters.

Linear voltage regulators are among the simplest and affordable voltage regulators. From Tab. 1, it can be observed that these regulators have poor efficiency. Thus, if high efficiency and high output current are required, switching regulators represent more suitable alternative. However, switching regulators consists of an inductor that requires considerable chip area overhead, which makes these converters not really proper for integration. Additionally, the quality of on-chip inductors is relatively poor. Although charge pumps have lower efficiency than the switching regulators, they represent the better alternative for on-chip implementation because they do not required area-critical devices like inductors. Output current of the charge pump can be effectively increased by sufficiently large capacitors. Consequently, charge pumps are widely used in the supply part of integrated systems. Comparison of published works in terms of converter topology, input and output voltages and efficiency are summarized in Tab. 2.

Since the selection of proper voltage converter depends on the input source as well as its output impedance and output voltage, many works based on the different approaches can be found in the literature [24–34]. From Tab. 2, one can observe that if the input voltage value is equal to or lower than the threshold voltage of MOS transistor, in most cases, the efficiency of a voltage converter will not be more than 65 %. For a low value of the input voltage (about 50 mV), voltage converters based on the transformer or inductor is used. On the other hand, if the input voltage is quite high (about twice the V_{th}), voltage converters based on the charge pump approach become more appropriate. For the input voltage in the middle of this range, a combined voltage converter, which exploits advantages of the approaches based on the transformer and inductor voltage converters is employed. In such an approach, the low input voltage is increases using the inductor-based voltage converter first. Then, the output voltage of the inductor converter feeds a charge pump converter. In [28], a thermocell with the output voltage of 200 mV ($\Delta T = 5\,^{\circ}\mathrm{C}$) was used as the input source. The converter was designed in technology that offers transistors with the ultra low threshold voltage of 100 mV, and therefore, an external start-up source is not necessary. The first stage of the converter was formed by a switching regulator to increase the output voltage of thermocell, and a charge pump was used as the second stage. In this case, the charge pump helps increase the output voltage of the switching regulator. Taking into account that the input voltage is already increased by the switching regulator, the number of stages in the charge pump can be significantly reduced.

The main advantage of switching regulators is ability to transform a low input voltage to high value of the output voltage with a minimum amount of loss. However, very low value of the input voltage might cause start-up problems, and therefore, the control and switching logic have to be supplied from an external source. The switching converter concept presented in [26] can work with a low input voltage (about 20 mV) but for a proper functionality of the whole converter with control circuity, its output voltage has to be at least about 600 mV. This problem can be solved using specific technology, e.g. *Carbon Nanotube Field Effect Transistor* (CNFET), which offers transistors with an ultra-low value of the threshold voltage ($V_{\mathrm{th}} \approx E_{\mathrm{g}}/2q$) [25]. In [25], a charge pump was used as a part of switching regulator to control CNFETs.

As for charge pumps, the largest amount of loss is caused by parasitic capacitance of the switched capacitor. Coefficient α represents a ratio between a value of parasitic capacitance and a value of the nominal switched capacitor. In order to increase the charge pump efficiency, a poly-poly (PP) capacitor may be replaced by metal-insulator-metal (MIM) capacitor, since its parasitic capacitance is much smaller ($\alpha \approx 3\,\%$) than that of a poly capacitor ($\alpha \approx 20\,\%$). In [33], the input voltage is limited to 600 mV and this value is given by the threshold voltage of transistors in used CMOS 350 nm technology. On the other hand, in [30], [31] the input voltage is about 150 mV because these converters are implemented in 65 nm technology that offers transistors with a lower value of the threshold voltage.

Since the charge pumps represent the most appropriate solution for on-chip implementation of voltage converters, it is necessary to develop new CP topologies that would be less dependent on the threshold voltage of MOS devices in the selected integration technology.

3. Analysis of Different Charge Pumps

The detailed analysis of the different charge pump topologies (representing the most used charge pumps) was performed through simulation and comparison of the following parameters: the output power, the output voltage, the conversion efficiency and the silicon area in terms of the

Converter topology	Reference	Input voltage	Output voltage	Efficiency	Process
inductive	[24]	50 mV	1.8 V	58 %	350 nm
	[25]	100 mV	0.65 V	27 %	CNFET
inductive + CP	[26]	20 mV	1.0 V	46 %	130 nm
	[26]	100 mV	1.0 V	75 %	130 nm
	[27]	100 mV	0.9 V	72 %	65 nm
	[28]	200 mV	1.2 V	40 %	180 nm
	[29]	200 mV	2.8 V	63 %	350 nm
CP	[30]	150 mV	0.85 V	30-80 %	65 nm
	[31]	180 mV	0.7 V	N/A	65 nm
	[32]	450 mV	1.4 V	58 %	130 nm
	[33]	600 mV	2.0 V	73 %	350 nm

Tab. 2. Selected converters - parameter comparison.

	A	B	C	D	E
Number of stages	4	4	4	4	4
Max. V_{out} (V)	1.64	1.60	2.48	1.64	2.43
Max. P_{out} (µW)	49	79	217	59	62
Max. η (%)	26	27	40	21	18
V_{out}@Max. η / Max.V_{out} (%)	64.7	50.1	60.5	67.2	68.0
V_{rip}@Max. η (%)	0.26	0.41	0.51	0.04	0.89
Number of transistors	5	5	16	16	18
Number of capacitors	4+1	4+1	8+1	8+1	8+1

A - Cockcroft-Walton charge pump
B - Dickson charge pump
C - Cross-coupled switched capacitors charge pump
D - Cross-coupled switched capacitors charge pump with only NMOS
E - Cockcroft-Walton charge pump with controlled charging

Tab. 3. Achieved parameters of analyzed charge pumps.

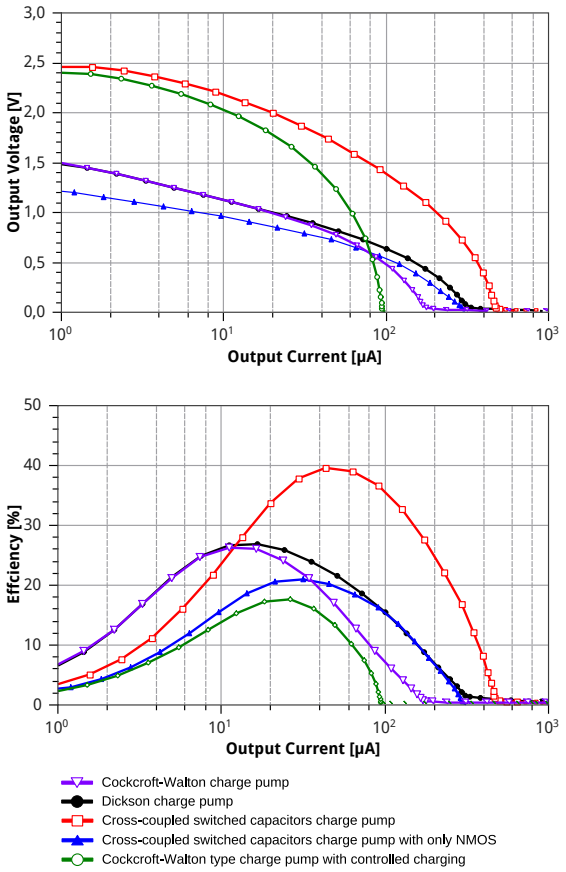


Fig. 1. Comparison of CP parameters.

number of circuit elements. More detailed description of the analyzed CP topologies is presented in [35]. However, it is important to note that the selected CP topologies, designed in 90 nm CMOS technology, were not optimized that enables the relevant comparison of the CP topologie in terms of the area requirements and the output power. The size of all MOS transistors and all capacitors including the output capacitors was identical in all topologies that were realized as four-stage charge pumps. The input voltage (V_{in}) was chosen so that its value would be greater than the threshold voltage (V_{th}) of used transistors. Thus, for the input voltage as well as the switching voltage (V_{ϕ}), the value of 500 mV was used. This voltage ensures that all transistors will work in the active region.

In Tab. 3, the achieved parameters of the analyzed CPs are presented, where the most important properties are summarized and compared. Figure 1 shows the dependency of the CP parameters on the value of the output current.

From the presented results, one could possibly draw that in 90 nm CMOS technology, the Cockcroft-Walton charge pump and Dickson charge pump are comparable with respect to the output voltage level and the conversion efficiency. Another significant parameter is the circuit size mainly given by the number of all circuit components. It can be observed that the highest output voltage can be obtained by the cross-coupled switched capacitors charge pump and Cockcroft-Walton topology with controlled charging, in which the number of used devices is nearly the same. The main difference between all analyzed topologies is the maximum efficiency and the output power that can be possibly achieved. In applications that harvest the power supply from alternative energy sources, the conversion efficiency, of course, is the most important parameter. Taking this priority into account, the cross-coupled switched capacitors charge pump exhibits the maximum achievable conversion efficiency of 40 %.

From the preformed analysis, it can be concluded that the cross-coupled switched capacitors charge pump represents an appropriate topology choice if high efficiency is primarily targeted. Therefore, in the next section, the conventional gate-driven cross-coupled charge pump as well as proposed bulk-driven cross-coupled CP are described and their properties are analyzed and compared.

4. Proposed Bulk-driven Charge Pump

4.1 Conventional Cross-coupled CP

Figure 2 shows a CMOS realization of the conventional charge pump based on the cross-coupled voltage doubler. This charge pump represents one of the highly efficient

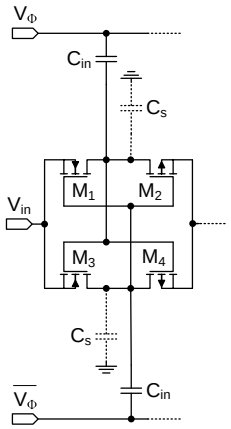
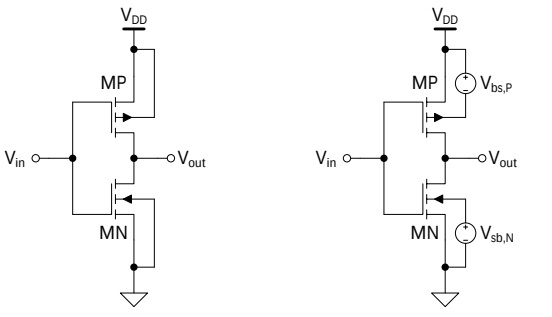
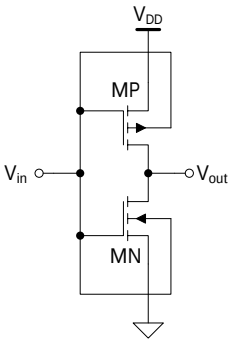


Fig. 2. Classical cross-coupled CP (one stage).



(a) CMOS inverter (b) Reduced V_{th} MOS inverter



(c) Dynamic V_{th} MOS inverter (DTMOS)

Fig. 3. Different inverters in CMOS technology.

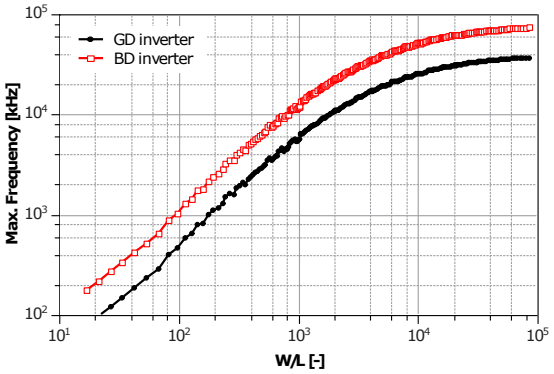


Fig. 4. Cut-off frequency of dynamic V_{th} inverter (V_{DD} = 200 mV, C_{load} = 1 pF).

topologies that are implementable on-chip. Cross-coupled charge pump uses both types of MOS transistors. The used control method eliminates the voltage stress exerted on the transistor's gate oxide [35]. Voltage losses contain only the voltage drop at the open transistors and the equivalent resistance of the switched capacitors [20], [21].

4.2 Dynamic V_{th} MOS Inverter

As can be seen from Fig. 2, the cross-coupled charge pump is based on two inverters connected across. The minimum input switching voltage $V_{\phi min}$ for this topology is, like in the case of a CMOS inverter, twice the threshold voltage of the MOS transistor used. Therefore, in order to use this topology in the ultra low-voltage applications, some modifications are needed. The possible solution how to decrease the value of the minimum input switching voltage is to replace one of transistors with a resistor that will create a pseudo-inverter. Unfortunately, this increases the current consumption in an unacceptable way for most of applications. Another possible approach is based on shifting the threshold voltage of the MOS transistor by connecting its bulk electrode to a fixed potential, as depicted in Fig. 3(b). Nevertheless, this solution will increase the leakage current significantly and therefore, it is not suitable for low-power charge pump design. The proper solution seems to be dynamic control of the substrate electrode. Bulk dynamic threshold inverter (Fig. 3(c)) is based on controlling the substrate electrode of NMOS and PMOS transistors by the input signal [18], [19]. When the transistor is turned off, the threshold voltage achieves its nominal value and the leakage current is minimized. Otherwise, if the transistor is turned on, the threshold voltage is decreased that will cause the increase of the output current and switching speed.

MOS inverter topology with dynamic V_{th}, shown in Fig. 3(c), represents an appropriate building block for low input voltage and low-power design of charge pumps. However, it is important to note that dynamic V_{th} MOS inverter may be implemented only in twin-well CMOS process, where PMOS and NMOS transistors may be placed in separated wells. Since the dynamic V_{th} MOS inverter is based on the bulk-driven approach, the maximum value of supply and in-

put voltages should not exceed 0.6 V [18], [19]. Otherwise, parasitic NPN and PNP bipolar transistors will turn on, which with the high probability may cause latchup. These limitations have to be taken into account if designing the charge pump with dynamic V_{th} MOS inverters.

In order to justify the employment of the dynamic V_{th} inverter in charge pumps with low input voltage, the switching performance of the inverter was investigated through simulation of the maximum frequency for different size of the MOS transistors (Fig. 4). Obtained maximum frequency of dynamic V_{th} inverter was compared to the maximum frequency of a conventional CMOS inverter for supply voltage of 200 mV and load capacitance of 1 pF. As can be seen from the Fig. 4, cut-off frequency of dynamic V_{th} inverter is a bit higher than in the case of the conventional gate-driven inverter. However, if we consider a lower load capacitance, e.g. the input capacitance of DTMOS inverter, the cut-off frequency can be even higher.

4.3 Bulk-driven Cross-coupled CP

The proposed bulk-driven charge pump designed in 90 nm CMOS technology is based on the cross-coupled topology, where dynamic V_{th} MOS inverter was used (Fig. 5). All limitations described in the previous section were taken into account. The proposed charge pump can work with very low input voltages, which is the main advantage of this topology. On the other hand, an increased possibility of latchup occurrence is the most significant drawback. Therefore, the proposed bulk-driven cross-coupled charge pump is supposed to be used only in low-voltage and low-power applications.

Theoretical value of the output voltage can be expressed as follows:

$$V_{out} = V_{in} + N\left(V_{\phi}\frac{C_{in}}{C_{tot}} - I_L\left(R_{on} + \frac{R_{eq}}{2}\right)\right) \quad (1)$$

where

N is a number of stages used
V_{in} is the input voltage
V_{out} is the output voltage
V_{ϕ} is the switching voltage
C_{in} is the switching capacitance
C_{tot} is sum of switching capacitance and parasitic capacitance

$$C_{tot} = C_{in} + C_s \quad (2)$$

I_L is sum of output and leakage currents

$$I_L = I_{out} + I_{leakage} \quad (3)$$

R_{on} is switch-on resistance of NMOS and PMOS transistor
R_{eq} is equivalent resistance of switching capacitor

$$R_{eq} = \frac{1}{fC_{tot}}. \quad (4)$$

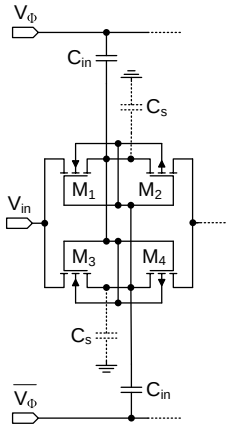


Fig. 5. Bulk-driven cross-coupled CP (one stage).

4.4 Design and Optimization of Proposed CP

In the design phase of analog integrated circuits, usually the compromise between area and current consumption has to be made. Such a compromise can be achieved, for example, through the optimization process presented in [4], where optimization of Dickson charge pump was presented. For optimum design of the proposed bulk-driven cross-coupled charge pump in terms of area and supply current, (1) has to be rewritten as follows:

$$V_{out} = V_{in} + NV_{\phi}\frac{1}{1+\alpha} - NI_L R_{on} - NI_L\frac{1}{C_{tot}2f} \quad (5)$$

where f is the switching frequency and α is technology parameter that expresses a ratio between parasitic (C_s) and nominal capacitance (C_{in}) of the selected capacitor that is given by (6).

$$\alpha = \frac{C_s}{C_{in}}. \quad (6)$$

It is important to note that term C_{in} / C_{tot} from (1) can be expressed using parameter α as follows:

$$\frac{C_{in}}{C_{tot}} = \frac{1}{1+\alpha}. \quad (7)$$

The optimization process targets finding an optimum number of stages and an optimum value of the switching capacitor for the given input and output voltages, output current and switching frequency. Thus, we first express the dependence of the total area of charge pump on the selected design parameters. The optimization process in terms of area and total current consumption, presented in the next two subsections, can be applied to both the classical cross-coupled and also to the proposed bulk-driven cross-coupled charge pump.

4.4.1 Area Optimization

The total area of the proposed charge pump can be expressed by (8):

$$S_{tot} = S_{cap} + S_{mos} \quad (8)$$

where S_{cap} is the area of all switched capacitors and S_{mos} is the total area of transistors. In order to simplify the optimization process, in the most cases, the area of transistors can be neglected since being much smaller than the area of switched

capacitors. Thus, the total area is given by the following equation:

$$S_{\text{tot}} \approx S_{\text{cap}} = k_{\text{C}} 2NC_{\text{in}} \tag{9}$$

where k_{C} is a coefficient that represents capacitance per area and its unit is Fm^{-2}. If we consider that $\alpha = 0$, using (5) and (9), one can get (10) that expresses the dependence of the CP total area on selected design parameters

$$S_{\text{tot}} = \frac{N^2}{V_{\text{in}} + N.V_{\phi} - NI_{\text{L}}R_{\text{on}} - V_{\text{out}}} \frac{k_{\text{C}} I_{\text{L}}}{f}. \tag{10}$$

In order to obtain the optimum number of stages for required parameters of the charge pump, (10) is derived with respect to the number of CP stages. To find a local extrema, the derivation of (10) with respect to the number of stages is set equal to zero. How is presented in (11)

$$\begin{aligned} \frac{\partial S_{\text{tot}}}{\partial N} &= 0, \\ \frac{\partial \left(\frac{N^2}{V_{\text{in}} + NV_{\phi} - N.I_{\text{L}}R_{\text{on}} - V_{\text{out}}} \frac{k_{\text{C}} I_{\text{L}}}{f} \right)}{\partial N} &= 0, \\ \frac{-2N\Delta V + N^2 V_{\text{eff}}}{(-\Delta V + NV_{\text{eff}})^2} \frac{k_{\text{C}} I_L}{f} &= 0, \\ N\left(-2\Delta V + NV_{\text{eff}}\right) &= 0. \end{aligned} \tag{11}$$

There are two roots of (11), where the first one is $N = 0$ that cannot be practically implemented. The second root represents an optimum number of CP stages with respect to area and is given by (12):

$$N_{\text{Sopt}} = 2\frac{\Delta V}{V_{\text{eff}}} \tag{12}$$

where ΔV is a difference between the required input and output voltages of the proposed charge pump and V_{eff} is an effective value of the switching voltage, as expressed in (13).

$$\begin{aligned} \Delta V &= V_{\text{out}} - V_{\text{in}} \\ V_{\text{eff}} &= V_{\phi} - I_{\text{L}} R_{\text{on}} \end{aligned} \tag{13}$$

From (12), it can be observed that the optimum number of CP stages should be two times higher than the required voltage gain of the charge pump (which is given by ratio of ΔV and V_{eff}). Finally, using (10) and (9), the optimum value of the switched capacitor can be obtained for required parameters of the charge pump (14)

$$C_{\text{in opt}} = \frac{N_{\text{Sopt}}}{V_{\text{in}} + N_{\text{Sopt}} V_{\phi} - N_{\text{Sopt}} I_{\text{L}} R_{\text{on}} - V_{\text{out}}} \frac{I_{\text{L}}}{2f}. \tag{14}$$

If we neglect the term $NI_{\text{L}}R_{\text{on}}$ in (10) and (14), for the area optimization process, one can conclude that the total area of the charge pump increases linearly with the load current and quadratically with the number of stages. How is presented in (10). On the other hand, the area overhead can be reduced by increasing the switching frequency.

4.4.2 Current Consumption Optimization

A similar approach can be applied for optimization of the charge pump in terms of current consumption. The total current consumption I_{VDD} of N-stage charge pump can be expressed as:

$$I_{\text{VDD}} = (I_{\text{ideal}} + I_{\text{par}}) \tag{15}$$

where I_{ideal} is an ideal current delivered to the load from the supply source, which can be defined as amount of charge ΔQ that is passed across the CP stages during one period of switching signal, descripted with (16). I_{par} represents a current that is needed for charging parasitic capacitances and is given by (17). It is important to note that for simplified analysis, the losses between stages have not been considered.

$$I_{\text{ideal}} = (N+1)\frac{\Delta Q}{T/2} = (N+1)I_{\text{L}} \tag{16}$$

$$I_{\text{par}} = N\frac{C_{\text{s}} V_{\phi}}{T/2} = \alpha N C_{\text{in}} 2 f V_{\phi} \tag{17}$$

By combining (14), (15), (16) and (17), the dependence of the total current consumption on the CP parameters can be obtained, as expressed in (18). It can be seen that the total current consumption depends neither on the value of switched capacitors nor on the switching frequency. However, it is linearly dependent on the output current of a charge pump

$$I_{\text{VDD}} = \left((N+1) + \alpha \frac{N^2}{V_{\text{in}} + NV_{\phi} - NI_{\text{L}}R_{\text{on}} - V_{\text{out}}} V_{\phi} \right) I_{\text{L}}. \tag{18}$$

As in the previous case, derivation of (18) with respect to the number of stages will give the optimum number of stages with respect to the total current consumption. This is expressed as follows:

$$N_{\text{Iopt}} = \frac{\Delta V}{V_{\text{eff}}} \frac{1 + \frac{\alpha V_{\phi}}{V_{\text{eff}}} \sqrt{1 + \frac{V_{\text{eff}}}{\alpha V_{\phi}}} + \frac{\alpha V_{\phi}}{V_{\text{eff}}}}{1 + \frac{\alpha V_{\phi}}{V_{\text{eff}}}}. \tag{19}$$

The optimal number of stages is given by the required voltage gain. Again, the value of the switched capacitor can be obtained using (14).

5. Achieved Results

The proposed bulk-driven (BD) and classical gate-driven (GD) cross-coupled charge pumps were designed and analyzed, and the achieved parameters were compared. Design was realized in 90 nm CMOS technology. The number of stages and size of used transistors and capacitors in both topologies were identical. Moreover, in both cases, values of the input voltage V_{in} and the switching voltage V_{ϕ} were equal. Non-overlapping clock with frequency of 100 kHz was used. NMOS transistors with channel dimensions (width/length) of 100 µm/0.1 µm were used, while PMOS transistors were two times larger. If considering the given dimensions of NMOS and PMOS transistors, R_{on} of one stage of the proposed BD and conventional GD CP will be 675 Ω and 1750 Ω, respectively.

In order to evaluate the accuracy of the output voltage calculation (based on (1)), the calculated output voltages

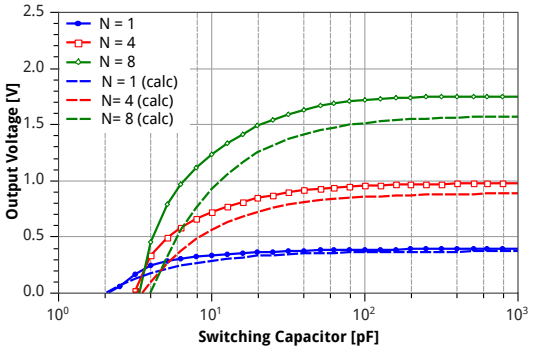


Fig. 6. Output voltage vs. Switching capacitor (GD CP) (V_{in} = 200 mV, f = 100 kHz, I_{out} = 100 nA, R_{on} = 1750 Ω).

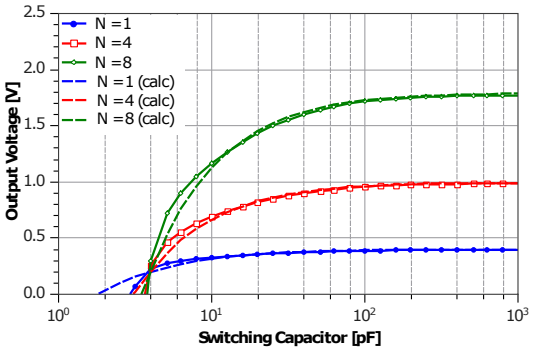


Fig. 7. Output voltage vs. Switching capacitor (BD CP) (V_{in} = 200 mV, f = 100 kHz, I_{out} = 100 nA, R_{on} = 650 Ω).

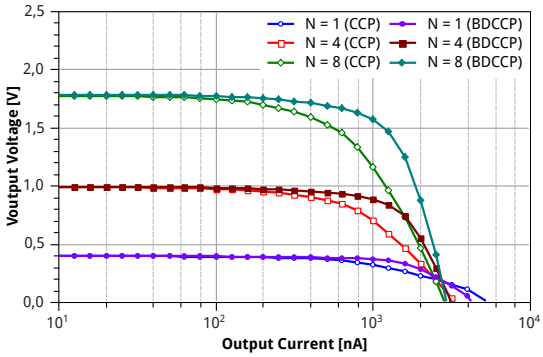


Fig. 8. Output voltage vs. Output current (V_{in} = 200 mV, f = 100 kHz, C_{in} = 1 nF).

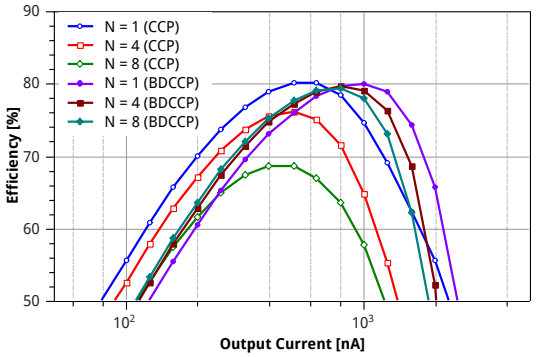


Fig. 9. Conversion efficiency vs. Output current (V_{in} = 200 mV, f = 100 kHz, C_{in} = 1 nF).

were compared to the simulated values, and results for both CP topologies are presented in Fig. 6 and Fig. 7. In the performed simulations, an ideal current source was used as the load of the charge pump in order to ensure a constant output current at the CP output. In this experiment, the following setup was used: V_{in} = 200 mV and I_{out} = 100 nA. From Fig. 6, one can observe a certain difference between calculated (dashed curves) and achieved simulated (solid curves) values. The reason is that the equation for the output voltage calculation is based on static parameters and does not include dynamic behavior. Additionally, the input voltage V_{in} is lower than the threshold voltage of MOS devices. Thus, for $V_{in} > V_{th}$, the relative error is smaller than 10 %. In the case of the proposed BD cross-coupled CP (Fig. 7), expected and achieved results are almost identical since use of the dynamic threshold MOS inverter eliminates the impact of V_{th} value on the calculation accuracy.

Comparison of results achieved for both topologies in terms of the output current is depicted in Fig. 8, where a good match of the output voltage is observed in the whole considered range of the output current. One can also observe that with increasing output power, the voltage loss gets higher for classical cross-coupled CP with respect to BD topology (e.g. see for I_{out} = 1 µA). For four-stage charge pumps (N = 4), the output voltage of 0.70 V and 0.89 V is achieved for classical topology and BD topology, respectively. It means that there is a difference of 189 mV for the two solutions, which corresponds to loss of almost one stage. This difference is even greater for eight-stage (N = 8) charge pumps, i.e. the output voltage values are 1.17 V (classical topology) and 1.57 V (bulk-driven) that makes the difference of 400 mV. This corresponds to loss of about two stages of the charge pump.

Figure 9 shows dependence of the efficiency of both CP topologies on the output current for following parameters: $V_{in} = V_{\phi}$ = 200 mV and f = 100 kHz; C_{in} = 1 nF. The best efficiency for the given parameters can be observed for the output current of 1 µA, where the new bulk-driven cross-coupled charge pump achieves the efficiency of 80 % in four-stage architecture (N = 1).

In the next step, we compared calculated and simulated results, where optimization (described in Sec. 4.4) of classical gate-driven (GD) cross-coupled and the proposed BD charge pump in terms of the total area and current consumption was performed. Table 4 presents results of area optimization for both CP topologies and for different output voltage values, where the switching frequency and the output current was set to 100 kHz and 1 µA, respectively. It can be observed that the optimum number of stages for the required output voltage is the same for both topologies. Therefore, switched capacitors as well as the total area of charge pumps are similar in both cases too. Nevertheless, the simulated output voltage of the proposed BD

V_{out} [V]	0.5		1		1.5		2	
Typ	BD	GD	BD	GD	BD	GD	BD	GD
N [-]	3	3	8	8	13	13	18	18
C_{in} [pF]	75	78	75	78	75	78	75	78
S_{tot} [mm^2]	0.11	0.12	0.29	0.31	0.47	0.50	0.65	0.69
V_{outSIM} [mV]	289	213	598	407	897	603	1 195	799
error [%]	42.2	57.4	40.2	59.3	40.2	59.8	40.3	60.1

Tab. 4. Comparison of BD and GD charge pumps in terms of area optimization.

V_{out} [V]	0.5		1		1.5		2	
Typ	BD	GD	BD	GD	BD	GD	BD	GD
N [-]	2	2	5	5	8	9	12	12
C_{in} [pF]	170	177	251	266	285	150	170	177
S_{tot} [mm^2]	0.17	0.18	0.62	0.65	1.12	0.66	1.00	1.10
V_{outSIM} [mV]	484	395	998	776	1 501	1 077	1 902	1 464
error [%]	3.2	21.0	0.2	22.4	0.1	28.2	4.9	26.8

Tab. 5. Comparison of BD and GD charge pumps in terms of current consumption optimization.

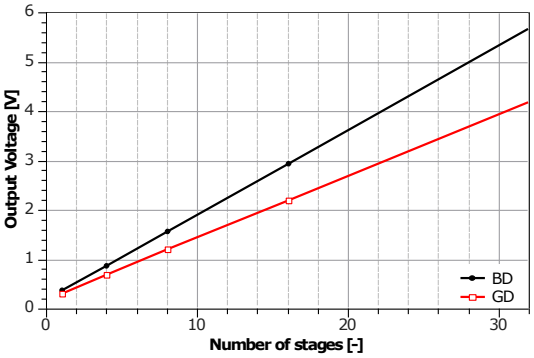


Fig. 10. Output voltage vs. number of stages (V_{in} = 200 mV, f = 100 kHz, C_{in} = 1 nF, I_{out} = 1 µA).

topology is higher despite the fact that the calculation error is about 40 %. For the classical charge pump topology, the calculation error of 60 % is reported.

Similarly, the optimization process in terms of the total current consumption for both analyzed CP topologies and for different output voltage was done, and the comparison of the achieved results is summarized in Tab. 5.

As in the previous case, the optimum number of stages as well as the value of switched capacitors and the total area are similar for both topologies. The calculated number of CP stages was rounded to an integer. To reduce the difference (calculation error) between the theoretical and simulated values of the output voltage, the rounding up may be used, which will cause a decrease of C_{in} value and the total area (S_{tot}) will be affected as well.

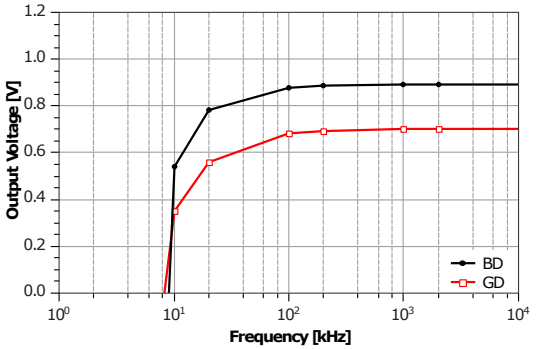
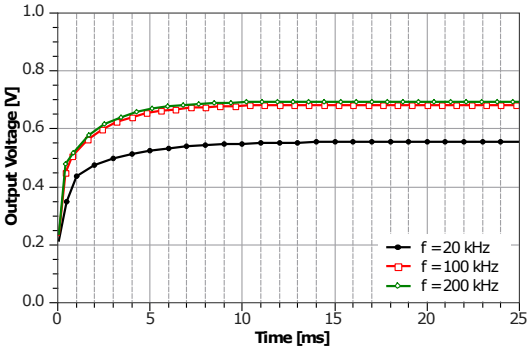
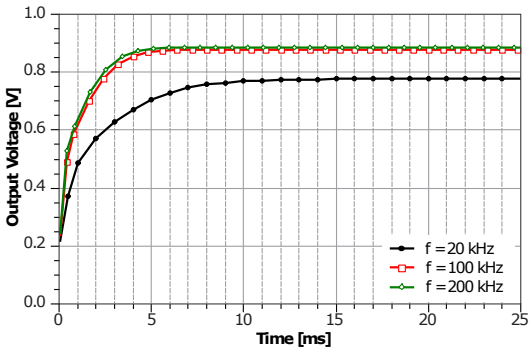


Fig. 11. Output voltage vs. switching frequency (V_{in} = 200 mV, C_{in} = 1 nF, I_{out} = 1 µA, N = 4).



(a) Gate-driven charge pump



(b) Bulk-driven charge pump

Fig. 12. Start-up process of charge pumps (V_{in} = 200 mV, C_{in} = 1 nF, I_{out} = 1 µA, N = 4).

Finally, the efficiency of the proposed BD charge pump was investigated and achieved results compared to those of a conventional GD cross-coupled topology. Such a comparison, presenting the output voltage of both topology for different the number of stages, is depicted in Fig. 10. One can observe that for high number of stages, the output voltage of the proposed BD charge pump is higher. Both CP topologies exhibit the same trend of the output voltage vs switching frequency curve. Particularly, both charge pumps achieve approximately 97 % of the maximum output voltage at the switching frequency of 100 kHz (Fig. 11).

Figure 12(a) and 12(b) show the start-up process of 4-stage GD and BD charge pump, respectively. As expected,

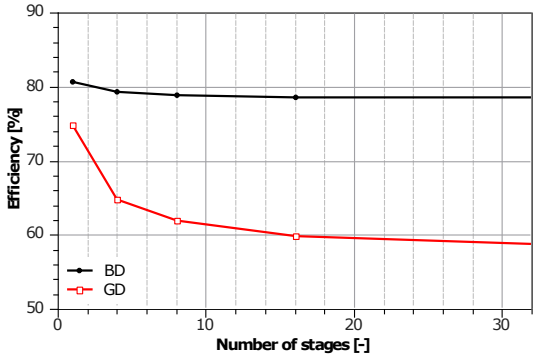


Fig. 13. Efficiency vs. number of stages (V_{in} = 200 mV, f = 100 kHz, C_{in} = 1 nF, I_{out} = 1 µA).

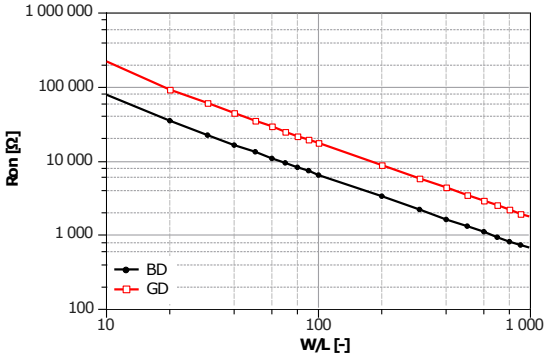


Fig. 14. R_{on} vs. MOS transistor's dimensions.

the slowest starting time is observed for the lowest switching frequency (black line with a dots). Time needed to achieve 95 % of the maximum output voltage (at the switching frequency of 100 kHz) is 4.4 ms and 3.4 ms for GD and BD charge pump, respectively.

Figure 13 shows dependence of the efficiency of the BD and GD cross-coupled charge pumps on the number of stages. It can be observed that for a small number of stages, the efficiency will be approximately similar for both topologies. However, for higher number of stages, the BD charge pump exhibits higher efficiency (by up to 20 %).

6. Discussion and Conclusion

From the preformed analysis, it can be concluded that using the proper design and optimization of the proposed cross-coupled charge pump based on the bulk-driven approach, higher efficiency than in the case of GD cross-coupled charge pump can be achieved.

As described in the previous section, the optimization process and all general equations are valid for both topologies and can be effectively used in design of cross-coupled CPs of different topologies. However, the main difference between compared topologies is in the switch-on resistance of one stage. Figure 14 shows the dependence of one stage switch-on resistance on dimensions of MOS transistors forming the charge pumps. It is important to underline that one stage of the proposed BD cross-coupled charge pump has about three times lower switch-on resistance than one stage of the conventional GD cross-coupled charge pump.

Optimizations of the designed charge pumps in terms of the total area and current consumption have been performed in order to evaluate the best achievable parameters. Optimization process is based on the finding an optimal number of stages for required parameters of the selected CP topology. Simulation results of such an optimization in terms of area indicated that when using the optimum number of stages, the output voltage value will be lower by 50 % than in the case of calculated results. The main reason is that in the simulations, the ideal current source was connected to the CP output. From Fig. 6 and Fig. 7, it can be observed that calculated dependence of the output voltage and the value of switched capacitor slightly differ from those obtained by simulation. This causes certain inaccuracy in the optimization process. On the other hand, it was shown that for the number of stages above 10, the efficiency of the proposed BD cross-coupled charge pump is about 20 % higher than in the case of conventional cross-coupled charge pump. Here, it is important to note that during the comparison process, identical chip area for both topologies was considered. However, if we consider the same efficiency for both CP topologies, the total area needed for one stage of the proposed BD charge pump will be smaller by 38 %, where switched capacitors' size is reduced by 33 %, while MOS transistors can be smaller by 40 %.

The proposed topology of cross-coupled charge pump based on the DTMOS inverter can be effectively used in battery-powered applications, where low supply voltage value is expected. Cross-coupled charge pump based on the bulk-driven approach has about 20 % higher efficiency than GD cross-coupled charge pump. On the other hand, some layout techniques have to be applied in order to prevent latchup triggering. Nevertheless, the proposed BD cross-coupled topology represents good choice for ultra low-voltage and low-power systems and on-chip energy harvesters implemented in nanoscale technologies.

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