FULL CUSTOM DESIGN OF A 8-BIT SUBRANGING FLASH A/D CONVERTOR

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Abstract

This paper describes the design of a Nonius Flash Analog to Digital Convertor for video-applications. The conversion is split up in two stages: the MSB and the LSB conversion stage. In the LSB conversion stage, the reference-voltage for the comparators is shifted up and down as a nonius of a vernier gauge, according to the MSB conversion obtained in the first half clock cycle. The MSB's and LSB's are simultaneously available at the output to make a 8-bit representation of the analog signal. Using the subranging mechanism, the number of comparators is reduced from 256 to 32 and the Nonius approach results in a very simple configuration for the subranging switches. The design has been simulated with HSPICE in ES2 1.5 CMOS technology.

Keywords:

Microelectronics, A/D convertors, Integrated circuits, Custom design

1. Introduction

A lot of AD-convertor architectures have been published for all kind of applications. This design is intended for CMOS Video CODEC's and is based on a new variant of the well known subranging flash AD-convertor concept. The convertor consists of two functional blocks: the first block is converting the MSB's and the second block is zooming in for the LSB's. The 4 MSB's give the course range of the analog signal and the position for the second block to zoom in with a higher precision by means of 4 LSB's. For the zoom action the reference voltage of the LSB comparators is shifted according to the obtained MSB-code. The MSB and LSB convertor make the 8-bit representation of the analog signal available in 2 consecutive half clock cycles.

The architecture of the flash-AD consists of 3 basis-blocks as presented in figure 1:

- an array of comparators to compare the input signal with the reference voltages on the resistive divider chain;
- a resistive ladder network to subdivide the reference voltages;
- a control block to convert the thermometer code to a binary code.

By using 2^n comparators for an n-bit flash-AD, the 2^n different reference levels are compared simultaneously with the input signal. The transition-level is obtained at once after the propagation delay of the comparators and the thermometer to binary code convertor. This is the fastest way of detection.

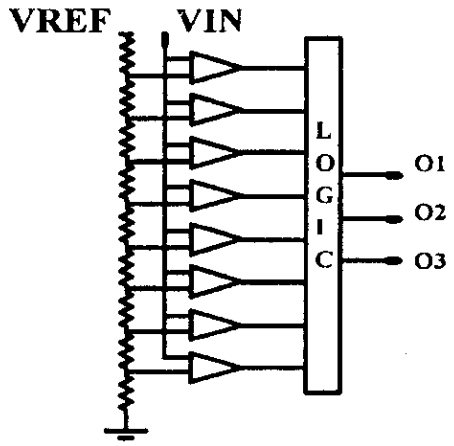

Fig. 1
Basic architecture of flash ADC (e.g. 3 bits)

However for a 8-bit AD-convertor, 256 comparators are placed in parallel, which result in a high input capacitance and a reduced bandwidth. Also the high number of comparators results in an increasing power consumption.

2. Flash AD-convertor with shifting reference voltages

As in every subranging flash A/D, to improve the detection according to speed and power consumption, not all 256 levels are compared simultaneous with the input

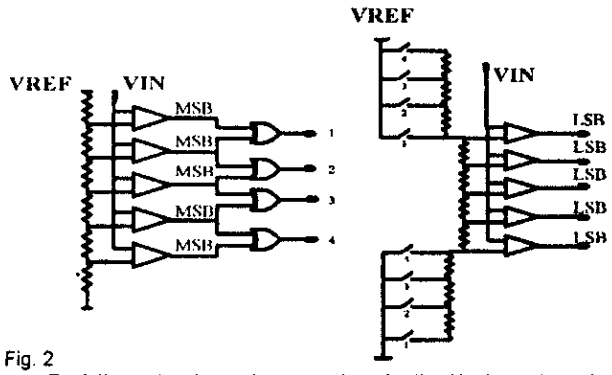

Fig. 2
Resistive networks and comparators for the Nonius subranging flash ADC

signal. The detection is divided into the MSB-part and the LSB-part as illustrated in figure 2 for a 4 bit A/D.

Looking at figure 2 we see that the switches on the nonius resistor string are always at the positive or negative reference potential so avoiding non-linearity errors from the bulk effect of the switches.

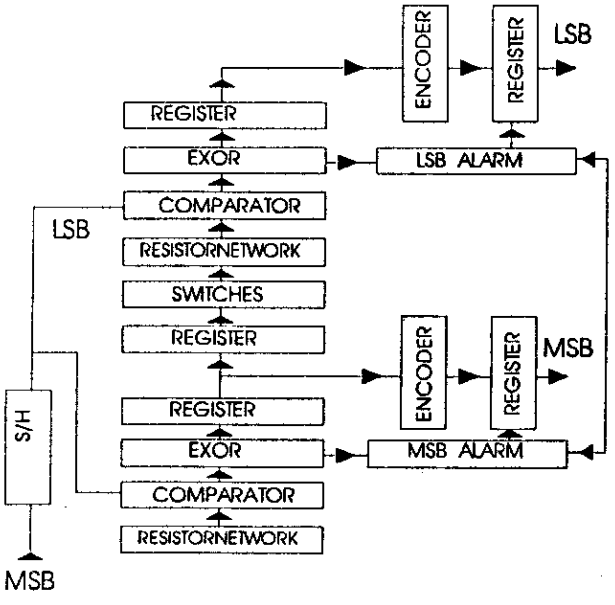

Fig. 3
Architecture of flash ADC with shifting reference voltage

The architecture of the global AD-convertor is illustrated in figure 3.

First, a resistive ladder and the MSB-comparators detect the MSB's and this result set the switches of an other resistive network for the detection of the LSB's. During the detection of the corresponding LSB's, the first resistive network and MSB-comparators are already working on the MSB's for the next sample. The MSB's are delayed over half a clock cycle in order to be presented simultaneously with the LSB's at the output. To obtain the high speed and to be sure of the synchronisation among all subblocks, a pipeline structure is used.

2.1 MSB-detection

In the first stage, the input signal is compared with the 16 reference voltages for the detection of the 4 MSB's of the converting signal. The exor-gates calculate between which comparators the position of the transient is located. This result is converted by the encoder to a binary code for the MSB's and also controls the switches of the resistive network for the LSB's. In addition to this an alarm is detected as eventually it occurs that a comparator is sitting on the metastable position between a zero or one decision. In case of an alarm detection the convertor is repeating the previous sample instead of a wrong code.

2.2 LSB-detection

After closing the correct switches of the resistive network, the detection of the LSB's can start in the next half clock cycle.

A sample and hold circuit is avoiding time skew between the MSB and the LSB conversion of one sample.

As well as on the MSB's an alarm detection is provided on the LSB's.

2.3 MSB- and LSB-conversion to binary code

The conversion of the LSB's is similar to the conversion of the MSB's. The output signals of the exors are converted by the encoder to binary code. The outputs of the MSB- and LSB-encoder are shifted in a register and make the 8-bit converted signal at the ADC-output. However,

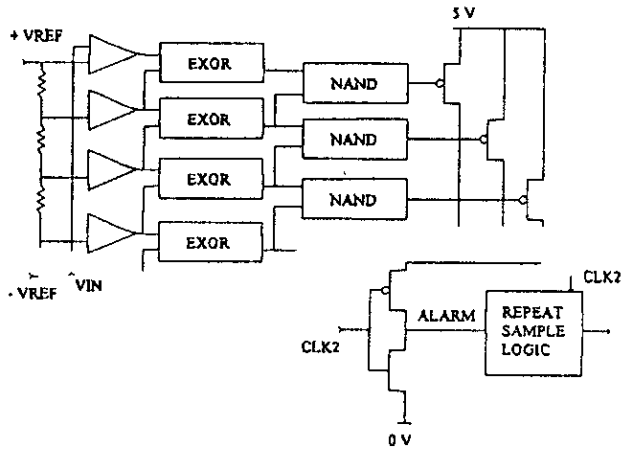

Fig. 4
Illustration of the circuit that is used to detect the multiple 1's.

because the MSB's and LSB's are detected separately and on a different moment, the MSB's are delayed over half of a clock cycle to resynchronise the LSB's.

2.4 Alarm detection

Both the MSB and the LSB convertor contain an alarm detection logic to detect the comparators being on the metastable point in between the 0/1 decision. As this

condition can occur, the exor array will produce multiple 1's causing abrupt code errors. The alarm signal is used to cause a repetition of the previous code instead of the erronevous code. Figure 4 illustrates the circuit that is used to detect the multiple 1's..

3. CAD-Software

For the design of the ADC in 1.5U CMOS technology from ES2, CAD-software from IMEC (Leuven-Belgium) and EUROCHIP (Education initiative of the EC) have been used.

HSPICE has been used for simulation of the subcircuits and finally for simulation of the whole circuit, parasitic effects due to layout included. For the layout of the sub-circuits, the symbolic layout programme Cameleon (IMEC) and Cadence have been used.

4. Conclusion

A new variant on the well known subranging A/D architecture is described. Using the 'nonius' principle the switches for the subranging in the LSB convertors resistor string don't suffer from the bulk effect that can cause linearity errors.

The described architecture is applied in a high speed 8-bit A/D convertor for video application.

5. References

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