A DIGITALLY PROGRAMMABLE DIFFERENTIAL INTEGRATOR WITH ENLARGED TIME CONSTANT

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Abstract

A new Operational Amplifier (OA)-RC integrator network is described. The novelties of the design are used of single grounded capacitor, ideal integration function realization with dual-input capability and design flexibility for extremely large time constant involving an enlargement factor (K) using product of resistor ratios. The aspect of the digital control of K through a programmable resistor array (PRA) controlled by a microprocessor has also been implemented. The effect of the OA-poles has been analyzed which indicates degradation of the integrator-Q at higher frequencies. An appropriate Q-compensation design scheme exhibiting 1 : $|A|^2$ order of Q-improvement has been proposed with supporting experimental observations.

1. Introduction

Microelectronic integrators are useful for a variety of signal processing/conditioning applications, e.g., wave-generation and shaping, as electronic controller and pole-zero compensator and as building blocks for state variable type double-integrator loop filters/oscillators and differential analyzers etc. [1]. Their digitally programmable versions, like digitally controlled amplifiers [2],[3], will be equally useful for the processing/conditioning of digital signals [4]. In all these analog/digital applications, it is desirable that the reset time constant (T_0) should be tunable by a single resistor and it should be very large without having to depend on large-value capacitors since integrated capacitors are limited only to low values. Hence a multiplier (K > 1) that enlarges the nominal time constant (T) to T_0 (=KT) must be available in the circuit design where the parameter K should involve an independent resistor ratio to ensure tunability. If this resistor ratio is replaced by a PRA [2],[3] from which appropriate resistors are switched into the circuit and if the switches are activated by a switch driving digital word (or code), then a digitally programmable integrator may be obtained.

In this paper, we describe an active-RC integrator structure with the above features. Other additional advantages are use of a single grounded capacitor, realizability of extremely large K involving product of resistor-ratios (possibility of square law enlargement) and the dual-input capability. Although several single-ended inverting/noninverting structures have been reported [5]-[8], a large time constant single grounded capacitor tunable dual-input integrator is not yet available in the literature.

We examined the performance of the proposed integrator under both continuous and digital T_o-control schemes. For digital control, we used a binary weighted PRA that was connected appropriately by CMOS (CD 4066) switches. The switch driving digital code had been derived from SDA-UNI-01 microcomputer system based on Intel 8085 microprocessor. The integrator performance has been verified experimentally with square wave inputs and some test results on the digitally programmable dual-input characteristics are included.

The effect of the OA poles on the performance of the integrator at relatively high-frequencies has been examined. It has been shown that the integrator quality factor Q [9] is degraded at higher frequencies owing to OA poles. An appropriate high frequency Q-compensation scheme [10]-[12] by utilizing another matched OA has been presented. The proposed compensation design yields 1 : $|A|^2$ order of Q-improvement compared to 1 : $|A|$ obtainable in ref. [12].

2. Dual-Input Integrator

Analysis of the proposed network in Fig.1, assuming high-gain (A >1) OA yields

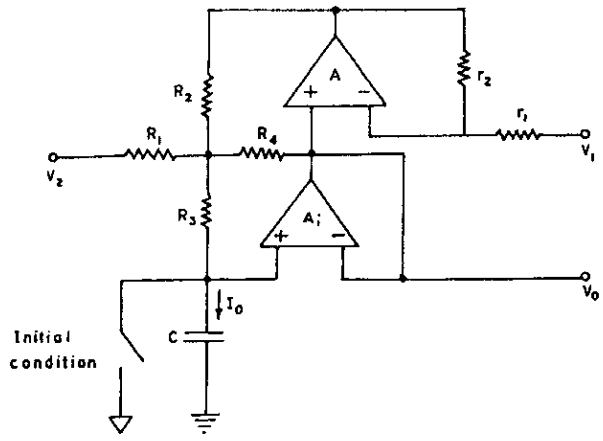


Fig. 1.
Dual-input integrator

$$V_o\left[sCR_3\left\{1+R_1\left(\frac{1}{R_2}+\frac{1}{R_3}+\frac{1}{R_4}\right)\right\}+\left\{1-\frac{R_1r_2}{R_2r_1}\right\}\right] =$$

$$= V_2 - V_1\frac{r_2R_1}{r_1R_2} \tag{1}$$

The realizability condition for a dual-input integrator in eqn (1) is

$$\frac{R_1}{R_2}=\frac{r_1}{r_2} \tag{2}$$

This gives

$$\frac{V_0}{V_2-V_1}(s)=\frac{1}{sT_0} \tag{3}$$

$$T_0=\frac{CR_1R_3}{R_x} \tag{4}$$

where $\frac{1}{R_x}=\sum\frac{1}{R_i}$; $i=1$ to 4 .

A simplified design equation is obtained by writing $R_1=R_2=R$, $R_3=nR$ and $R_4=\frac{R}{\lambda}$; this gives

$$T_0=KT \tag{5}$$

where

$$K=1+2n+n\lambda;\ K>1$$

$$\text{for } n>0,\ \lambda>0 \tag{6}$$

and $T=RC$.

Thus a large value of the enlargement factor (K), involving the product of independently adjustable resistor ratios, can be designed which gives extremely large values of the integrator time constant without having to depend on large capacitors. Moreover, the designer has the flexibility to realize a square law-enlargement by conveniently selecting $n=\lambda$ which of course will necessitate ganged variation of two resistors.

Other advantages of network are use of a grounded capacitor [1],[6], ease of setting a desired initial condition, improved d.c. stability over conventional Miller integrator and possibility of realizing an alternate network function leading to a tunable Transconductance amplifier. Ease of setting the initial condition to an integrator is an advantageous feature when the integrator forms the functional building block of a differential analyzer. In the proposed configuration the initial condition may be introduced by connecting the capacitor's upper plate to a d.c. voltage (or to ground for reset) through a switch as shown in Fig.1. The conventional Miller integrator has a floating capacitor and the output and input pins of the OA may get shorted if such a switch is connected; but here the output remains always isolated from the input. Also, because of the floating capacitor in the Miller integrator, its d.c. stability is not adequate; stabilizing resistors in parallel to the capacitor are often used for stability improvement. In contrast, both the OAs in Fig.1 have their individual d.c. negative feedback paths, and they were seen to be fully stable under no signal (only d.c. bias) conditions. One of the OAs is used in voltage follower mode with hundred percent negative feedback that are now readily available in integrated form (LM 110). Some precision type OA chips (superbeta SN 7277 or low-offset SN 52108A) may also be chosen for this circuit.

Finally, the proposed configuration may alternatively be utilized as a tunable transconductance (G_O) amplifier with a grounded load if the load current (I_O) is considered as the output variable. The transfer relation may be expressed as

$$\frac{I_0}{V_2-V_1}=G_0=\frac{G_1G_3}{\Sigma G_i}\ ;\quad i=1 \text{ to } 4 \tag{7}$$

where the G's are the passive conductances used. Thus G_O is tunable independently by G_3 and G_4. The simplified design of $G_1=G_2=G$, $G_3=G/n$ and $G_4=\lambda G$ yields

$$G_0=G/(1+2n+n\lambda)$$

3. Sensitivity

We now consider the sensitivity characteristics of the proposed integrator. The response of such active circuits depend on certain undesired influences, e.g., component manufacturing tolerance and variation of ambient temperature during operation. The values of the network parameters deviate from their nominal design value as a result of these influences. The fractional change in the network parameter T_O (or G_O) may be expressed in terms of the sensitivity (S^{T_O}) summation and in terms of the incremental changes in the RC components, given by

$$\frac{\Delta T_0}{T_0}=\sum_{i=1}^{4}\left(S_{R_i}^{T_0}\right)\left(\frac{\Delta R_i}{R_i}\right)+\left(S_C^{T_0}\right)\left(\frac{\Delta C}{C}\right) \tag{9}$$

where S^{T_O} denotes the classical sensitivity figure defined by

$$S_{\mu}^{T_0} = \left(\frac{\mu}{T_0}\right)\left(\frac{dT_0}{d\mu}\right) \tag{10}$$

The various S^{T_0} sensitivities are given in Table-1. It may be calculated from Table-1 that

μ	$S_{\mu}^{T_0}$		$\lvert S_{\mu}^{T_0} \rvert$
	Nominal Design	Simplified Design	
R_1	$\dfrac{(1+\frac{R_3}{R_p})}{(1+\frac{R_3}{R_1}+\frac{R_3}{R_p})}$	$\dfrac{1+n+n\lambda}{1+2n+n\lambda}$	<1
R_2	$\dfrac{-1}{1+R_2(1/R_1+1/R_3+1/R_4)}$	$\dfrac{-n}{1+2n+n\lambda}$	<1
R_3	$\dfrac{1+R_1/R_p}{1+R_1/R_3+R_1/R_p}$	$\dfrac{2n+n\lambda}{1+2n+n\lambda}$	<1
R_4	$\dfrac{-1}{1+R_4(1/R_1+1/R_2+1/R_3)}$	$\dfrac{-n}{1+2n+n\lambda}$	<1
C	1		

Table1
Sensitivity Characteristics

$$\sum_{i=4}^{4} S_{R_i}^{T_0} = 1 \tag{11}$$

In monolithic or hybrid-IC technology components of the same kind track quite closely, that is, the fractional changes of all the resistances (and capacitances) will be the same, i.e.,

$$\frac{\Delta R_i}{R_i} = \frac{\Delta R}{R}; \qquad i = 1 \text{ to } 4 \tag{12}$$

Hence we can write

$$\frac{\Delta T_0}{T_0} = \frac{\Delta R}{R} + \frac{\Delta C}{C} \tag{13}$$

It is possible to obtain resistor and capacitor components with equal but opposite temperature co-efficient in thin-film technology. Hence we may finally obtain

$$\Delta T_0/T_0 = 0 \tag{14}$$

4. Digital Control

For digital control of T_O, we used a binary weighted programmable resistor array (BW PRA), as shown in Fig. 2, for the tuned components R_3 or R_4 (or both). Appropriate resistor combinations were then switched using CMOS (CD 4066) SPST switches which were controlled by a switch driving digital code generated by the microprocessor. The switching functions ϕ_i(i=1 to 4) are

$$\phi_i = \begin{cases} 1 & \text{ON} \\ 0 & \text{OFF} \end{cases} \tag{15}$$

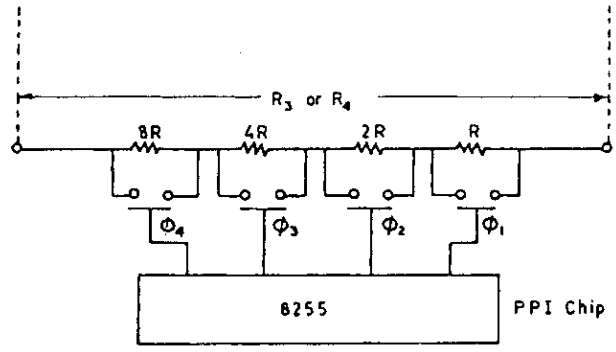


Fig. 2.
BWPRA for digital T_o control

The enlargement factor *(K)*, assuming $n = 1$ for simplicity and using a BWPRA for R_4, will be given by

$$K = 3 + decimal\left\{\bar{\phi}_4\bar{\phi}_3\bar{\phi}_2\bar{\phi}_1\right\} \tag{16}$$

The digital control of K and hence of T_O has been achieved by developing a suitable truth table for the switching function in eqn (16) that serves as the 4 bit switch driving code. To this end, we used the SDA-UNI-01microcomputer system based on Intel 8085 microprocessor. The code has been obtained from the B-port of 8255 programmable peripheral interface chip as in Fig. 2. In Fig. 3 we show the Flow-chart and the corresponding Assembly Language Program for the sequential generation (increasing from 1 r to 10) of the typical truth table as shown in Table-2. We also incorporated a Jump instruction and Delay subroutine and observed the generation of triangular waves changing slope (mV/ms) that appeared on the oscilloscope repeatatively. We designed a subroutine to provide a delay of about 6 sec. using the built-in 7.85 μsec of the microcomputer system. No distortion in these waves were observed during the execution of the program.

ϕ_4	ϕ_3	ϕ_2	ϕ_1	λ	K	T_o(ms)	Slope (mv/ms) Theo.	Slope (mv/ms) Prac.
1	1	1	0	1	4	4	900	891
1	1	0	0	3	6	6	600	594
1	0	1	0	5	8	8	450	447
0	1	1	0	9	12	12	300	282

Components : $R_1 = R_2 = 10$ kΩ, $C = 0.1$ μF.

Table2
Design for digital T_o - control in Fig.1 and some measured results

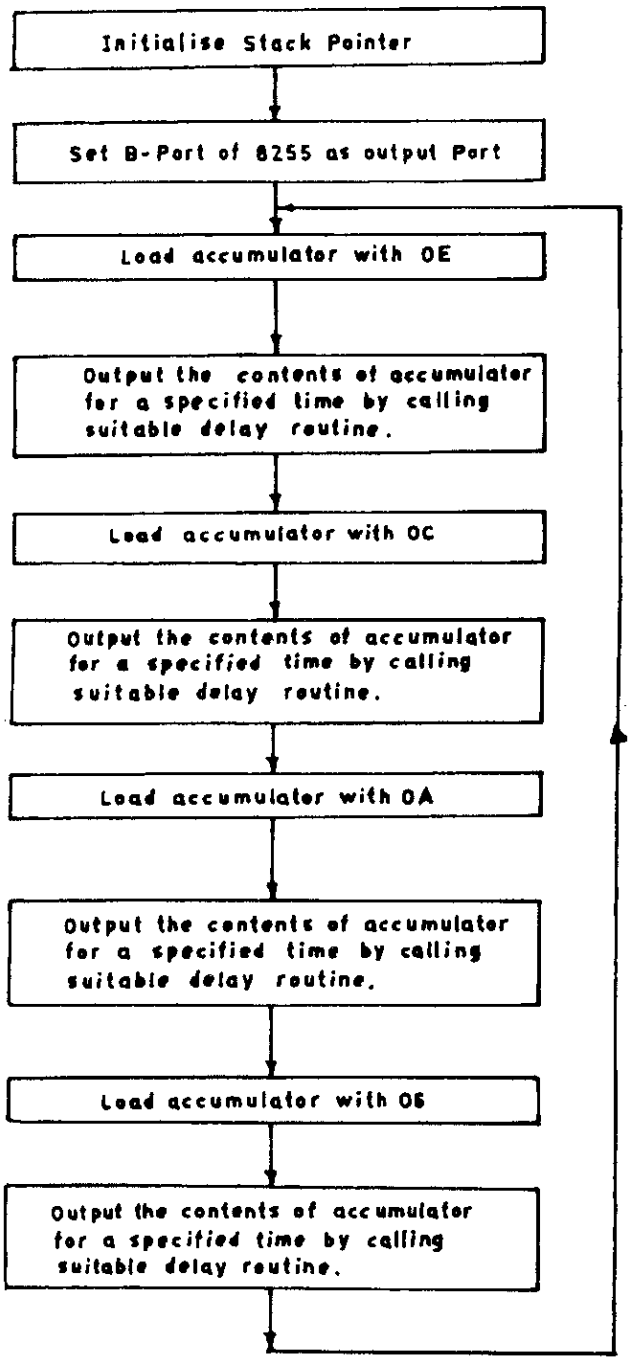


Fig. 3.
a) Flow chartEffect of OA-Pole

We now consider the effect of the OA-pole in Fig. 1 by writing $A = A_0/(s+\omega_1)$, where A_O is the open-loop d.c. voltage gain, ω_1 is the 3-dB corner frequency and $s = (j\omega)$ is the Laplace operator. For $\omega/\omega_1 > 1$, the OA gain can be represented by the one-pole model $A \approx B/s$ where $B(=A_0\omega_1)$ is the unity gain-bandwidth product.

```
LABEL     MNEMONICS          COMMENTS
          LXI SP, 2700H      : Initialise Stack Pointer
          MVI A, 00H
          MVI A, 80H         : Control word for Port B
          OUT 08H            : Address for control register
LOOP1 :   MVI A, 0EH         : Load accumulator with 0E
          OUT B
          CALL DELAY         : It provides a delay of about 5 sec.
          MVI A, 0CH
          OUT B
          CALL DELAY
          MVI A, 0AH
          OUT B
          CALL DELAY
          MVI A, 08H
          OUT B
          CALL DELAY
          JMP LOOP1
DELAY :   MVI B, 99
LOOP2 :   CALL DELAY1        : It generates a delay of 7.65
                               msec provided by the system
          DCR B
          JNZ LOOP2
          RET
```

Fig. 3.
b) Assembly Language Program

Analyzing Fig. 1 with the simplified design ($R_1=R_2=R$, $r_1=r_2=r$, $R_3=nR$ and $R_4=R/\lambda$) and thereafter substituting $A=B/s$, assuming for the moment that the buffer stage (A_1) consist of a wide-band device, we get

$$V_0 = \frac{V_2\left(\frac{2s}{B}+1\right) - V_1}{\left(\frac{2s^2T_0}{B}\right) + s\left(T_0 - \frac{4}{B}\right)} \tag{17}$$

Thus owing to the OA-pole, unequal input signal transmission occurs; however, for $\omega < B/2$ one gets a true dual input feature.

Next, the effect of the OA-pole on the integrator-Q [9] can be evaluated from (17) by writing the uncompensated transfer function (G_u) in the form

$$G_u(\omega) = \frac{1}{A(\omega) + jB(\omega)} \tag{18}$$

The Q may be written as

$$Q = B(\omega)/A(\omega) \tag{19}$$

Combining these expressions one gets the uncompensated $Q(Q_u)$ as

$$Q_u \approx |A|/2 \tag{20}$$

5. Q - Compensation

The proposed Q-compensation design scheme is shown in Fig. 4. Writing $A = B/s$ and assuming a pair of matched OAs (e.g. LM 747), we get

$$V_0 = \frac{V_2(2s^2 + sB + uB^2) - V_1(sB + B^2/2)}{2s^3T_0 + s^2(BT_0 + 4) + usB^2T_0 + B^2(2u - 1)}; \quad (21)$$

$u = r_b/(r_a + r_b)$

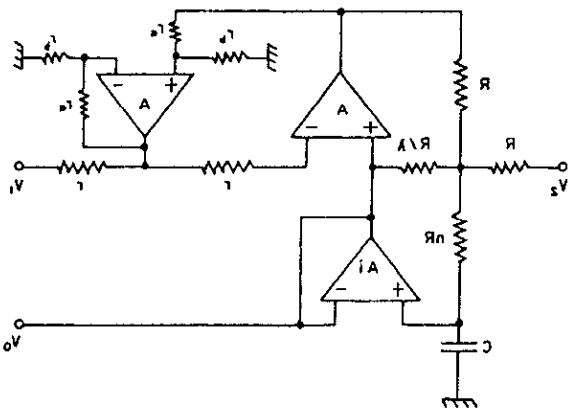


Fig. 4.
Q-compensation Scheme

Assuming $\omega < B\sqrt{u/2}$ and making $T_0 > \frac{4}{B}$, we obtain the compensated - $Q(Q_C)$

$$Q_c = \frac{u^2}{2b^3}\left\{\frac{1 - (b/u^2)(2u-1)[(1/\omega T_0) + (\omega/B)]}{\left(\frac{u-\frac{1}{2}}{BT_0b^3}\right) - 1}\right\} \quad (22)$$

where

$$b = \omega/B \quad (23)$$

The desired Q-compensation design is

$$u = 1/2\,. \quad (24)$$

This gives the quality factor (Q_C) of the compensated true dual-input integrator for $\omega < B/2$ as

$$Q_c = \left(\frac{|A|}{2}\right)^3 \quad (25)$$

Thus the enhancement factor Q_C: Q_u is proportional to $|A|^2$. The compensated transfer function of the dual-input integrator of Fig. 4 for $\omega < B/2$ may be obtained from (21) as

$$G_c(s) = \frac{V_0}{V_2 - V_1} = \frac{(2s/B) + 1}{sT_0\left[\left(\frac{2s}{B}\right)^2 + \left(\frac{2s}{B}\right) + 1\right]} \quad (26)$$

The phase error (ϕ_e) of the compensated network can be derived to be

$$\phi_e \cong \arctan\frac{1}{|Q_c|} \quad (27)$$

The non ideality of the input buffer amplifier (A_f) would introduce another pole, which lies at $B_f/2$. Its effect can be avoided by choosing a wide-band device (LF 356 : B_f=5 MHz) for A_f with respect to the main amplifiers A(LM 741 or LM 747; B=1 MHz). Fast integrated voltage follower chips are readily available now (LM 110).

6. Stability Analysis

The stability analysis can be carried out by taking into account the second corner frequency (ω_2) of the OA device. The OA-gain A(s) is now expressed as

$$A(s) = \frac{B\omega_2}{(s + \omega_1)(s + \omega_2)} \quad (28)$$

Re-analysis of Fig. 4 with (28) yields the necessary condition for the integrator stability as

$$\frac{\omega_2}{B} > (2u - \frac{1}{4}) \quad (29)$$

Combining (24) and (29), the condition for stability reduces to $\omega_2/B > 3/4$. This makes the integrator of Fig. 4 inherently stable since $\omega_2 > B$. A practical design can be obtained using the readily available matched dual-OA (LM 747) element with typical device parameters of B=1MHz and f_2= 2 MHz.

7. Experimental Results

The proposed integrator had been built using LM 747 dual-OA chip. Experimental verification of integration function with both continuous and digital control of T_O has been carried out first in single ended mode with symmetrical square wave inputs of 3.6 volts and 1.0 m sec period with continuous tuning. To ensure $R_f/R_2 \leq r_f/r_2$, we selected r_2=R_2, r_f=R_f and then connected a small resistance (δr_1) in series with r_f.

For square-wave testing of Fig. 1 we used the input signals V_2 = - V_1 = 5 Volts. A typical design of T = 2.5 nF x 10 kΩ and n = 1 with λ = 1 to 10 variable had been used. With continuous tuning of T_O, expected variation of the slope (S) of the rising/falling edge of the output triangular wave form was observed. The response of the compensated integrator at frequency of 100 kHz is shown in Fig. 5 with $T = 25\mu s$, $n = \lambda = 1$, i.e., T_O= 100 μs.

Digital control had been verified with suitable design as in Table-2. Wherein the typical switching function combinations were generated by the microprocessor as described earlier. Discrete variation in the slope (s) of inverting/noninverting triangular wave output was observed and measured as indicated in Table-2.

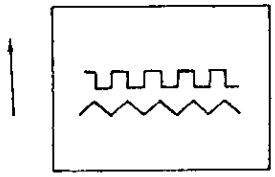
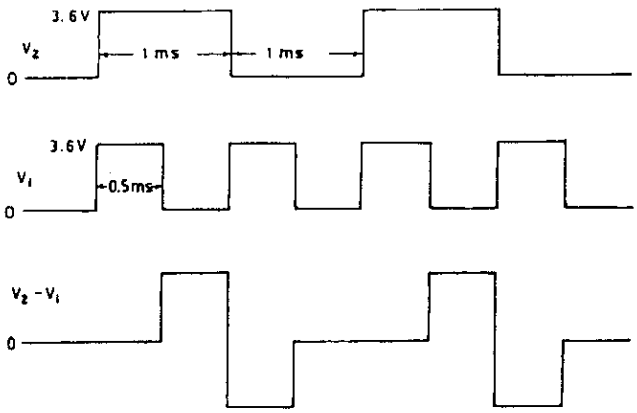
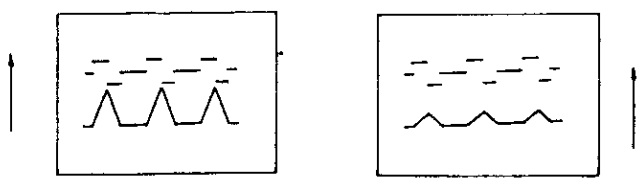


Fig. 5. Compensated integrator response with square wave input.
Horizontal scale 5 sμ/div.
upper trace: input wave, vertical scale 10 V/div
lower trace: output wave, vertical scale 0,5 V/div

Finally, we verified the differential mode function by simultaneous application of two square wave inputs of same magnitude but of different periods of V_2 and V_1. Wave-forms for V_1, V_2 and $(V_2\text{-}V_1)$ are sketched in Fig. 6(a) while Fig. 6(b) and (c) show the experimental response of the dual input integrator for different time constant settings obtained by adjusting n and then λ digitally.



a)



b) c)

Fig. 6.
Response of dual-input integrator with digital control.
(a) Input waveforms V_1, V_2 and $(V_2\text{-}V_1)$
(b) Response at $\phi_4\phi_3\phi_2\phi_1$= 1110
(c) Response at $\phi_4\phi_3\phi_2\phi_1$= 1100

The frequency response of both the uncompensated and compensated networks were measured with a differential mode of $V_2 = -V_1 = 1 \sin \omega t$ (volts). The measured response for the phase error (ϕ_e) is shown in Fig. 7.

It may be seen in Fig. It has been observed during experimentation that when the proposed integrator was operated in a single ended non-inverting mode (V_1=0), excellent compensation had been achieved and the usable frequency range extended upto about 750 kHz. This result is also shown in Fig. 7 where b is the phase error in differential mode and c is that under noninverting mode.

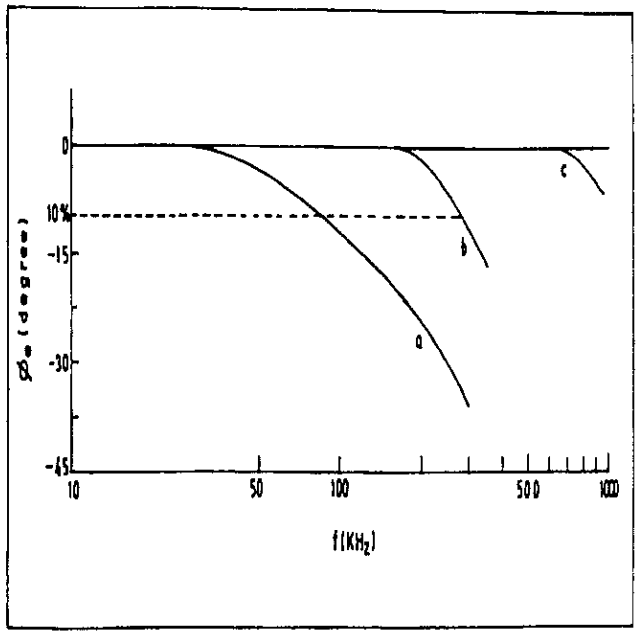


Fig. 7.
Measured phase response
a - uncompensated
b - compensated dual-input
c - compensated noninverting

8. Conclusion

The novel active-RC integrator is described whose novelties are:

(i) realizability of ideal integrator network function with dual-input capability.

(ii) use of extremely low valued grounded capacitor.

(iii) enlargement of time constant over that obtainable by the nominal RC products by an enlargement factor K>1 where K is single-resistor double-multiplier extendable.

(iv) availability of alternate network functions, viz., integrator or transconductance amplifier.

(v) improved d.c. stability and ease of incorporating initial conditions; low component sensitivity $S^{T_0} \leq 1$.

(vi) design flexibility to continuous/digital T_0 control.

(vii) Analysis shows that the integrator becomes nonideal at relatively high frequencies owing to the OA poles. An appropriate Q-compensation design scheme has then been proposed, by which 1: $|A|^2$ order of Q-enhancement is possible. The integrator has been tested in the laboratory and the performance of both the uncompensated and the compensated circuits was measured. These results, showing the predicted improvement, are presented.

9. Acknowledgement

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