An Optical Carry Chain Fast Adder

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Abstract

A significant problem in Arithmetic Unit design and particularly for systolic arrays remains the speed attainable in achieving high speed addition. The root of the problem is carry propagation and a method is presented which is relatively independent of word length.

The problem is addressed by the description of a suggested radical design involving a hybrid optical and electronic approach. The method of carry chain addition through pass gates is explained and a suggested implementation utilising Fabry-Perott resonators, optical waveguides and voltage controlled couplers is described. The design is suitable for n-stage modular expansion.

Keywords:

Systolic arrays, Look ahead carry, Pass gate, Fabry-Perott resonators,Optical waveguides,Optical couplers.

1. Introduction

The adder is a fundamental circuit in arithmetic units in central processors and in more specialised systolic array implementations. The basic binary adder which computes the sum of single bit numbers is described by the logic equations:

$$s_i = x_i \oplus y_i \oplus c_{i+1} \quad (1)$$

and

$$c_i = x_i y_i + x_i c_{i+1} + y_i c_{i+1} \quad (2)$$

This functionality can be implemented as a two level realisation but combining these full adders to yield an n-bit addition requires the inclusion of carry in and carry out facilities. It is simple to accommodate the carry by ripple through action but this is an insufficiently fast technique particularly for systolic array processor elements. The general strategy for designing high speed adders is to tackle the issue of carry propagation. Typically, the solution involves determining the input carry of stage (i) directly from the inputs of the preceding stage. This creates a "look ahead" carry action. In this option each adder produces a "carry generate" (g) and a carry propagate (p) signal. An ancillary two level look ahead carry circuit produces carry inputs to each bit adder. The carry generate and carry propagate functions are defined as:

$$g_i = x_i y_i \quad (3)$$

$$p_i = x_i \oplus y_i \quad (4)$$

The carry signal forwarded to the i-1 stage is defined as follows:

$$c_i = g_i + p_i c_{i+1} \quad (5)$$

The carry in may be expressed as a sum of products of the (p) and (g) outputs of preceding stages. The carry of bit 0 in a four stage carry lookahead adder are:

$$c_0 = g_0 + p_0 g_1 + p_0 p_1 g_2 + p_0 p_1 p_2 g_3 + p_0 p_1 p_2 p_3 c_{in} \quad (6)$$

The complexity of the carry generate equations increases with the number of stages and it is generally considered practical to limit the number of carry lookahead stages to a maximum of eight. Conventional approaches thus deal with large word sizes by carry propagation between groups of up to eight bits. This compromise does not overcome the basic problem of ripple through carry propagation. Derivations of the standard equations occur in Hayes [1]

2. An enabling addition method

The objective is to create an addition implementation method which is not constrained by ripple through actions and which operates with a single gate delay between input and output. The first step in acheiving this is to develop a sympathetic technique. The proposed method will be described by algorithm and example. Consider two eight bit numbers, x and y. The numbers are assigned arbitrary values:

$x = 01001111$

$y = 01101001$

Two concurrent logic operations are then performed. In one case x is bit-wise ANDED with y to create a new variable A.

A= 01001001

In the other case a new variable B is obtained by bit wise XOR of the the two original variables x and y.

B= 00100110

With the two new variables A and B aligned by column the process begins at the least significant end of the "A" word. The word is scanned toward the most significant end until a "1" is found. The "1" is transferred left until the next column of "B" contains "0" when it projects down to the result. Every column between a "1" in "A" and the next "0" in "B" inclusively is said to be within the *shift span*. All the bits within the shift span are ANDED to generate the result as shown below.

```
bit   7 6 5 4 3 2 1 0
A=    0 1 0 0 1 0 0 1
B=    0 0 1 0 0 1 1 0

sum   1 0 1 1 1 0 0 0
```

Outside the shift span, bits in the two variables "A" and "B" are ORed. Bit 5 in the example sum illustrates. In mapping this algorithm in circuitry the concurrency of the basic operations indicate that a single gate level is required. The shift left and transfer of "1" bits in "A" is an additional necessary feature that might be implemented in conventional VLSI. The simplest suitable device is the "pass" transistor but regrettably the propagation delay through the chain necessary for large word size calculations negates the speed advantage of the system.

3. Suitable optical devices

Berra et al [2] describes the Fabry-Perott resonator. The device is illustrated in Figure 1. The device is constructed by sandwiching a non linear electro-optical material, typically Lithium Niobate ($LiNbO_3$) between two partially reflective mirror surfaces. With correct relationships between the mirror surface spacing and the wavelength of the optical signal being passed throught the device, the mirror surfaces will be transparent. Changing the apparent spacing by altering the index of refraction of the material between the mirror surfaces results in a "blocking" action. The refractive index of Lithium Niobate may be altered by the application of a control beam as shown. The switching speed of such optical devices is reported as less than 1 picosecond. The details of light operated bistable switches similar to, or based upon the Fabry-Perott device are described in Gibbs et al [3] and Warren et al [4]. The Fabry-Perott device or derivatives such as the etalon [3] are appropriate for an optical carry chain. One device is required for each adder bit and when used in conjunction with an optical waveguide formed by sputtered glass on Silicon Dioxide film over Silicon a practical VLSI implementation is apparent.

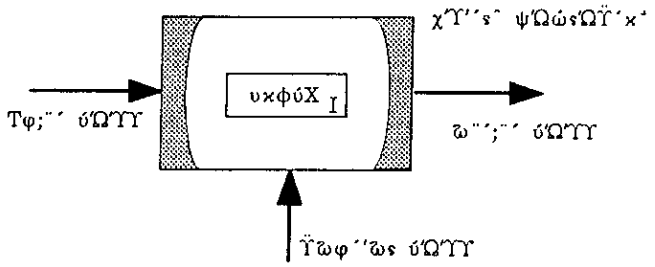

Fig. 1
Fabry-Perott resonator

Two other devices are necessary, one of which is a straightforward CMOS optical receiver such as that shown in Figure 2.

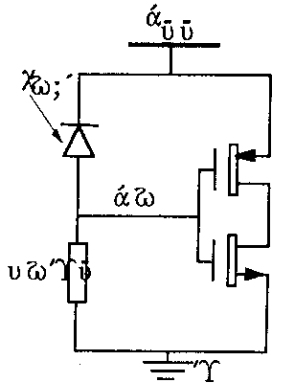

Fig. 2
CMOS receiver

This receiver translates light signals into electrical signals for the final output stage. The second necessary function is electrical to light signal translation. The design requires an electrically switchable Fabry-Perott control beam for each adder bit position. Whilst it is possible to use individual diode lasers or light emitting diodes, the preferred and most cost effective option is to use a single source and distribute a source beam via integrated optical waveguide with two voltage controlled optical couplers at every bit position. A suitable device is that described by Alferness[5]and is illustrated by Figure 3. This approach creates an controllable optical signal generator which is used by the logic that creates the A and B variables of the addition algorithm. The interconnection and geometry of the optical signal generator is shown in Figure 4.

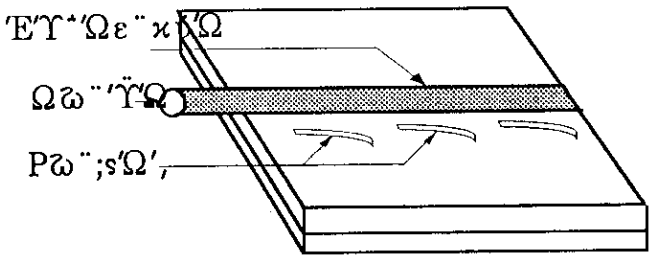

Fig. 3
Optical signal generator

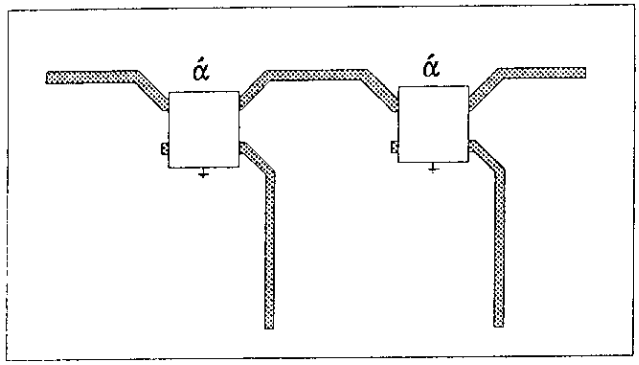

Fig. 4
1 bit section

4. System and action

The arrangement of a 4-bit adder module appears in Figure 5.

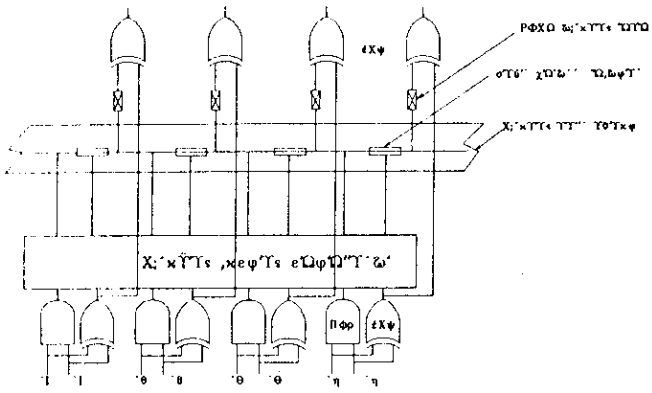

Fig. 5
4 bit adder module

Original binary numbers for addition are applied at inputs x and y. AND and XOR gates in parallel generate the A and B variables described in section 2 above. B bits control their associated Fabry pass gates in the optical carry chain via voltage operated couplers in the optical signal generator. If an A bit is "1", the output of its generating AND gate creates an "on" beam via the second voltage controlled coupler. The beam is injected into the optical carry chain prior to the following bit pass gate. Whether the A bit "1" is propagated depends upon the state of that following pass gate. Since pass gate states are controlled by B bits, an injected signal is propagated leftwards until encountering a "0" B bit. The process used to generate A and B from x and y ensures that a given bit in A cannot have the same state as that bit in B. This allows the use of XOR as the output function for each bit instead of the AND/OR action prescribed by the algorithm. Figure 6 demonstrates the action using the least significant 4 bits of the example values for A and B. In the simplified figure, a "1" at an AND gate output implies a light beam injected into the carry chain. Input XOR "1" outputs switch on the carry chain pass gates, whilst "0"s render the pass gates off or blocking. The output XOR gates have associated B bit inputs together with an input derived from the optical carry chain via CMOS optical receivers such as are illustrated in Figure 2. The Fabry-Perott pass gates all receive their control inputs simultaneously resulting in a minimised set up time for the chain.

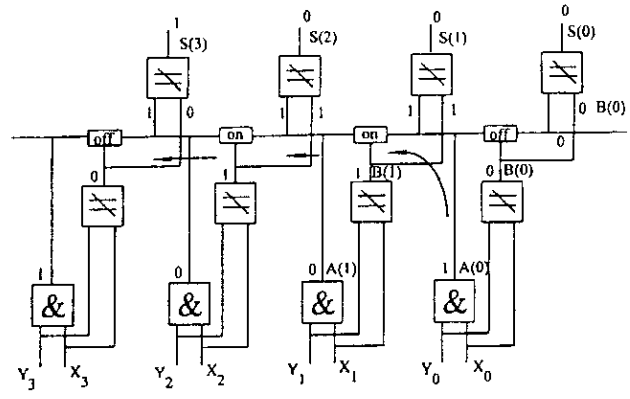

Fig. 6
System Actions

5. Conclusions

The inherent parallelism in the generation of A and B variables, together with the simultaneous set up of the pass gates result in a very high speed performance. Current technology can produce gate delays of around 1 nanosecond. Assuming 4 gate delays inherent to an XOR function the overall delay in the appearance of the sum outputs will be:

8 gate delays+1	coupler switching time+1
optical receiver+1	Fabry-Perott resonator delay.

Typical coupler switching times are around 0.2 nanoseconds with Fabry devices operating in sub 1 nanosecond and optical receivers producing outputs in about 2.3 nanoseconds. The total delay predicts potential operation at around 1 GHz. The most important feature of the design is the ability to cascade adder modules with insignificant increased delay for any word size. Extra overheads are solely contributed by the greater length of the integrated optical waveguide forming the extended carry chain. Implementation requires hybrid optical and

electronic circuits in VLSI. Granestrand et al [6] report 64 couplers with DC voltage control implemented in a single chip 60mm in length, whilst Ventkatesan et al [7] claim Fabry-Perott resonator fabrication in 9 micrometer square. It is concluded that fabrication of hybrid adder modules using the principles described could be achieved in VLSI. The considerable speed available would particularly enhance the performance of systolic array processing elements, allowing their application to signal and image processing of high bandwidth data in real time.

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