GRAY CODE ADC BASED ON AN ANALOG NEURAL CIRCUIT

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Abstract

In this paper a new neural ADC design is presented, which is based on the idea to replace all functional components needed in the ADC block scheme by a simple connection of neurons. Transformation of ADC functional scheme into an analog neural structure and its computer simulation is one of the main results of this paper. Furthermore, a discrete component prototype of the proposed A/D converter is discussed and experimental results are also given.

Keywords:

AD converter, Gray code, Neural networks.

1. Introduction

Many of methods for ADC design, based on analog neural networks, have been developed after first proposal by Hopfield [1]. The suppression of spurious state presence in the Hopfield's proposal, caused by local minima, has been always the main aim in all the successive published works [2]. A great accuracy of A/D conversion is the second aim, which is followed simultaneously, in these designs. A number of new architecture were developed to fulfil the first aim [2], [3] The circuit design of these structures exploits some characteristic properties of chosen output code.

One structural scheme of N-layers perceptron with output Gray code was designed in the [3]. The only problem of this proposed structure is the utilisation of a voltage controlled switch and a comparator not present in the set of neural building blocks. Each neural structure consits only from the building blocks such as multiplicator by constant, summing block and sigmoidal transfer functional block.

The other problem caused by the switch in the proposed architecture [3] is the occurrence of indefinite states during the switching transient phase.

To overcome these disadvantages, in the following, an improved neural based ADC design is shown which starts from a functional structure requested for. the realisation of the AD conversion with the output Gray code. The functional structure is transformed on the cascade of single bit stages, realised only with neurons and weighted connections among them. This architectures offers a circuit which is very simple for the realisation owing to identical stage structure. The final association of output summing operation with a similar operation of succesive stage creates a very compact neural based ADC which transfer characteristic can be easily modified for different transfer functions.

In this paper, after a description of proposed neural ADC design approach, a discrete component implementation is given,as are the experimental results and dynamic performance.

2. New design method of N-layers perceptron for Gray coded ADC

In analog neural networks all computational and decision operations are realisable in analog form by the networks of basic neural components. The new approach starts from the sophisticated connection of functional blocks which are able to convert the input signal into the output digital Gray code by analog operation with input signal. The output code is represented by the states of the output signals at the single blocks.

The symmetricalness of i-th binary digit shapes around each change on the neighbourhood of $(i+1)$-th digit line is a characteristic Gray code feature. Symmetrical shape with decreasing period in direction to the lower bits is another important property of this code. In general, each functional stage changes the continuos shape course of its input voltage doubling its frequency.

The proposed neural ADC (Fig.1) is based on a cascade of N functional stages linked in series. Each stage

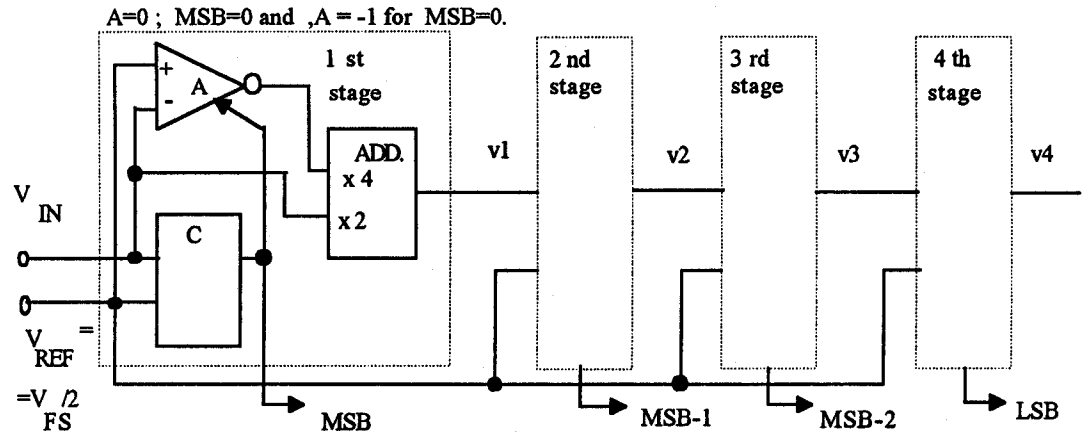

Fig. 1
Functional block-scheme.

consists of: (i) a comparator (C), (ii) an amplifier with controlled gain (A), and (iii) an adding block (ADD). By means of the comparator of the first stage, the input signal V_{in} is compared with a reference voltage equal to $V_{FS}/2$, (V_{FS} is the full scale voltage). The digital output is also used to control the gain of the amplifier A. The gain will be equal to 0 if $MSB = 0$ and -1 if $MSB = -1$. In such a way, the functional operation carried out by the switch used in [3] is obtained, without commutation problems of the switch. Then, the output of the amplifier A and the input signal V_{in} are amplified and added in the adding block ADD. The output of the adding block is then applied into the input of the successive ADC stage. In order to normalise the value of the output signal of the stage to the full voltage scale, the analog input signal to the stage is amplified by factor 2 or -2, the corresponding digital output is 0 or 1 respectively.

The amplification -2 is obtained adding, in the block ADD, to the input signal amplified by 2 the same signal amplified by -4 received from the amplifier with controlled gain A.

In order to realise the neural ADC of Fig.1 only with neural building blocks, the amplifier A, the comparator C and the adding block ADD of each stage have been replaced with analog neurons. The neurons with common slope G of the sigmoidal transfer function are supposed.

The first block to be replaced is the comparator. Its main feature is its extremely high amplification. The weighting values in the transfer characteristics of neuron w_{CA}, and w_{CB} allow to adjust enough high slope of comparating characteristics (1) as well as to make one input as noninverting and other as an inverting one with mutual inverted signums of the weighting coefficients $w_{CA} = c$, $w_{CB} = -c$.

$$y = \frac{-1}{1 + e^{-Ga}} = \frac{-1}{1 + e^{-G(w_{CA}x_A + w_{CB}x_B)}} \qquad (1)$$

The second block to be replaced with analog neurons is the amplifier with controlled gain (A). It represents a parametrical nonlinear circuit and the variation of the amplification coefficient A is possible by the shift of the operational point along the sigmoidal transfer characteristics of the neuron. The high weighting coefficient w_C of control input x_C enables to shift the operational point significantly between points with amplification $A = -G/2$, for $x_C = 0$, and $A = 0$, for $x_C = -1$. In order to suppress the -0.5 offset value and the nonlinear distortion introduced by the sigmoidal transfer characteristics a parallel compensating connection of two neurons is carried out with its mutual inverse transfer function.

$$y' = \frac{-1}{1+e^{-Ga_1}} + \frac{1}{1+e^{-Ga_2}} =$$

$$= \frac{1}{2}\left[-\tanh(a_1\frac{G}{2}) + \tanh(a_2\frac{G}{2})\right] \qquad (2)$$

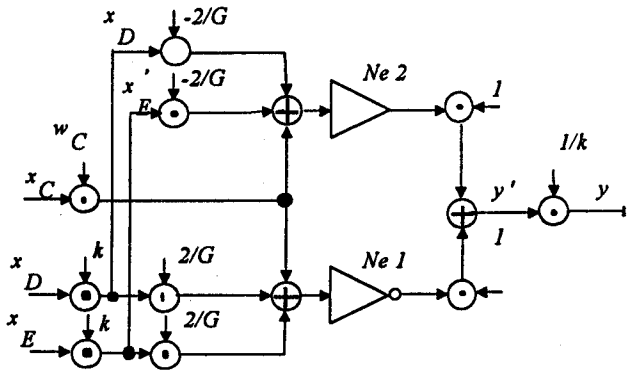

Fig. 2
Gain controled amplifier realised by neurons.

The activities a_1 of inverting neuron Ne1 and a_2 of noninverting neuron Ne2 for $x_C = 0$ are: $a_1 = w_D x'_D + w_E x'_E$ $a_2 = -w_D x'_D - w_E x'_E$.

The added output signal y' is a product of amplification of input signals x'_D and x'_E. To obtain a total amplification for the input signals x'_D and x'_E equal to -1, the synapses weighting coefficients w_D and w_E must be fixed to double of the reciprocal value of sigmoidal characteristics slope about inflexion point $wD = w_G = 2/G$ previous. The equation (1) can be rewritten in the form of McLaurin's series under condition of sufficiently small arguments $a_1\frac{G}{2} \le 4/\pi$ and $a_2\frac{G}{2} \le 4/\pi$.

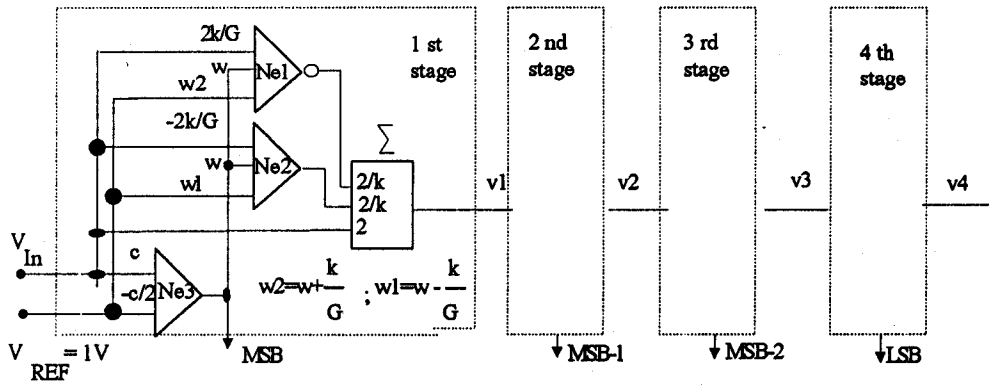

Fig. 3
Gray code ADC in form of 2N-layer perceptron.

$$y=\frac{1}{2}\Big[-\frac{G}{2}\Big(\frac{2}{G}x'_D+\frac{2}{G}x'_E\Big)+\frac{G^3}{3.2^3}\Big(x'_D+\frac{2}{G}x'_E\Big)-$$

$$-\frac{2.G^5}{15.2^5}\Big(\frac{2}{G}x'_D+\frac{2}{G}x'_E\Big)^5-\ldots\Big]+\frac{1}{2}\Big[-\frac{G}{2}\Big(\frac{2}{G}x'_D+\frac{2}{G}x'_E\Big)+$$

$$+\frac{G^3}{3.2^3}\Big(\frac{2}{G}x'_D+\frac{2}{G}x'_E\Big)^3-\frac{2.G^5}{15.2^5}\Big(\frac{2}{G}x'_D+\frac{2}{G}x'_E\Big)^5+\ldots\Big] \qquad (3)$$

The linear component of y for the control input value $x_C=0$ is equal to $A=-1$. The nonlinearity of the resulting transfer function is a distortion source of the input signal. The only way to suppress the nonlinear distortion to the requested level is to make the signals x_D and x_E small in order to be in narrow surrounding of the inflexion point.. This aim is achieved by multiplying the signals x_D and x_E with coefficient $k<1$. The expanding of the output signal from the neuron with the reciprocal constant $1/k$ is a needed complementary operation. The output signal y for the resulting neuron assembly which replaces the controlled amplifier can be described by the equations:

$$y=0 \quad \text{for} \quad x_C=-1,$$

$$y=-(x_D+x_E)+\frac{k^2}{3}(x_D+x_E)^3-\frac{2k^4}{15}(x_D+x_E)^5\ldots$$

$$\text{for} \quad x_C=0, \qquad (4)$$

The coarse estimation of the value k follows the idea of significant reducing of the components with higher power. The deal of the nonlinear distortion components in (4) will be under 1% when the condition (5) is fulfilled.

$$\frac{k^2(x_D+x_E)^2}{3}-\frac{2k^4(x_D+x_E)^4}{15}<0.01 \qquad (5)$$

The maximal value of the input signal is $(x_D+x_E)_{max}=V_{FS}=1$. The resulting value of the coefficient k is $k=0.0575$ in the case.

The functional scheme (Fig.1) is transformed into structure shown on Fig.3.

The third block to be replaced is the adding block ADD. In this case the task of the block has been accomplished by the neuron adding capability. This transformation is the final step in the proposed design approach. The resulting neural structure for A/D converter with output Gray code is in Fig.4. The value of each synapses weight is determined by a multiplication of all weights on the path from the relevant neuron input to the corresponding neuron output . As an example we can show the determination of synapses value T_{93}. The path from the input of neuron Ne 1 of the third stage with weight $2k/G$ is going from the adding block with amplification 2 in the second stage and throw the adding block ADD with amplification 2 in the second stage and throw its adding block ADD with the amplification $2/k$ in the first stage to the output of neuron Ne 2 in first stage. This synapses weight value represents, in the

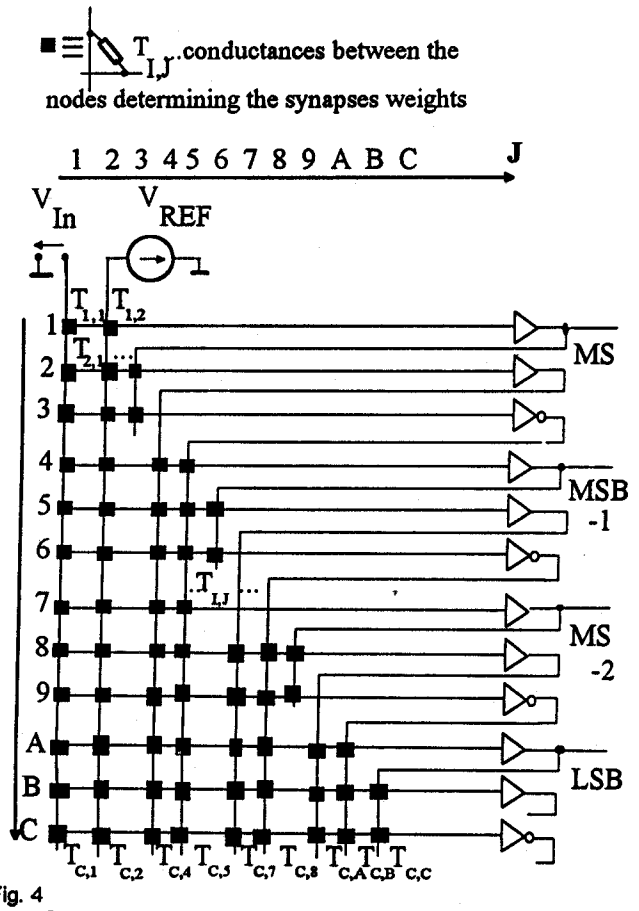

Fig. 4
Gray code ADC in form of 2N-layer perceptron.

I,J	1.00	2.00	3.00	4.00	5.00	6.00	7.00	8.00	9.00	A	B	C
1.00	c	c / 2										
2.00	-2k / G	-w_cc1	w									
3.00	2k / G	-wc2	w									
4.00	2c	c / 2	0.00	2c / k	2c / k							
5.00	-4k / G	-wc1	0.00	-4 / G	-4 / G	w						
6.00	4k / G	-wc2	0.00	4 / G	4 / G	w						
7.00	4c	c / 2	0.00	4c / k	4c / k	0.00	2c / k	2c / k				
8.00	-8k / G	-wc1	0.00	-8 / G	-8 / G	0.00	-4 / G	-4 / G	w			
9.00	8k / G	-wc2	0.00	8 / G	8 / G	0.00	4 / G	4 / G	w			
A	8c	c / 2	0.00	8c / k	8c / k	0.00	4c / k	4c / k	0.00	2c / k	2c / k	
B	-16k / G	-wc1	0.00	-16 / G	-16 / G	0.00	-8 / G	-8 / G	0.00	-4 / G	-4 / G	w
C	16k / G	-wc2	0.00	16 / G	16 / G	0.00	8 / G	8 / G	0.00	4 / G	4 / G	w

Tab. 1
Conductances $T_{I,J}$ in the final analog neural circuit for Gray code AD conversion.

corresponding analog neural structure at Fig.4, the conductivity between the input of the neuron Ne 1 of the third stage and the output of the neuron Ne 2 of the first stage. The final connection matrix is lower triangular.According to [2] the A/D converter has no "spurious states".

The structural scheme Fig.4 is achieved from the cascade scheme Fig.3. by the replacing the summing block only. The resulting transfer function and error features of those both types are identical for this reason.

The resulting values of the conductances in the final neural structure designed for AD conversion with Gray output code are shown in the Tab.1.

3. Simulation and Circuit Realisation of the Proposed A/D Neural Converter

The behaviour of .the proposed neural A/D converter (Fig. 4) was studied by PSPICE simulating software package. The digital output values from each level were studied with help of DC analysis of linear change input voltage. The output file from the simulating program with PSPICE, together with software package PROBE, was used also for the evaluation of the transfer characteristics error from the non-linear distortion. .

The neuron is modelled by functional block with ideal sigmoidal function of its transfer characteristics. The sum of weighted signals at the input of each neuron is obtained by utilising conductances T_{ij} connected to low input impedance of each neuron as shown in Fig.4. The neuron time behaviour has been represented with a parallel RC circuit connected on its input. The input voltages V_{in} of neurons programmed as the comparators gained from the computer simulation are shown in Fig.5. The comparing neuron output level V_{out} represents relevant bit of the output Gray code (MSB,MSB-1,..LSB) in the neural network Fig.4. in accordance to the relations $V_{out} = H$ for $V_{in} > 0$ and $V_{out} = L$ for $V_{in} < 0$. The similarity of input voltage V_{in} to the triangular folded shape secures high accuracy of A/D transfer characteristics.

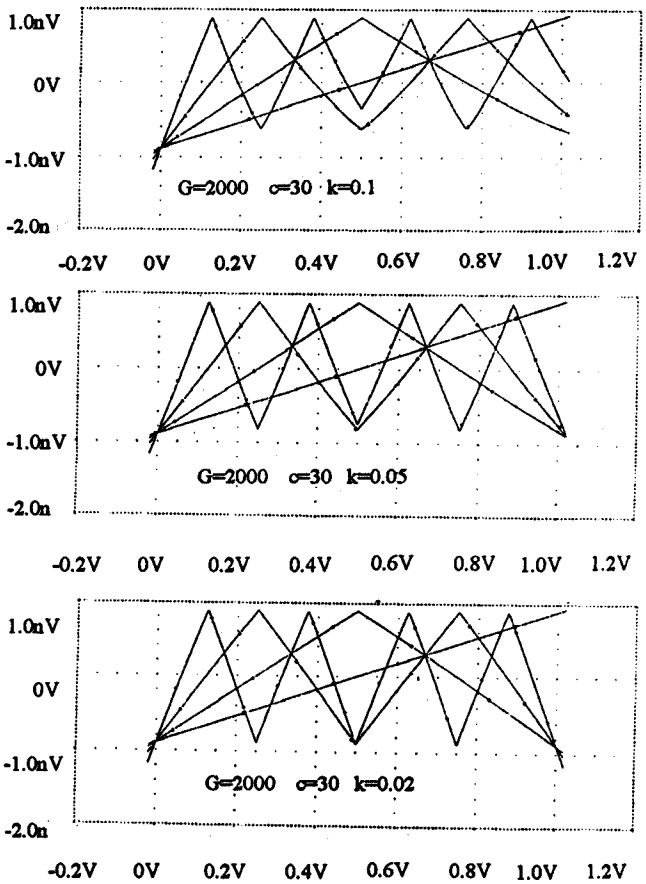

Fig.5.
The comparing neurons input voltages V_{in} for different values of k

The simulation of developed ideal neural scheme shows its high sensitivity to the coefficient k for certain number of bits N. The decrease of nonlinear distortion produced by the decrease of k , increases the noise - signal ratio at the neuron inputs. Comparison of the impact from the noise impulses generated on the supply lines for different ADC neural structures was an other study task. The computer simulation of noise interference is not very representative because of information lack about several parasitic components caused by these effects. The only way to evaluate possible structure behaviour in dynamical mode was its experimental testing. In order to carry out the experimental testing of a circuit prototype a simple assembly 8 identical stages similar to structure Fig.3. for a whole ADC was simulated and realised. Fig.6 shows a structure of single stage. The simple neuron based on the operational amplifier was designed to obtained the neuron with low nonlinear distortion. The transfer characteristics of proposed circuit structure is piece-wise linear in this case. The synapses weights have been obtain with help of input resistances. The neuron with high weighting coefficients is created with help of integrated comparator.

A dominant request in the circuit design was the accuracy rules for obtaining the value of the differential nonlinearity DNL of converter transfer function $DNL < 0.5U_{LSB}$. The transfer characteristics of each stage is determined by resistors with high accuracy and with the low temperature coefficients. Moreover, the parasitic temperature dependence is suppressed with compensating circuit design. Here, the input resistors and the feedback resistors with the same value, same metal-thin hybrid technology on the same substrate and with the same temperature feature of merits have been utilised. Each voltage to be added in the neuron and the adding point input is derived from one common etalon voltage source, that is the same for all stages. The comparator and operational amplifier with low value of offset, corresponding to the equation , have been requested. The value of output voltage of each stage equal to V_{FS} for input

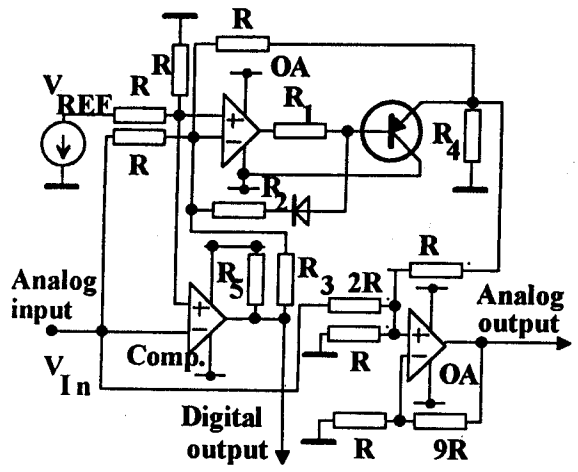

Fig.6
The single stage circuit scheme of the cascade neural Gray code ADC (Fig.3).

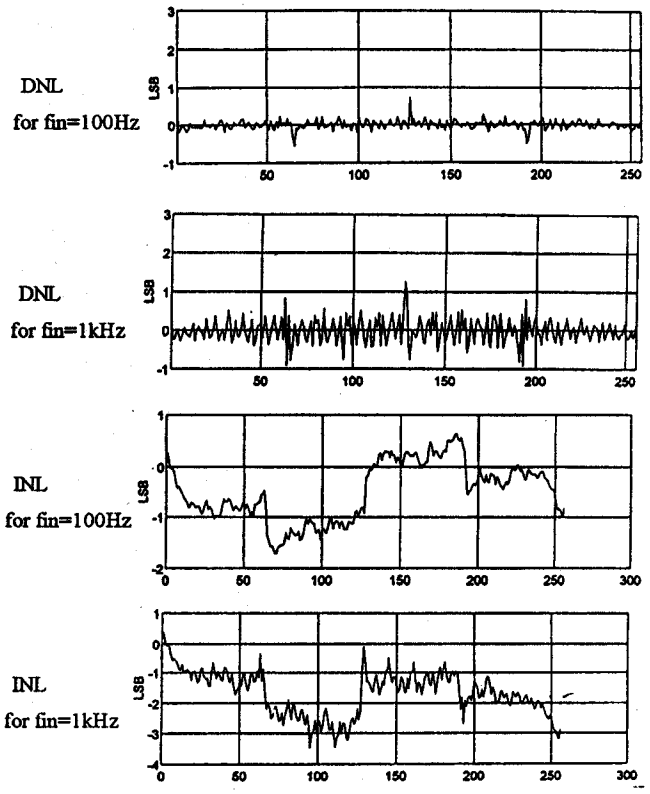

Fig.7.
Measured DNL and INL of the Gray code ADC in form of 8-bit perceptron

voltage equal to $V_{FS}/2$ is adjusted by resistor R27 (Accuracy =1% and Tempco=10 ppm.). The output voltage equal 0 for the input voltage V_{FS} is adjustable by resistor R10 (Accuracy=1% and Tempco= 20 ppm) at the each stage. Error of first stage is multiplied by next - going stages and has main impact on total error characteristics.

Several evaluation tests of assembled Gray coded ADC prototype were conducted. Histogram method was applied as the basic testing method . The processed samples were acquired from the ADC output by a fast digital interface. The precision harmonic signal source connected to the ADC input was utilised as a test generator. The testing procedure was applied for different values of testing signal frequencies. The acquired histogram allows to determine many characteristic feature of merit .

The Fig.7. shows the resulting differential nonlinearity coefficient DNL(k) and the integral nonlinearity coefficient INL(k) computed from the acquired histogram for a different frequencies of a harmonic input testing signal.

Measured DNL is represented by a sum of errors belonging to the single bits in the output Gray code. This behaviour is characteristic for successive approximation ADC, where the occurrence of single error components along the input axes is a periodical function. [7],[8]. The DNL(k) error function is periodical along the axes representing binary expressed value of the output digital Gray code. The final dependence of DNL on the input

value V_{in} could be achieved after transformation of points from Gray expressed space into the natural binary space.

4. Conclusions

The electrically programmable neural networks are new comprehensive tool for optimisation and pattern recognition application. Such circuits are able to table continuous input signal into the set with final number of output classes, in accordance to the classification rule. This approach enables complex neural networks to work at extremely high speed , mapping analog input data into digital decision oriented output. Inputs and outputs are ideally adapted to real -world sensing because , like real world inputs are analog and final human decisions are discrete. The utilisation of commercial produced circuits [6] allows customer to prepare such classification system working in a real time very easily.

5. References

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