THE DCF77 DECODER - FAST CODE GENERATOR

Marek SKOTNICA
Academy of Sciences of Czech Republic
Institute of Geonics Studentská 1768, 708 00
Ostrava--Poruba, Czech Republic E-mail:
skotnica@ugn.cas.cz

Abstract

Signal of the DCF amplitude-modulated transmitter, located in Braunschweig (Germany) is widely used for synchronizing of time information during different laboratory and field experiments. The full time information of this time normal is coded and presented within every minute using different length of second time marks. The knowledge of the exact time of occurrence of seismic events is the fundamental information during the seismic activity monitoring. With respect to the fact that the duration of individual records having sometimes a few seconds at minimum, the time generator ensuring the complete time information within every second, is needed. That is why the special timing device controlled by the DCF77 signal and generating every second the full time information was developed. Description of the function of decoder, internal clock and fast code generator implemented on the basis of FPGA circuits is the subject of this paper.

Keywords:

DCF77 code decoder, synchronization, exact time measurement, fast code generator, FPGA circuit, shift register, parity generator, timer.

1. Introduction

The DCF77 code consists of 59 second time marks transmitted every minute, the last one representing the minute synchronization is missing. The beginning of the second is determined by the first edge of the second mark. If the length of the mark is approximately 100 ms, it means binary 0, then 200 ms mark represents in binary code 1. The full time information is BCD coded in last 23 bits of each minute. There are three parity bits for checking purposes. The detailed description of DCF77 code is given in 1.

2. Device block diagram description

As seen from Fig. 1, essential parts of *DCF77 Decoder -- Fast Code Generator* are: *decoder, internal clock* and *fast code generator*.

The *decoder* consists of a *time signal decoder*, a *phase decoder*, an *input shift register*, a *parity and format*

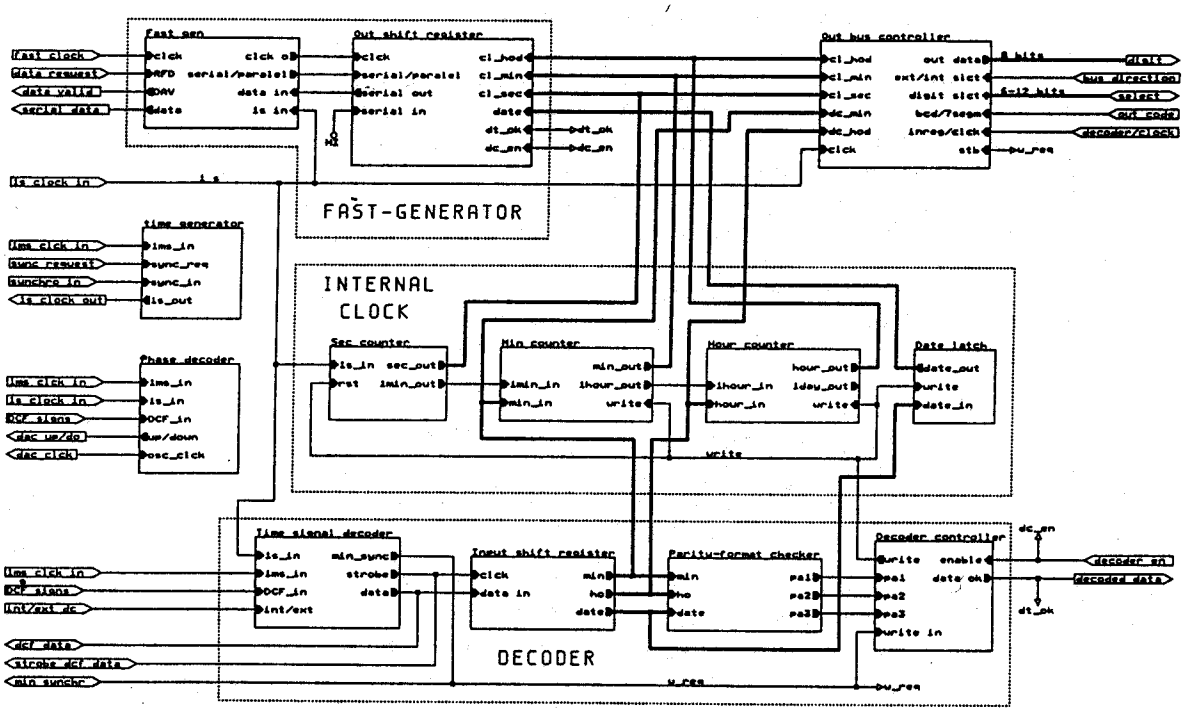

Fig.1 : DC F77 Decoder -- Fast Code Generator -- block diagram

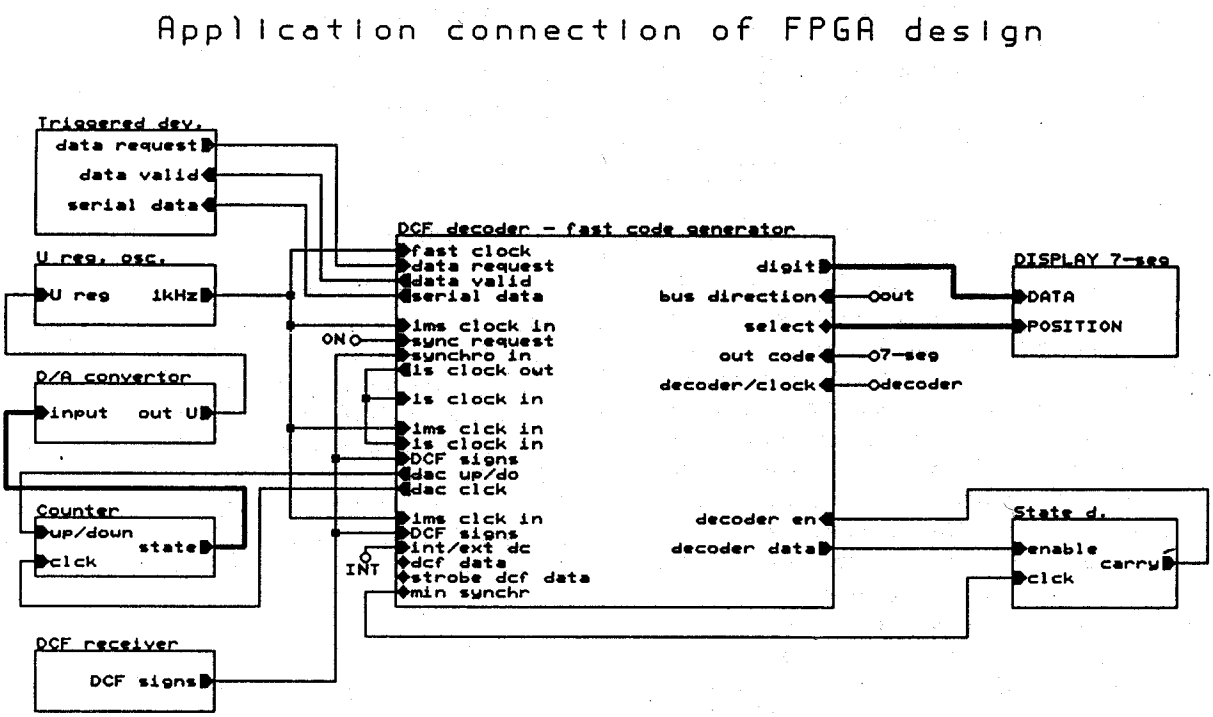

Fig .2 : DC F77 Decoder – Fast Code Generator – application diagram.

checker and a *decoder controller*. The *decoder* receives the time marks, decodes them in the *time signal decoder* and their bit representation stores in the *input shift register*. Only bits needed for the full time decoding are stored. The *time signal decoder* also generates signal *w_req* marking that the minute synchronization is detected. The *decoder controller* generates signal *write* updating time information in *internal clock*. This signal is generated, if *parity-checker* finds valid data, external *enable* signal is active and *w_req* signal comes.

Internal clock is a cascade of BCD counters, which counts *1 s clk* internal signal derived by *time_generator* from exact external oscillator. This clock has a possibility of parallel adjusting by time information from decoder.

The third part is the *fast generator*, which generates time information in the form of DCF code extended by seconds (see 2). Transmitting of the code is synchronized by *1s clock* signal, i.e. on the beginning of every second comes synchronization word. The *fast generator* consists of *out shift register*, which is parallelly updated by the time information from *internal clock* on the beginning of every second. Updating is realized in the time period when the synchronization word is transmitted. The transmitting rate is defined by external *fast clock* signal, which is logically multiplied with *data request* signal and directly connected to clock input of *output shift register*.

The *time generator* generates *1s clock* signal externally synchronized by DCF marks. This synchronization can be switch off by deactivating the signal *sync_req*.

The *phase decoder* checks synchronization of time marks and internal clock signal and generates pulses for controlling external oscillator.

The out bus controller is used for monitoring state of *decoder* and *internal clock*. It generates signals for driving an external display digits. The signal *out code* determines if the 7-segment decoder is inserted. The time information is displayed in the time multiplex which can be controlled (on the base of input *bus direction*)by external signals or generated automatically.

3. Implementation

The device should be implemented on FPGA series TPC10. The design is made like Orcad hierarchical structure using special gates equivalent to predefined TPC10 series software macros described in 3. There are expected also user defined macros, which are represented by special components created for this purpose. Describing blocks by true tables is also used. The possibilities of heterogeneous approach to design of FPGA is described in 4.

4. Conclusion

On the basis of the FPGA the DCF77 Decoder -- Fast Code Generator has been projected. Together with external radio receiver and oscillator, it generates a special serial code containing time information synchronized by atom clock. The full time information is available every second, the accuracy of time synchronization is approximately 1 ms. The Baud rate of output signal is variable, the limits are done by the length of code (64 bits/sec) and by internal parameters of FPGA arrays. The whole device developed in the Institute of Geonics AS CR is in preparation for application in seismic monitoring system.

5. References

[1] Chytil, M.: Princip časových signálů atomových hodin PTB v Braunschweigu šířených vysílačem DCF77. Automatizace 38, 1995, n.4, p. 110-113.

[2] Knejzlík, J. a kol.: Přístrojové vybavení pro monitorování přirozené a indukované seismicity v jižní části OKR. [Technical description of device], Ostrava, HOÚ ČSAV, 1991, 67p.

[3] Texas Instruments: Field Programmable Gate Array - Data Manual. [Firm literature], Texas Instruments 1993, p. 2.24-2.41.

[4] Texas Instruments: Field Programmable Gate Array - Application Manual. [Firm literature], Texas Instruments 1993, chapt. 2-4.

obr 1: DCF77 Decoder - Fast Code Generator - block diagram.

About author,...

Marek SKOTNICA was born in Čeladná, North Moravia, in 1967. He graduated from Electrotechnical fakulty of Technical university VUT in Brno, section Radiotechnics, in 1990. Now employed in Institute of Geonics of Czechoslovak Academy of Sciences in Ostrava, Division of Geophysics and Special Measurement Methods. Interested in computer programing and electronic circuits design.