# UNBALANCED CZARNUL RESISTIVE MOS CIRCUIT IN THE SYMMETRICAL MOSFET-C FILTERS

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## Abstract:

*The analysis of influence of mismatches of the MOS transistor array on center frequency $\omega_O$ and Q-factor of the MOSFET-C filter poles is performed. As a useful parameter characterizing mismatches of transistors, the dispersion of the threshold voltage $V_T$ and transconductance K per unit area in the VLSI process is considered. The optimal formula for the control gate voltages $V_{G1}, V_{G2}$ of MOS transistors, minimizing the absolute errors of $\omega_O, Q$ parameters is given.*

## Keywords:

MOS filters design, MOS resistive circuits

## 1. Introduction

In the MOSFET-C continuous-time filters, the MOS resistive circuits (MRC), shown in Fig.1, are often used [1,2,3]. As shown in [1], if transistors T1 ÷ T4 are identical and terminals 3 and 4 are connected to the input of the ideal OPAM, than $V_4 = V_3 = V$, in nonsaturation region all nonlinear products of the transistors cancel and the circuit of Fig.1 can be replaced by linear equivalent conductance circuit shown in Fig.2. If $G_i = G_i^-$ for $i$=1,2, then the current difference $i_1 - i_2$ is proportional to the input voltage difference $V_1 - V_2$ as follows

$$i_1 - i_2 = (G_1 - G_2)(V_1 - V_2) = G(V_1 - V_2) \qquad (1)$$

where:

$$G_1 = 2K(V_{G1} - V_T), \quad G_2 = 2K(V_{G2} - V_T) \qquad (2)$$

$$G = G_1 - G_2 = 2K(V_{G1} - V_{G2}) \qquad (3)$$

$K = 0.5\mu C_{OX} W / L$ is the transconductance parameter (in nonsaturation) depending on the ratio of the width $W$ to the length $L$ of the channel, $\mu C_{OX}$ is the transconductance per unit area, and $V_T$ is the threshold voltage of MOS transistor respectively. The conductance $G=G_1-G_2$ is controlled by gate voltage difference $V_{G1}-V_{G2}$ and independent of the threshold voltage $V_T$.

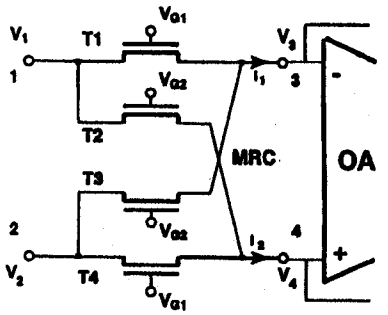


Fig.1 The MRC building block

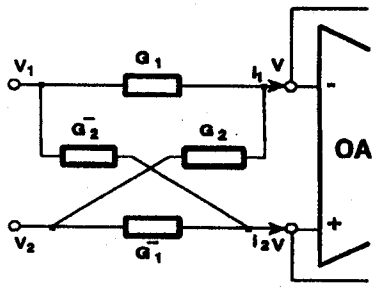


Fig.2 The linear unbalanced model of MRC block

Due to inaccuracies of the technological process, threshold voltage $V_T$ and transconductance $K$ of transistors in MRC are both different. The MRC is unbalanced and the equivalent pair of conductances must be modified in such way, that $G_i^- \neq G_i$ , $i$ = 1,2 as shown in Fig.2. In general $i_1 \neq i_2$ or $i_1 \neq -i_2$. There are however two special cases:

a) $i_1$=-$i_2$ when pins 3, 4 are shortened (this condition is not satisfied if pins 3, 4 are connected to an ideal OPAM),
b) $i_1$=0 and $i_2$=0 when pins 3, 4 are isolated.

The two above cases do not apply to the practical MOS filter structures.

In Fig.2 it is assumed that the two pairs of conductances $G_1, G_1^-$ and $G_2, G_2^-$ are different. If these assumptions hold then the results of analysis presented below are true. In case when $G_1 = G_1^-$ and $G_2 = G_2^-$, the nominal value of the of conductance $G$ in (3) can be achieved by correcting the difference of gate voltages $V_{G1} - V_{G2}$ thus eliminating the mismatch effects. In

general case when all four transistors of the MRC circuit are different, only statistical analysis is correct [4,5].

In present paper the analysis of influence of dispersion of the $V_T$ voltage and transconductance $K$ on the properties of MRC and MOSFET-C filter was performed. The optimal formula for the control gate voltages $V_{G1}, V_{G2}$ of MOS transistors, minimizing the mismatches effect is also given.

## 2. Analysis of unbalance of the MRC circuit

Assuming that both transistor pairs (T1,T3) and (T2,T4) are identical respectively, we can obtain by Kirchhoff's law (Fig.2):

$$i_1 - i_2 = GV_1 - G^{-}V_2 + (G^{-} - G)V \tag{4}$$

where $G = G_1 - G_2$, $G^{-} = G_1^{-} - G_2$. Conductances in the expressions (4) depend on transistor parameters as follows:

$$G_i = 2K(V_{Gi} - V_T), \quad G_i^{-} = 2K^{-}(V_{Gi} - V_T^{-}), \; i = 1,2 \tag{5}$$

where: $V_T^{-} = V_T + \Delta V_T$, $K^{-} = K + \Delta K$. Substituting the expression (5) into (4) we can obtain

$$G = 2K(V_{G1} - V_{G2}) + 2K\Delta V_T - 2(V_{G2} - V_T)\Delta K + 2\Delta K\Delta V_T \tag{6a}$$

$$G^{-} = 2K(V_{G1} - V_{G2}) - 2K\Delta V_T + 2(V_{G1} - V_T)\Delta K - 2\Delta K\Delta V_T \tag{6b}$$

Let us denote $G^{-} = G(1+\delta)$, where: $\delta = (G^{-} - G)/G = \Delta G/G$ is the relative error of conductances G. From expressions (6a,b) and when the second order product proportional to $\Delta K\Delta V_T$ is neglected because $|\Delta K\Delta V_T| << |K\Delta V_T|$, we obtain

$$\delta = \frac{-2\dfrac{V_T}{V_{G1}-V_{G2}}\dfrac{\Delta V_T}{V_T} + \dfrac{\Delta K}{K}\left(\dfrac{V_{G1}+V_{G2}-2V_T}{V_{G1}-V_{G2}}\right)}{1 + \dfrac{V_T}{V_{G1}-V_{G2}}\dfrac{\Delta V_T}{V_T} - \dfrac{\Delta K}{K}\left(\dfrac{V_{G2}-V_T}{V_{G1}-V_{G2}}\right)} \tag{7}$$

where $\Delta K/K$, $\Delta V_T/V_T$ are relative errors of the transconductance parameter and threshold voltage respectively.

In this case the equation (1) has the following form

$$i_1 - i_2 = G[(1+\delta)(V_1 - V_2) + \delta V] \tag{8}$$

The mismatches effect can be minimized when values of $\delta$ can be minimized. In the ideal case $\delta = 0$ and expression (8) reduces to (1). In the worst case the $\delta$ is limited by:

$$\delta_{min} < |\delta| < \delta_{max} \tag{9}$$

where:

$$\delta_{min} = \left| \frac{2\left|\dfrac{V_T}{V_{G1}-V_{G2}}\right|\left|\dfrac{\Delta V_T}{V_T}\right| - \left|\dfrac{V_{G1}+V_{G2}-2V_T}{V_{G1}-V_{G2}}\right|}{1 + \left|\dfrac{V_T}{V_{G1}-V_{G2}}\right|\left|\dfrac{\Delta V_T}{V_T}\right| + \left|\dfrac{V_{G2}-V_T}{V_{G1}-V_{G2}}\right|\left|\dfrac{\Delta K}{K}\right|} \right| \tag{10a}$$

$$\delta_{max} = \left| \frac{2\left|\dfrac{V_T}{V_{G1}-V_{G2}}\right|\left|\dfrac{\Delta V_T}{V_T}\right| + \left|\dfrac{V_{G1}+V_{G2}-2V_T}{V_{G1}-V_{G2}}\right|}{1 - \left|\dfrac{V_T}{V_{G1}-V_{G2}}\right|\left|\dfrac{\Delta V_T}{V_T}\right| - \left|\dfrac{V_{G2}-V_T}{V_{G1}-V_{G2}}\right|\left|\dfrac{\Delta K}{K}\right|} \right| \tag{10b}$$

The range of $\delta$ can be minimized by an appropriate choice of $V_{G2}$. If the gate voltage $V_{G2}$ is greater, but nearly equal to $V_T$ and if the voltage difference $V_{G1} - V_{G2}$ is greater than $V_T$, according to (10a,b)

$$V_{G2} \cong V_T, \quad V_{G1} - V_{G2} > V_T \tag{11}$$

then $\delta$ reduces to $\delta^*$:

$$\delta^* = \frac{-2\dfrac{V_T}{V_{G1}-V_{G2}}\dfrac{\Delta V_T}{V_T} + \dfrac{\Delta K}{K}}{1 + \dfrac{V_T}{V_{G1}-V_{G2}}\dfrac{\Delta V_T}{V_T}} \tag{12}$$

and the following inequality constraints are satisfied

$$\delta_{min} \le \delta^*_{min} \le |\delta^*| \le \delta^*_{max} \le \delta_{max} \tag{13}$$

where

$$\delta^*_{min} = \left| \frac{2\gamma\left|\dfrac{\Delta V_T}{V_T}\right| - \left|\dfrac{\Delta K}{K}\right|}{1 + \gamma\left|\dfrac{\Delta V_T}{V_T}\right|} \right|, \quad \delta^*_{max} = \left| \frac{2\gamma\left|\dfrac{\Delta V_T}{V_T}\right| + \left|\dfrac{\Delta K}{K}\right|}{1 - \gamma\left|\dfrac{\Delta V_T}{V_T}\right|} \right| \tag{14}$$

and $|\gamma| = V_T/(V_{G1} - V_{G2})|$

If the voltage $V_{G1}$ tends to infinity, the error $\delta$ decreases but remains no less than $|\Delta K/K|$, $|\delta| \le |\Delta K/K|$. Also if $V_{G1}$ tends to $V_{G2}$ (independently of the value of $V_{G2}$), then $|\delta|$ increases but remains less than 2, $|\delta| \le 2$.

For the VLSI 1.6 $\mu m$ process, in case of the NMOS transistors, the typical values of parameters used are:

$V_T = 0.7V$, $K = 24\mu A/V^2$, $|\Delta V_T/V_T| = 1.7\%$, $|\Delta K/K| = 9\%$.

Results of the above analysis can be illustrated by the two following cases.

Case a). Assuming $V_{G2} = 0{,}81\,V$, greater than $V_T$, $V_{G1} = 1\,V$ ($V_{G1} - V_{G2} = 0.19\,V$) and relative errors equal to $\Delta V_T/V_T = 1.7\%$, $\Delta K/K = -9\%$. On the basis of expression (9) we obtain: $|\delta| = 0.2847$, $\delta_{max} = 0.3529$,

$\delta_{min} = 0.0188$. Plot of the boundary area of $|\delta|$ versus $V_{G1} \in [0.9, 1.5]\,V$ is shown in Fig.3.

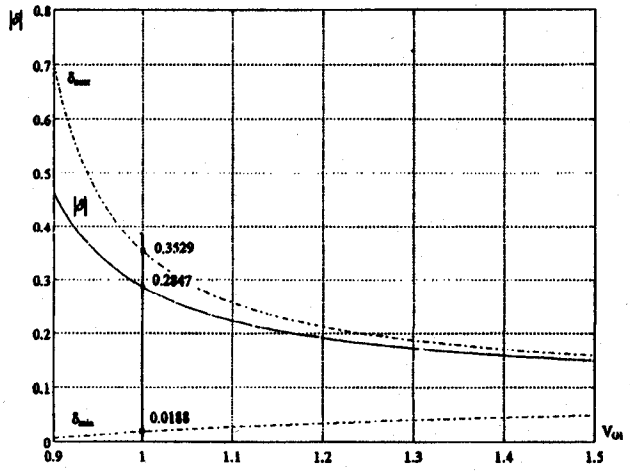


Fig.3 Error $|\delta|$ versus $V_{G1}$, for $|\Delta K/K| = 9\%$, $|\Delta V_T/V_T| = 1.7\%$, $V_{G2}$=0.81V

Case b). Assuming $V_{G2} = 0.71\,V$, greater and nearly equal to $V_T$, and $V_{G1} = 0.9\,V$, $(V_{G1} - V_{G2} = 0.19\,V)$ and the same values of relative errorss $\Delta V_T/V_T$, $\Delta K/K$ as above. We obtain $|\delta^*| = 0.2025$, $\delta^*_{max} = 0.2290$, $\delta^*_{min} = 0.0359$. Plot of the boundary area of $|\delta^*|$ versus $V_{G1} \in [0.8, 1.5]\,V$ is shown in Fig.4.

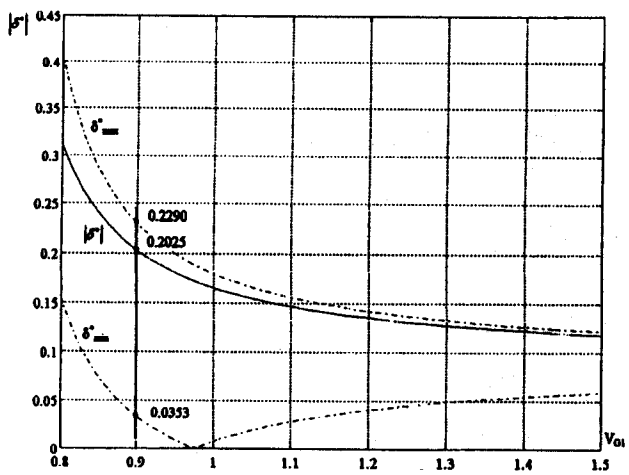


Fig.4 Error $|\delta^*|$ versus $V_{G1}$, for $|\Delta K/K| = 9\%$, $|\Delta V_T/V_T| = 1.7\%$, $V_{G2}$=0.71V

In both cases, according to (3) conductance $G$ has the same value $G = 2K(V_{G1} - V_{G2}) = 48 \cdot 10^{-6} \cdot 0.19 = 9.12\,\mu S$. Comparison of Fig.3 and Fig.4 shows that the boundary area of $|\delta|$ is smallest when conditions (11) are satisfied. For given values of $\Delta V_T/V_T$ and $\Delta K/K$ we have $|\delta^*|/|\delta| \le 0.7$ and $|\delta^*|$ is 30% less than the $|\delta|$.

# 3. Implementation to the analysis of the MOSFET-C filter

The center frequency $\omega_o$ and Q-factor for every known MOSFET-C filter, as for the Tow-Thomas filter structure [2] shown in Fig.5, are determined by $\omega_o = G/C = \mu C_{ox}(W_o/L_o)(V_{G1} - V_{G2})$ and $Q = G/G_Q = (W_o/L_o)/(W_Q/L_Q)$, if according to (3) the voltage difference $V_{G1}$-$V_{G2}$ in formulas for $\omega_o$ and $Q$ remains the same.

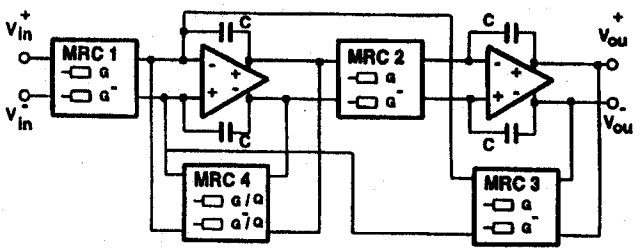


Fig.5 Tow-Thomas MOSFET-C filter structure

Values of the $\omega_o$ and $Q$ are fixed by the choice of geometric ratios $W_o/L_o$, $W_Q/L_Q$ for MOS transistors of the MRC circuits. In the worst case, the errors of center frequency $\omega_o$ and Q-factor are equal to:

$$\left|\frac{\Delta\omega_o}{\omega_o}\right| = \left|\frac{\Delta G}{G}\right| = |\delta|, \qquad \left|\frac{\Delta Q}{Q}\right| = \left|\frac{\Delta G}{G} - \frac{\Delta G_Q}{G_Q}\right| \le 2|\delta|$$

and the errors $\Delta\omega_o/\omega_o$, $\Delta Q/Q$ can be minimized by choosing the gate voltages $V_{G1}, V_{G2}$ according to (11). In consequence the procedure given to minimize the mismatches of the MRC transistor array is equivalent to the corresponding procedure minimizing the errors of frequency responses of MOSFET-C filters by minimizing the errors of the $\omega_o$, $Q$ parameters.

# 4. Conclusions

The errors of center frequency $\omega_o$ and $Q$-factor with respect to mismatches of the transistor array in the MRC circuit can be minimized by choosing the gate controlled voltages $V_{G1}, V_{G2}$, according to the formula (11). Minimum errors occur, if the voltage $V_{G2}$ is nearly equal to the threshold voltage $V_T$, which in turn is less than $V_{G1}$. In this case the boundary area of $\delta$ is practically limited by $\Delta V_T/V_T$ and $\Delta K/K$. In other cases the error boundary of $\delta$ becomes much greater.

By minimizing the error $|\delta|$, the automatic tuning circuit of the MOSFET-C filter [2] with smaller dynamic range can be used because the error of $\delta$ and the range of corrected values of $\omega_O$, $Q$ are smaller.

Finally, the nonlinear product of the unbalanced MRC circuit can be also minimized, because when the

terms defined by (11) are satisfied, the mismatches of transistors in MRC circuits are minimized. The nonlinear product due to mismatches of the transistors T1 - T4 in the MRC circuits is also minimized.

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