PREVENTING INDUCTIVE OUTPUT IMPEDANCE OF HIGH-FREQUENCY EMITTER FOLLOWER STAGES

Jiří NERAD
Dept. of Radio Engineering
Czech Technical University of Prague
Technická 2, 166 27 Praha 6, Czech Republic
(+420 2) 2435 2247, Nerad@feld.cvut.cz
and
Richard C. TOZER
Dept. of Electronic and Electrical Engineering
University of Sheffield
Mappin Street, Sheffield S1 3JD, England

Abstract

Large output inductance is one of major issues of high-frequency emitter follower design. The most often suggested technique to reduce its value is the decreasing of AC transconductance which offers small output inductance at the expense of loosing low output resistance. The paper presents a different approach; it is shown that output inductance can be completely cancelled while keeping very low output resistance by introducing a pole at the input node which may be more suitable in many types of design. Complete analytical evaluation based on the full hybrid-π model of the bipolar transistor device is given.

Keywords

emitter follower, high frequency, bandwidth, output impedance, output inductance, output resistance, bipolar transistor, BJT, hybrid-π model

1. Common approach (resistive source)

Firstly, the common conclusions and suggestions based on the simplest model of the bipolar transistor device (BJT) expressing its current gain roll-off will be discussed [3] [4].

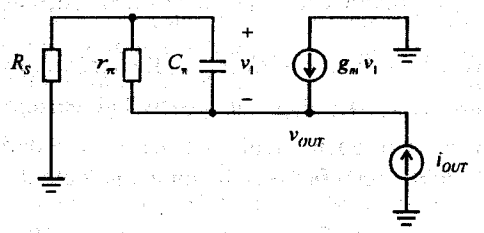

Fig. 1. Output impedance of emitter follower driven by resistive source

The output impedance of the stage in Fig. 1 is

$$Z_{OUT} = \frac{v_{OUT}}{i_{OUT}} = \frac{1}{G_S}\frac{G_S + g_\pi + sC_\pi}{g_m + g_\pi + sC_\pi} = \tag{1}$$

$$= \frac{1}{G_S}\frac{G_S + g_\pi}{g_m + g_\pi}\frac{1+\frac{s}{s_Z}}{1+\frac{s}{s_P}}$$

where

$$s_P = -\frac{g_m + g_\pi}{C_\pi} \tag{2}$$

and

$$s_Z = -\frac{G_S + g_\pi}{C_\pi} \tag{3}$$

If the zero is to match or follow the pole, the conditions below will apply

$$\frac{g_m + g_\pi}{C_\pi} \le \frac{G_S + g_\pi}{C_\pi} \tag{4}$$

i. e.

$$g_m \le G_S \tag{5}$$

Discussion

At very low frequencies, all terms associated with the capacitance C_π need not be considered and, provided the LF [1] current gain $\beta = \frac{g_m}{g_\pi}$ is high (i. e. $g_m >> g_\pi$), the LF output resistance can be expressed from Eq. 1 as follows

$$R_{OUT} = \frac{1}{G_S}\frac{G_S + g_\pi}{g_m} = \frac{1}{g_m} + \frac{R_S}{\beta} \tag{6}$$

[1] *LF* denotes the *low-frequency range* (starting with those frequencies at which all decoupling capacitors and inductors can be regarded as DC voltage and current supplies, respectively, and ending with those frequencies at which the effects of other capacitive or inductive elements can no longer be neglected).

Consequently, $\frac{R_{OUT}}{R_S}$ can approach $\frac{1}{\beta}$ unless $\frac{1}{g_m}$ is too large (compared to $\frac{R_S}{\beta}$). Anyway, whatever the transconductance, the major contribution to the output current is always provided by the controlled current supply.

In contrast, at very high frequencies, C_π will short circuit the control voltage v_1, so that the controlled current supply will behave as an open circuit and the whole stage will behave as a short circuit between its input and output.

Conclusion

As far as the circuit in Fig. 1 is concerned, whatever its LF output resistance, at very high frequencies its output impedance will *always* become resistive having the value of R_S. What Cond. 5 [3] [4] actually suggests, is the *increasing* of the LF resistance to reach R_S in order to avoid the +20 dB/dec section. (This can always be accomplished by decreasing the DC collector current (I_C) as g_m is directly proportional to I_C while β is almost independent of I_C over many decades.) In that case, however, the using of the emitter follower stage to reduce the (LF) output resistance of the previous stage makes little sense as it can only reduce the loading of that stage at low frequencies.

2. New approach (capacitive source)

2.1 Introduction

The central idea of a different design approach to be described here can be explained as follows:

The frequency dependence of the output impedance examined above can involve the +20 dB/dec section because, due to the transistor current gain roll-off, the stage gradually looses the impedance transforming capability, so that the full source impedance will eventually appear at the output. As the roll-off is unavoidable, the only way of achieving very small values of the LF output resistance while preventing the output impedance from increasing with frequency is the appropriate reducing of the source impedance at high frequencies.

So far, a purely resistive source has been assumed. Next, consequences of adding a parallel capacitance to the source resistance will be examined. Conditions of avoiding inductive output impedance will be investigated in three steps, beginning with the simplest model of the BJT expressing its current gain roll-off and ending with the full hybrid-π model. This approach had to be used because the formulas given by the full model are too complex to suggest a design procedure whereas the using of a simple model to derive general conditions and then gradual extending the model while watching changes of these conditions was found quite suitable here.

2.2 First approximation

Fig. 2 shows the circuit used to find out general conditions of cancelling inductive component of output impedance.

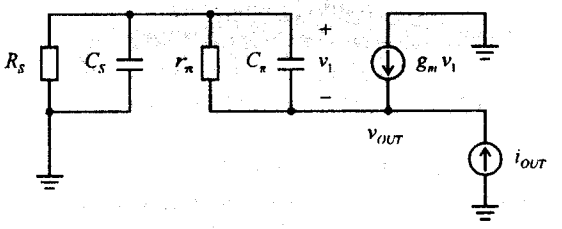

Fig. 2. Output impedance of emitter follower (first approximation)

The output impedance is now

$$Z_{OUT} = \frac{v_{OUT}}{i_{OUT}} = \frac{G_S + g_\pi + s(C_S + C_\pi)}{(G_S + sC_S)(g_m + g_\pi + sC_\pi)} = \tag{7}$$

$$= \frac{1}{G_S}\frac{G_S + g_\pi}{g_m + g_\pi}\frac{1 + \frac{s}{s_Z}}{\left(1 + \frac{s}{s_{P1}}\right)\left(1 + \frac{s}{s_{P2}}\right)}$$

where

$$s_{P1} = -\frac{G_S}{C_S} \tag{8}$$

$$s_{P2} = -\frac{g_m + g_\pi}{C_\pi} \tag{9}$$

and

$$s_Z = -\frac{G_S + g_\pi}{C_S + C_\pi} \tag{10}$$

If $|s_{P2}|$ is to be less than or equal to $|s_Z|$, i. e.

$$\frac{G_S + g_\pi}{C_S + C_\pi} \geq \frac{g_m + g_\pi}{C_\pi} \tag{11}$$

then it is necessary that

$$1 > \frac{C_\pi}{C_S + C_\pi} \geq \frac{g_m + g_\pi}{G_S + g_\pi} \tag{12}$$

and again

$$g_m < G_S \tag{13}$$

The relation between the LF output resistance and that of the source is

$$R_{OUT} > \frac{1}{g_m} > R_S \tag{14}$$

and the same conclusion as that of the previous section can be drawn.

By contrast, if $|s_{P1}|$ is to be less than or equal to $|s_Z|$, i. e.

$$\frac{G_S + g_\pi}{C_S + C_\pi} \geq \frac{G_S}{C_S} \tag{15}$$

or

$$\frac{G_S + g_\pi}{G_S} \geq \frac{C_S + C_\pi}{C_S} \tag{16}$$

a new condition will apply

$$\frac{g_\pi}{C_\pi} \geq \frac{G_S}{C_S} \tag{17}$$

which is by no means related to the LF transconductance (I_C).

Conclusion

The output impedance of the stage in Fig. 2 cannot become inductive at any frequency provided *the time constant formed by the resistance and capacitance of its source is larger than or equal to the time constant associated with the current gain cut-off of the BJT.* In contrast to previous conditions giving fixed limits of the LF transconductance (g_m) for each value of the source resistance (R_S), there is one degree of freedom now; inductive output impedance can be cancelled for any two values of R_S and g_m by adjusting the source capacitance (C_S).

2.3 Second approximation

The next step consists in including the base resistance (r_b) in the model of the BJT (see Fig. 3).

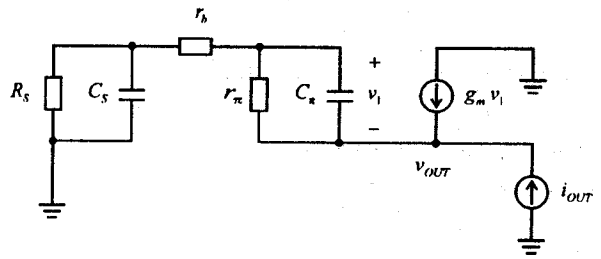

Fig. 3. Output impedance of emitter follower (second approximation)

The presence of r_b will worsen the performance, which is easy to understand if r_b is viewed as a series element added to the source considered previously: it increases its resistance - and hence the resistance seen at the output at very high frequencies - by a constant amount.

In terms of pole and zero frequencies:

On evaluating the output impedance

$$Z_{OUT} = \frac{v_{OUT}}{i_{OUT}} = \tag{18}$$

$$= \frac{g_b G_S + g_\pi G_S + g_\pi g_b + s(g_b C_S + g_\pi C_S + g_b C_\pi + G_S C_\pi) + s^2 C_\pi C_S}{g_b (G_S + sC_S)(g_m + g_\pi + sC_\pi)} = \frac{N}{D}$$

where

$$N = g_b G_S + g_\pi G_S + g_\pi g_b + s(g_b C_S + g_\pi C_S + g_b C_\pi + G_S C_\pi) + s^2 C_\pi C_S \tag{19}$$

$$D = g_b G_S (g_m + g_\pi)\left(1 + \frac{s}{s_{P1}}\right)\left(1 + \frac{s}{s_{P2}}\right) \tag{20}$$

$$s_{P1} = -\frac{G_S}{C_S} \tag{21}$$

and

$$s_{P2} = -\frac{g_m + g_\pi}{C_\pi} \tag{22}$$

it can be seen that both poles remained unchanged.

To find the placement of the zeros, s_{Z1} and s_{Z2}, simplified formulas assuming $|s_{Z1}| << |s_{Z2}|$ will be used [2]. The first zero is now

$$s_{Z1} \approx -\frac{g_b G_S + g_\pi G_S + g_\pi g_b}{C_S(g_b + g_\pi) + C_\pi(g_b + G_S)} \tag{23}$$

whereas the first (and only) zero of the output impedance examined previously was (Eq. 10)

$$s'_{Z1} = -\frac{G_S + g_\pi}{C_S + C_\pi} \tag{24}$$

The comparison of Eq. 23 and 24 shows that

- $s_{Z1} \approx s'_{Z1}$ if $g_b >> g_\pi, G_S$
- $|s'_{Z1}| \geq |s_{Z1}|$

Conclusions

(i) As the base resistance (r_b) is increased, the first zero moves towards low frequencies while both poles remain unchanged.

(ii) To prevent inductive output impedance, the source time constant ($R_S C_S$) will need to be *larger* than that of the current gain cut-off ($r_\pi C_\pi$) unless r_b is very small compared to the source resistance (R_S) and the base-emitter resistance (r_π).

To complete the calculation, the relation between the second pole and zero (s_{P2} and s_{Z2}) has to be verified [2].

$$s_{Z2} \approx -\frac{C_S(g_b + g_\pi) + C_\pi(g_b + G_S)}{C_\pi C_S} = \tag{25}$$

$$= -\left(\frac{g_b + g_\pi}{C_\pi} + \frac{g_b + G_S}{C_S}\right)$$

If s_{Z2} is not to precede s_{P2}, then

$$\frac{g_b + g_\pi}{C_\pi} + \frac{g_b + G_S}{C_S} \geq \frac{g_m + g_\pi}{C_\pi} \tag{26}$$

The *sufficient* condition of this inequality being

$$g_b \geq g_m \frac{C_S}{C_S + C_\pi} \tag{27}$$

For many high-frequency/wideband transistors biased to obtain high unity-gain frequency, the base resistance (r_b) is very small (10 Ω or even less) while the base-emitter capacitance (C_π) is considerably large (above 5 pF; see Appendix). Hence, Cond. 27 is quite unlikely to force changes of circuit design. Nevertheless, it can be concluded by saying that, due to the presence of the base

[2] The discussion below is of theoretical rather than practical importance. For most high-frequency / wideband transistors, Eq. 22 and 25 give frequencies beyond the range in which the hybrid-π or Gummel-Poon approach is applicable.

resistance, the transconductance is no longer without a theoretical limit.

2.4 Third approximation

To obtain the complete hybrid-π model, the internal and external base-collector capacitance (C_μ and $C_{\mu 1}$, respectively) and the output resistance (R_{OUT}) have been added to the last circuit (see Fig. 4).

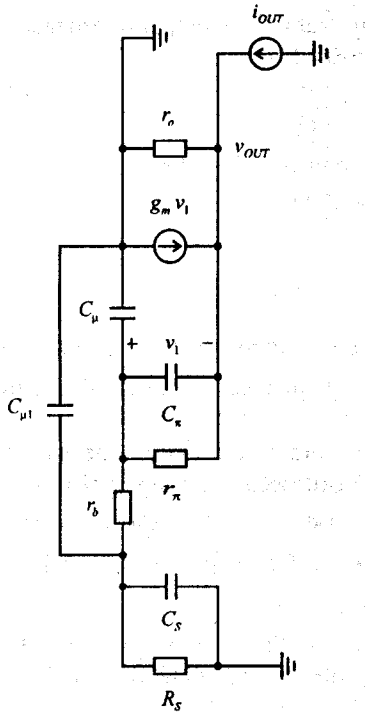

Fig. 4. Output impedance of emitter follower (complete hybrid-π model)

Before evaluating its output impedance, the above circuit can be simplified without loss of generality:

- $C_{\mu 1}$ can be included in the source capacitance (formerly C_S, now C_{S1})

$$C_{S1} = C_S + C_{\mu 1} \tag{28}$$

- Since only the conditions of avoiding / cancelling inductive component of output impedance are to be sought, R_{OUT} can be left out for it does not influence its presence.

The circuit used for the final analysis is shown below.

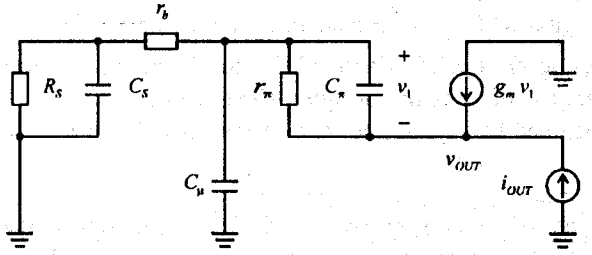

Fig. 5. Output impedance of emitter follower (third approximation)

The output impedance of the stage is

$$Z_{OUT} = \frac{v_{OUT}}{i_{OUT}} = \tag{29}$$

$$= \frac{\begin{array}{c} g_b G_S + g_\pi G_S + g_\pi g_b + \\ + s\left[g_b C_{S1} + g_\pi C_{S1} + g_b\left(C_\pi + C_\mu\right) + G_S\left(C_\pi + C_\mu\right)\right] + \\ + s^2\left(C_\pi + C_\mu\right)C_{S1} \end{array}}{\begin{array}{c} \left(g_m + g_\pi + sC_\pi\right) \times \\ \times\left[s^2 C_{S1} C_\mu + s\left(C_{S1} g_b + C_\mu g_b + C_\mu G_S\right) + G_S g_b\right] \end{array}} =$$

$$= \frac{N}{D'D''}$$

where

$$N = \tag{30}$$

$$= g_b G_S + g_\pi G_S + g_\pi g_b +$$
$$+ s\left[g_b C_{S1} + g_\pi C_{S1} + g_b\left(C_\pi + C_\mu\right) + G_S\left(C_\pi + C_\mu\right)\right] +$$
$$+ s^2\left(C_\pi + C_\mu\right)C_{S1}$$

$$D' = \left(g_m + g_\pi + sC_\pi\right) \tag{31}$$

and

$$D'' = s^2 C_{S1} C_\mu + s\left(C_{S1} g_b + C_\mu g_b + C_\mu G_S\right) + G_S g_b \tag{32}$$

As can be seen from Eq. 31,

$$s_{P2} = -\frac{g_m + g_\pi}{C_\pi} \tag{33}$$

remained unchanged. To find the other two poles, s_{P1} and s_{P3}, from Eq. 32, simplified / approximate formulas assuming $|s_{P1}| << |s_{P3}|$ have to be used again [2]. The estimation of the first pole s_{P1} is

$$s_{P1} \approx -\frac{G_S g_b}{g_b C_{S1} + g_b C_\mu + G_S C_\mu} = -\frac{1}{\dfrac{C_{S1} + C_\mu}{G_S} + \dfrac{C_\mu}{g_b}} \tag{34}$$

while the estimation of the higher-order pole s_{P3} is

$$s_{P3} \approx -\frac{C_{S1} g_b + C_\mu g_b + C_\mu G_S}{C_{S1} C_\mu} = -\left(\frac{g_b}{C_\mu} + \frac{g_b + G_S}{C_{S1}}\right) \tag{35}$$

Notes

(i) As the order of the preceding circuit was two, apart from s_{P2} mentioned above, only the placement of s_{P1} can be compared with its counterpart, which is (Eq. 21)

$$s'_{P1} = -\frac{1}{\dfrac{C_S}{G_S}} \tag{36}$$

(ii) For most HF transistors (with forward biased base-emitter and reverse biased base-collector), C_μ is only a fraction of C_π while the order of g_m is unlikely to be larger than that of g_b (see Appendix). Consequently

$$|s_{P3}| > |s_{P2}| \tag{37}$$

and, since s_{P3} is the third pole while there are only two zeros, its frequency need not be considered any further.

As far as the zeros are concerned, it is important to note first that the last change of the numerator (now given by Eq. 30) can be viewed as the replacing of each occurrence of C_π with $C_\pi + C_\mu$. Consequently, s_{Z1} and s_{Z2} will be derived from Eq. 23 and 25 by means of this substitution.

$$s_{Z1} \approx -\frac{g_b G_S + g_\pi G_S + g_\pi g_b}{C_{S1}(g_b + g_\pi) + (C_\pi + C_\mu)(g_b + G_S)} \tag{38}$$

$$s_{Z2} \approx -\left(\frac{g_b + g_\pi}{C_\pi + C_\mu} + \frac{g_b + G_S}{C_{S1}}\right) \tag{39}$$

Again, the assumption of $g_b >> g_\pi, G_S$ is justified giving

$$s_{Z1} \approx -\frac{G_S + g_\pi}{C_{S1} + C_\pi + C_\mu} \tag{40}$$

in contrast to the first zero of the preceding circuit, which is (under the same condition)

$$s''_{Z1} \approx -\frac{G_S + g_\pi}{C_S + C_\pi} \tag{41}$$

Discussion

(I) On connecting C_μ both the first pole and zero move towards low frequencies, the ratio between the new and original frequency being $\frac{C_S}{C_{S1} + C_\mu}$ (for the pole) and $\frac{C_S + C_\pi}{C_{S1} + C_\pi + C_\mu}$ (for the zero). As $\frac{C_S}{C_{S1} + C_\mu} < \frac{C_S + C_\pi}{C_{S1} + C_\pi + C_\mu}$ for any values of capacitances involved, the pole always moves faster than the zero, i. e. the output impedance is made more capacitive or less inductive. This is because C_μ reduces the constant contribution to the source resistance (as seen by the internal base) caused by the presence of r_b.

(II) As far as the first pole and zero is concerned, the time-constant approach is applicable as introduced at the beginning of the analysis, i. e.

$$\frac{C_{S1}}{G_S} \geq \frac{C_\pi}{g_\pi} \tag{42}$$

is the *sufficient* condition for the first zero to match or follow the first pole

$$|s_{P1}| \leq |s_{Z1}| \tag{43}$$

or (Eq. 34 and 40)

$$\frac{C_{S1} + C_\mu}{G_S} + \frac{C_\mu}{g_b} \geq \frac{C_{S1} + C_\pi + C_\mu}{G_S + g_\pi} \tag{44}$$

It can easily be shown that Cond. 44 can be obtained from Cond. 42 by first rearranging the latter to obtain $\frac{C_{S1}}{G_S} \geq \frac{C_{S1} + C_\pi}{G_S + g_\pi}$ and next adding $\frac{C_\mu}{g_b} + \frac{C_\mu}{G_S}$ and $\frac{C_\mu}{G_S + g_\pi}$ to its left and right hand side, respectively, which, obviously, cannot change the inequality.

(III) By contrast, if the second zero is to match or follow the second pole, the following condition will apply (Eq. 33 and 39)

$$\frac{g_b + g_\pi}{C_\pi + C_\mu} + \frac{g_b + G_S}{C_{S1}} \geq \frac{g_m + g_\pi}{C_\pi} \tag{45}$$

As opposed to Cond. 26 and 27, no straightforward conclusion can be derived now. However, should C_μ be much smaller than C_π (it usually is; see Appendix)

$$g_b \geq g_m \frac{C_{S1}}{C_{S1} + C_\pi} \tag{46}$$

can again be considered as the sufficient condition of interest.

3. Summary

Detailed analysis of the placement of poles and zeros of the output impedance of the emitter follower stage has been presented using the complete hybrid-π model of the transistor device. It has been found that small low-frequency output resistance can be obtained and, at the same time, inductive output impedance can be prevented at all frequencies provided the source impedance can be expressed with a parallel RC circuit whose time constant is larger than that of the current gain cut-off (Cf. [1]).

If all of the obtained conditions of preventing inductive output impedance are to be strictly observed, there will also be a limitation regarding the low-frequency transconductance; in practice, however, it need not be assumed limited as its increase can only result in very small amount of output inductance (Cf. [1]).

4. Conclusion

Inductive component of output impedance can be reduced or - should it be the main design objective - prevented at all frequencies while maintaining low output resistance provided an input pole of down to the current gain cut-off frequency can be accommodated. This may but need not necessarily involve considerable loss of bandwidth; it should be borne in mind that emitter follower stages are very often placed after high-impedance or high-resistance nodes where poles of relatively low frequencies are hard to prevent.

Therefore it is the designer's responsibility to decide which approach is more favourable for each particular circuit: decreasing the transconductance resulting in irreversible increase of output resistance on one hand or decreasing the input pole frequency (whose effect can be compensated by introducing a zero somewhere else in the circuit, for instance) on the other hand. However, the common

approach cannot compete with the technique suggested in this paper whenever the input pole can be used as the dominant pole of a feedback amplifier.

5. Appendix hybrid-π model parameters of example HF transistors

Type	I_C (mA)	V_{CE} (V)	g_m $\left(\frac{1}{\Omega}\right)$	r_π (Ω)	C_π (pF)
Philips BFR92A	15	10	0. 57	160	12
Philips BFT92	15	10	0. 51	62	12

(cont'd)

Type	r_B (Ω)	C_μ (fF)	$C_{\mu 1}$ (fF)	r_o $(k\Omega)$
Philips BFR92A	10	43	240	3. 8
Philips BFT92	5	53	440	1. 8

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About author...

Jiří NERAD received his Ing. (M. Sc. equivalent) degree in Radio Engineering from the Czech Technical University of Prague in 1993. Next he attended a one-year MPhil by research course focused on high-frequency operational amplifier design at the University of Sheffield. He is currently finishing his PhD project at the Czech Technical University. His major research interest is CAD in electrical engineering focused on maximum-bandwidth design.

RADIOENGINEERING REVIEWERS

April 1997, Volume 6, Number 1