KVASIRESONANT DC-DC CONVERTER WITH SWITCHING AT ZERO CURRENT - PART 1

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Abstract
A kvasiresonant DC - DC converter and its control circuits are proposed. The relations useful for design of the converter will be deduced in the part 2.

The fundamental idea of the converter is the switching -on and -off a transistor at zero current. In this way the switching losses are eliminated. It enables to design a converter with a large output power (several kW), high switching frequency (about 200 kHz), very good efficiency and low radiation.

Keywords
switching losses, resistance losses, resonance, transistor, diode, choke coil, inductor, capacitor, controlling, damping, winding, coupling, comparator, PI regulator, pulse delaying, over-current protection, undervoltage protection

1. Introduction
The basic problem of resonant converters is a difficult regulation. The essential principle of described converter was received from [1] but a new control system was created. The original system used 8 additional switching transistors in the power circuit to reach for 256 levels of the resonant capacity (switched - capacitor - based resonant circuit). It represents additional resistance losses which are not negligible, especially in power applications. The new system uses only one resonant capacitor. That's why there are no additional switching transistors in the converter. The control system operates as a continuous-action controller and the reachable control range isn't reduced.

2. The power circuit of the converter
The scheme of the power circuit shows the fig. 1. It differs from the version of [1] only with using a simple resonant capacitor $C_R$.

The presumption for a good working of the converter is: The inductivity $L_p$ is so high, that the current $I_{open}$ is almost constant in a steady state regime. It's no practical problem, because the switching frequency is very high.

![Fig. 1 The power circuit of the converter](image)

The action of one switching cycle in a steady state regime shows the fig. 2. It's necessary to describe it very carefully if we want to explain the control system.

![Fig. 2 The action of one switching cycle in a steady state regime](image)
a) Before switching-on the transistor \( T \) the constant current \( I_{OUT} \) flows through the diode \( D_0 \). Its source is the choke coil \( L_R \). The diode \( D_0 \) is open, the voltage \( U_C \) on the capacitor \( C_R \) is zero. (We presuppose an ideal diode with zero forward voltage).

b) By switching-on the transistor \( T \) we put in fact the input voltage \( U_D \) directly onto the inductor \( L_R \) because the voltage \( U_C \) is zero (open diode \( D_0 \)). That’s why the current \( i_L \) in the inductor \( L_R \) starts to increase linearly from a zero initial value. It flows in fact through the open diode \( D_0 \) but „from the katode to the anode“! It’s better to say, that the real current through the \( D_0 \) „from A to K“ will be lower than \( I_{OUT} \) because it’ll be:

\[
i_{D_0}(t) = I_{OUT} - i_L(t)
\]

(1)

While \( i_L \) \(<\) \( I_{OUT} \), the diode \( D_0 \) continues to be open and the voltage \( U_C \) is zero. The linear increasing of the \( i_L \) can be described with an equation:

\[
i_L(t) = \frac{U_D \cdot t}{I_R}
\]

(2)

This process ends when passes the time \( t_1 \) and \( i_L \) equals to \( I_{OUT} \). In this while the current through diode \( D_0 \) reaches a zero value and the diode \( D_0 \) closes. From the equation (2) we can deduce a relation for the duration of \( t_1 \):

\[
t_1 = \frac{I_{OUT}}{U_D}
\]

(3)

c) Now disappeared the short circuit of \( C_R \), by closing the \( D_0 \). The current \( i_L \) in the inductor \( L_R \) now can be described with a relation:

\[
i_L(t) = I_{OUT} + i_{RES}(t)
\]

(4)

The \( i_{RES} \) is a resonant current in the resonant circuit \( L_R \) and \( C_R \). The current \( I_{OUT} \) is constant so it doesn’t make any voltage on \( L_R \). The resonant process so will be the same as in a serial resonant circuit \( L_R \) and \( C_R \) with zero initial values, which we put a voltage \( U_D \) on. The only difference is that in the time of this process there will flow a resonant current with a DC offset \( I_{OUT} \) in the \( L_R \) in our circuit instead of the only resonant current. The resonant current is defined by a relation:

\[
i_{RES} = i_{RES} \sin \frac{2\pi t}{T_{RES}}
\]

(5)

The \( T_{RES} \) is the period of resonant oscillations. During the resonant process the voltage \( U_{CR} \) is defined:

\[
u_{CR}(t) = U_D \left(1 - \cos \frac{2\pi t}{T_{RES}}\right)
\]

(6)

When the time \( T_{RES}/2 \) passes (positive-going half-wave \( i_{RES} \)), the voltage \( U_{CR} \) has its maximum value \( 2U_D \) (see fig. 2). Now the current \( i_{RES} \) reverses the polarity (negative-going half-wave) and starts to discharge the \( C_R \). The current \( i_L \) through the inductor \( L_R \) falls down because the \( i_{RES} \) now has a negative value (see relation 4).

A very important condition for a good working of the converter is, that the amplitude \( I_{RES} \) of the resonant current is higher than \( I_{OUT} \). Only in this case the \( i_L \) falls to zero (in some while of the negative-going half-wave \( i_{RES} \) and it „wants“ to reverse the polarity which isn’t possible because of the diode \( D_1 \) which closes. The process from the beginn of the negative-going half-wave \( i_{RES} \) till the while of disappearing \( i_L \) takes a time \( t_x \):

\[
x = \frac{\arcsin \frac{I_{OUT}}{I_{RES}}}{2\pi f_{RES}}
\]

(7)

When \( t_x \) passes, the voltage \( U_{CR} \) of capacitor \( C_R \) is:

\[
U_x = U_D \left(1 - \cos 2\pi f_{RES} \left(\frac{T_{RES}}{2} + t_x\right)\right)
\]

(8)

Let’s notice 2 facts: The current \( i_L \) (flowing through the transistor from the \( U_D \)-source) stopped to flow although the transistor is still switched-on and the \( U_x \) is higher than \( U_D \). But the necessary condition for this facts was:

\[
I_{RES} > I_{OUT}
\]

(9)

If (9) wasn’t true, the \( i_L \) wouldn’t disappear and would be broken by switching-off the transistor (switching losses, voltage peak of \( L_R \)).

d) The diode \( D_1 \) continues to be closed while \( U_{CR} > U_D \). After closing the diode \( D_1 \) the current \( I_{OUT} \) can’t flow from the \( U_D \)-source. So it starts to discharge the capacitor \( C_R \). Its voltage \( U_{CR} \) falls linearly down from a initial value \( U_K \) defined by the relation (8). When \( U_{CR} \) reaches zero the diode \( D_0 \) opens again because the \( I_{OUT} \) starts to be kept by \( L_R \) and it flows through the \( D_0 \).

The discharging of capacitor \( C_R \) takes a time \( t_2 \):

\[
t_2 = C_R U_D \frac{1 - \cos 2\pi f_{RES} \left(\frac{T_{RES}}{2} + t_x\right)}{I_{OUT}}
\]

(10)

During \( t_2 \) is the voltage \( U_{CR} \) defined:

\[
u_{CR}(t) = U_D \left(1 - \cos 2\pi f_{RES} \left(\frac{T_{RES}}{2} + t_x\right)\right) - \frac{I_{OUT} \cdot t}{C_R}
\]

(11)
The switch-off control signal for transistor T must come after disappearing \( i_{t} \) (as noticed) but before the \( u_{c} \) falls under \( U_{D} \). If the transistor stayed switched-on although \( u_{c} < U_{D} \), then the diode D1 would open and an unwanted current through the transistor would start to flow.

The new switch-on control signal mustn’t come before the \( u_{c} \) discharges to zero.

We can see that the switching-off comes at a zero current (zero switch-off losses). At the switching-on the current starts to increase so the switch-on losses won’t be zero. However in practice they’re very low (see the part 2).

3. The control system of the converter

The output DC voltage equals to the average value of the voltage \( u_{c} \), because the average value of the voltage on \( L_{T} \) must be zero.

It’s clear that we must control the switching frequency of the converter to reach a regulation of the average value of \( u_{c} \).

The switching frequency needed for one concrete output voltage depends of the output current \( I_{OUT} \). The reason for it is the dependence of durations \( t_{1}, t_{2}, t_{3}, t_{4}, t_{5} \) and \( t_{6} \) on \( I_{OUT} \) (see relations 3, 7, 10). The duration \( t_{2} \) has in practice a dominant influence. However the maximum reachable output voltage is almost independent on \( I_{OUT} \) and we get it when switch-on newly the transistor (next switching cycle) immediately after discharging of capacitor \( C_{R} \) to a zero voltage. (In fact it exists a very weak dependence of the maximum output voltage on \( I_{OUT} \) which is made by dependence of ratios of durations \( t_{1}, t_{2}, t_{3}, t_{4}, t_{5} \) and \( t_{6} \) on \( I_{OUT} \).)

The block diagram of control system shows the fig. 3. The system was designed as self-oscillating in accordance with the dependence of switching frequency on the \( I_{OUT} \) (for one defined value of output voltage).

a) the switch-on control signal is deduced from the voltage \( u_{c} \). As soon as this voltage falls down to zero, the transistor may be switched-on (signal of comparator \( K_{1} \)). The regulation consists in delaying of the real switch-on signal after the signal of comparator \( K_{1} \). The delay \( \Delta t \) is produced in the block called "control delay" and it’s fluently controllable from zero (full output voltage) to \( \Delta t_{\text{max}} \) (minimum output voltage). The output voltage from a standard PI regulator is the control signal for the block "control delay".

b) The switch-off signal must come after disappearing \( i_{t} \), but before falling \( u_{c} \) under \( U_{D} \) (see chap 2, letter d). This time interval is the narrowest when the \( I_{OUT} \) is maximum. In this case the \( t_{6} \) has the longest duration and that’s why the \( u_{c} \) falls down onto its lowest value \( U_{\text{Xmin}} \) (when \( i_{t} \) falls down to zero). That’s why the condition \( I_{RES} > I_{OUT} \) it will be always \( U_{\text{Xmin}} > U_{D} \). It enables to deduce the while of disappearing \( i_{t} \) (switching-off allowed) from the course of the voltage \( u_{t} \), on the inductor \( L_{R} \). This voltage is sensed by an auxiliary winding \( L_{R} \) (see fig. 3). An explanation gives the figure 4.

If the \( L_{R} \) was an ideal inductor, then the \( u_{t} \) would immediately fall down to zero at the same time when the \( i_{t} \) reaches a zero value. However in fact there appeared damped resonant oscillations after closing \( D_{1} \) and disappearing \( i_{t} \) (see fig. 4) because the real coil \( L_{R} \) has its own spurious capacity (parallel-connected to inductivity \( L_{R} \)). The coupling between the auxiliary and main windings is weak and the auxiliary winding is hardly damped by the resistor \( R \). That’s why the noticed spurious oscillations are very effectively damped in the auxiliary winding without damping the main winding (a weak
coupling). A damping in a main winding would cause big losses in the switching cycle of the converter.

The auxiliary winding has its spurious capacity too (in the practice lower than the main one). That’s why it arose a jumble of oscillations in the auxiliary winding without damping by resistor R after disappearing of iL. In the practice it caused an unreliable deduction of the switch-off signal.

The shaping circuits (in front of the RS flip flop) create a short pulse of logical zero when a continuous logical zero comes into their inputs. It guarantees that the active triggering signals (logical zero) for the inputs of RS flip flop are enough time-separated. That’s why no hazards are enabled, although the used comparators could overshoot (one of the inputs set or reset has always the passive logical one value).

4. Conclusions

On the base of this description a converter was constructed. The relations useful for designing will be deduced in the part 2 of this article.

The input voltage of the constructed converter was 300 V, output power 200 W. Resonant frequency 300 kHz and the resonant current amplitude 1.5 A. The minimum duration of switching cycle about 5 μs (200 kHz). The control delay in range of 0.5 μs to 90 μs. The output voltage was controllable in range 10 V to 204 V at the output current 1 A, which is from 3 to 68 % U_d. A MOSFET was used. The switching losses were negligible because the heating of the transistor cover corresponded almost to the calculated resistance losses.

The described system became a base for creating a new converter with a transformer, which contains next 4 commutating transistor switching at a zero voltage. It was constructed with simmilar parameters, the controllability of output voltage was better. Now it’s worked on a power version (5 kW) for arc welding.

References


About author

Pavel VOREL was born in Brno, Czech republic, in 1973. He received the Ing (MSc) from the Technical university of Brno. Dept. of Radioelectronics in 1996. His research interests include switching converters especially in power applications.