KVASIRESONANT DC-DC CONVERTER WITH SWITCHING AT ZERO CURRENT - PART 1

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Abstract

A kvasiresonant DC - DC converter and its control circuits are proposed. The relations useful for design of the converter will be deduced in the part 2.

The fundamental idea of the converter is the switching -on and -off a transistor at zero current. In this way the switching losses are eliminated. It enables to design a converter with a large output power (several kW) , high switching frequency (about 200 kHz), very good efficiency and low radiation.

Keywords

switching losses, resistance losses, resonance, transistor, diode, choke coil, inductor, capacitor, controlling, damping, winding, coupling, comparator, PI regulator, pulse delaying, over-current protection, undervoltage protection

1. Introduction

The basic problem of resonant converters is a difficult regulation. The essential principe of described converter was received from [1] but a new control system was created. The original system used 8 additional switching transistors in the power circuit to reach for 256 levels of the resonant capacity (switched - capacitor - based resonant circuit). It represents additional resistance losses which are not negligible, especially in power applications. The new system uses only one resonant capacitor. That's why there are no additional switching transistors in the converter. The control system operates as a continuous-action controller and the reachable control range isn't reduced.

2. The power circuit of the converter

The sheme of the power circuit showes the fig.1. It differs from the version of [1] only with using a simple resonant capacitor C_R.

The presumption for a good working of the converter is: The inductivity L_F is so high, that the current I_{OUT} is almost constant in a steady state regime.It's no practical problem, becouse the switching frequency is very high.

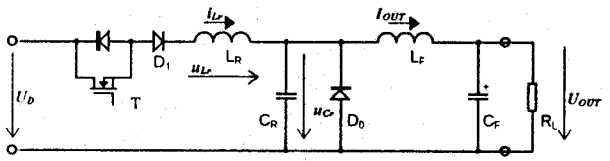

Fig. 1 The power circuit of the converter

The action of one switching cycle in a steady state regime showes the fig. 2. It's necessary to describe it very carefully if we want to explain the control system.

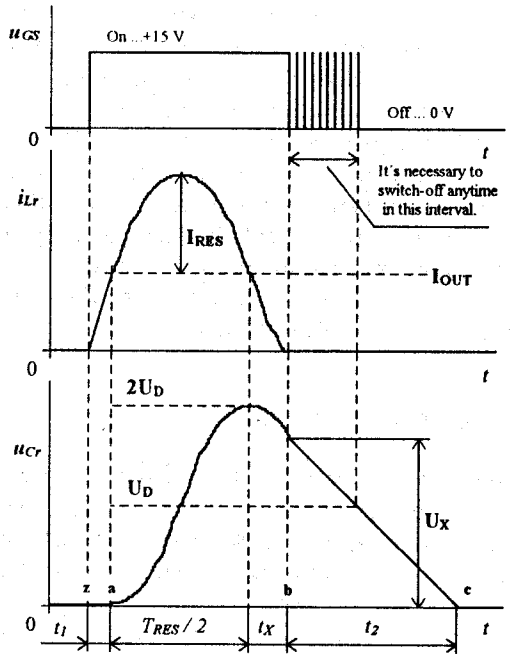

Fig. 2 The action of one switching cycle in a steady state regime

a) Before switching-on the transistor T the constant current I_{OUT} flowes through the diode D_0. Its source is the choke coil L_F. The diode D_0 is open, the voltage u_{Cr} on the capacitor C_R is zero. (We presuppose an ideal diode with zero forward voltage).

b) By switching-on the transistor T we put in fact the input voltage U_D directly onto the inductor L_R becouse the voltage u_{Cr} is zero (open diode D_0).That's why the current i_{Lr} in the inductor L_R starts to increase linearly from a zero initial value. It flowes in fact through the open diode D_0 but „from the katode to the anode"! It's better to say, that the real current through the D_0 („from A to K") will be lower than I_{OUT} becouse it'll be:

$$i_{D_0}(t) = I_{OUT} - i_{L_R}(t) \tag{1}$$

While $i_{Lr} < I_{OUT}$, the diode D_0 continues to be open and the voltage u_{Cr} is zero. The linear increasing of the i_{Lr} can be described with an equation:

$$i_{L_R}(t) = \frac{U_D \cdot t}{L_R} \tag{2}$$

This process ends when passes the time t_1 and i_{Lr} equals to I_{OUT}. In this while the current through diode D_0 reachs a zero value and the diode D_0 closes. From the equation (2) we can deduce a relation for the duration of t_1:

$$t_1 = L_R \frac{I_{OUT}}{U_D} \tag{3}$$

c) Now disappeared the short circuit of C_R, by closing the D_0. The current i_{Lr} in the inductor L_R now can be described with a relation:

$$i_{L_R}(t) = I_{OUT} + i_{RES}(t) \tag{4}$$

The i_{RES} is a resonant current in the resonant circuit L_R and C_R . The current I_{OUT} is constant so it does'nt make any voltage on L_R.The resonant process so will be the same as in a serial resonant circuit L_R and C_R with zero initial values, which we put a voltage U_D on. The only difference is that in the time of this process there will flow a resonant current with a DC offset I_{OUT} in the L_R in our circuit instead of the only resonant current. The resonant current is defined by a relation:

$$i_{RES} = I_{RES} \sin \frac{2\pi\, t}{T_{RES}} \tag{5}$$

The T_{RES} is the period of resonant oscillations. During the resonant process the voltage u_{Cr} is defined:

$$u_{Cr}(t) = U_D\left(1 - \cos\frac{2\pi t}{T_{RES}}\right) \tag{6}$$

When the time $T_{RES}/2$ passes (positive-going half-wave i_{RES}), the voltage u_{Cr} has its maximum value $2U_D$ (see fig. 2). Now the current i_{RES} reverses the polarity (negative-going half-wave) and starts to discharge the C_R. The current i_{Lr} through the inductor L_R falls down becouse the i_{RES} now has a negative value (see relation 4).

A very important condition for a good working of the converter is, that the amplitude I_{RES} of the resonant current is higher than I_{OUT}. Only in this case the i_{Lr} falls to zero (in some while of the negative-going half-wave i_{RES}) and it „wants" to reverse the polarity which isn't possible becouse of the diode D_1 which closes. The process from the beginn of the negative-going half-wave i_{RES} till the while of disappearing i_{Lr} takes a time t_x:

$$t_x = \frac{\arcsin \dfrac{I_{OUT}}{I_{RES}}}{2\pi f_{RES}} \tag{7}$$

When t_x passes, the voltage u_{Cr} of capacitor C_R is:

$$U_X = U_D\left(1 - \cos 2\pi f_{RES}\left(\frac{T_{RES}}{2} + t_x\right)\right) \tag{8}$$

Let's notice 2 facts: The current i_{Lr} (flowing through the transistor from the U_D-source) stopped to flow although the transistor is still switched-on and the U_X is higher than U_D. But the necessary condition for this facts was:

$$I_{RES} > I_{OUT} \tag{9}$$

If (9) wasn't true, the i_{Lr} wouldn't disappearand and would be broken by switching-off the transistor (switching losses, voltage peak of L_R).

d) The diode D_1 continues to be closed while $u_{Cr} > U_D$. After closing the diode D_1 the current I_{OUT} can't flow from the U_D-souce. So it starts to discharge the capacitor C_R. Its voltage u_{Cr} falls linearly down from a initial value U_X defined by the relation (8). When u_{Cr} reachs zero the diode D_0 opens again becouse the I_{OUT} starts to be kept by L_F and it flowes through the D_0.

The discharging of capacitor C_R takes a time t_2:

$$t_2 = \frac{C_R U_D}{I_{OUT}}\left(1 - \cos 2\pi f_{RES}\left(\frac{T_{RES}}{2} + t_x\right)\right) \tag{10}$$

During t_2 is the voltage u_{Cr} defined:

$$u_{Cr}(t) = U_D\left(1 - \cos 2\pi f_{RES}\left(\frac{T_{RES}}{2} + t_x\right)\right) - \frac{I_{OUT} \cdot t}{C_R} \tag{11}$$

The switch-off control signal for transistor T must come after disappearing i_{Lr} (as noticed) but before the u_{Cr} falls under U_D. If the transistor stayed switched-on although $u_{Cr} < U_D$, then the diode D_1 would open and an unwanted current through the transistor would start to flow.

The new switch-on control signal mustn't come before the u_{Cr} discharges to zero.

We can see that the switching-off comes at a zero current (zero switch-off losses). At the switching-on the current starts to increase so the switch-on losses won't be zero. However in practice they're very low (see the part 2).

3. The control system of the converter

The output DC voltage equals to the average value of the voltage u_{Cr} becouse the average value of the voltage on L_F must be zero.

It's clear that we must control the switching frequency of the converter to reach a regulation of the average value of u_{Cr}.

The switching frequency needed for one concrete output voltage depends of the output current I_{OUT}. The reason for it is the dependence of durations t_1,t_2 and t_x on I_{OUT} (see relations 3, 7 ,10). The duration t_2 has in practice a dominant influence. However the maximum reachable output voltage is almost independent on I_{OUT} and we get it when switch-on newly the transistor (next switching cycle) immediately after discharging of capacitor C_R to a zero voltage. (In fact it exists a very weak dependence of the maximum output voltage on I_{OUT} which is made by dependence of ratios of durations t_1 ,t_2 ,$T_{REZ}/2$ and t_x on I_{OUT}.)

The block diagram of control system showes the fig. 3. The system was designed as self-oscillating in accordance with the dependence of switching frequency on the I_{OUT} (for one defined value of output voltage).

a) the switch-on control signal is deduced from the voltage u_{Cr}. As soon as this voltage falls down to zero, the transistor may be switched-on (signal of comparator K_1). The regulation consists in delaying of the real switch-on signal after the signal of comparator K_1. The delay Δt is produced in the block called „control delay" and it's fluently controllable from zero (full output voltage) to Δt_{max} (minimum output voltage). The output voltage from a standard PI regulator is the control signal for the block „control delay".

b) The switch-off signal must come after disappearing i_{Lr} but before falling u_{Cr} under U_D (see chap 2.,letter d). This time interval is the narrowest when the I_{OUT} is maximum. In this case the t_x has the longest duration and that's why the u_{Cr} falls down onto its lowest value U_{Xmin} (when i_{Lr} falls down to zero). Thanks the condition $I_{RES} > I_{OUT}$ it will be always $U_{Xmin} > U_D$. It enables to deduce the while of disappearing i_{Lr} (switching-off allowed) from the course of the voltage u_{Lr} on the inductor L_R. This voltage is sensed by an auxiliary winding L_R' (see fig. 3). An explanation gives the figure 4.

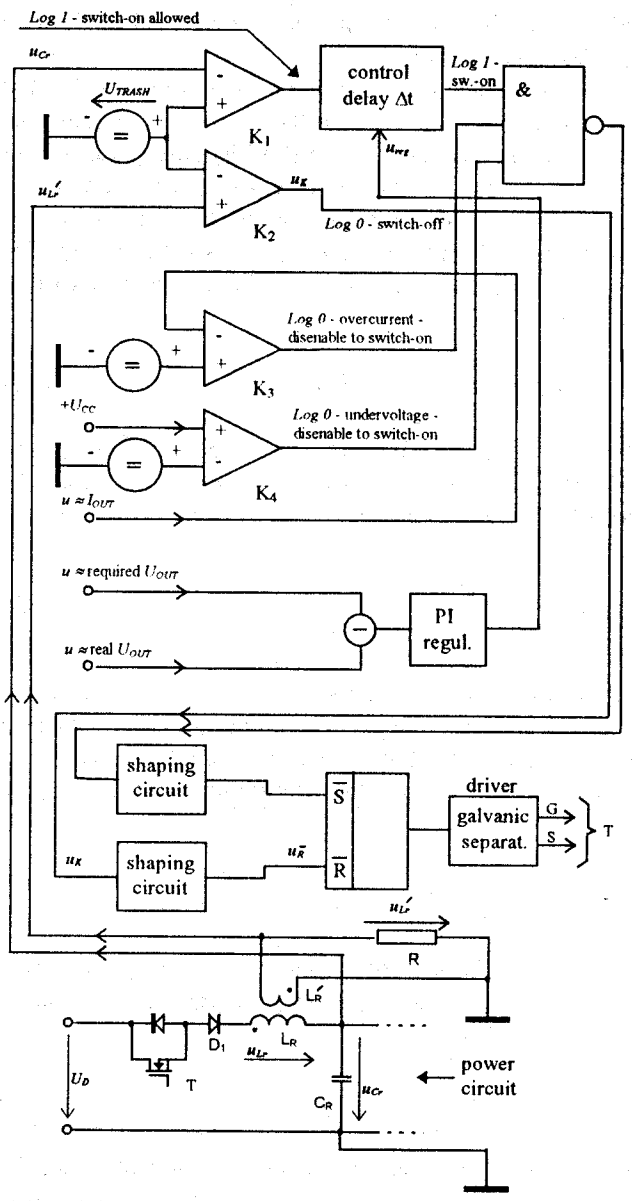

Fig. 3 The block diagram of control system

If the L_R was an ideal inductor, then the u_{Lr} would immediately fall down to zero at the same time when the i_{Lr} reachs a zero value. However in fact there appeared damped resonant oscillations after closing D_1 and disappearing i_{Lr} (see fig. 4) becouse the real coil L_R has its own spurious capacity (parallel-connected to inductivity L_R). The coupling between the auxiliary and main windings is weak and the auxiliary winding is hardly damped by the resistor R. That's why the noticed spurious oscillations are very effectively damped in the auxiliary winding withouth damping the main winding (a weak

coupling). A damping in a main winding would cause big losses in the switching cycle of the converter.

The auxiliary winding has its spurious capacity too (in the practice lower than the main one). That's why it arose a jumble of oscillations in the auxiliary winding without damping by resistor R after disappearing of i_{Lr}. In the practice it caused a unreliable deducation of the switch-off signal.

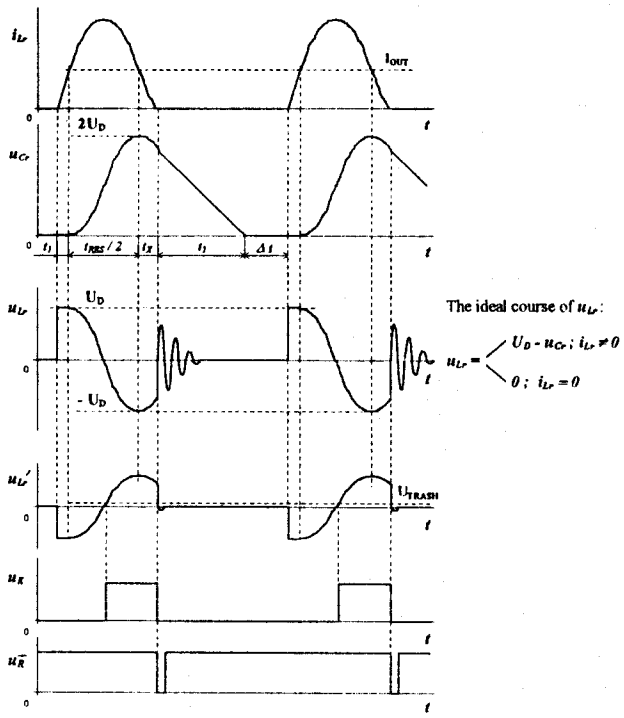

Fig. 4 The obtaining of switch-off signal from the voltage on L_R

c) The PI regulator is realized with an operational amplifier. It's a standard system of PI regulator. We can regulate the output voltage or output current according to the sensed signal (U_{OUT} or I_{OUT}).

d) It's necessary to use a fast over-current protection in the converter (comparator K_3), even also in the case when the PI regulator regulates the output current becouse the regulation response will be certainly very slow and it couldn't hinder a dangerous increasing of the output current if the output would be suddenly short-circuited (for example). When the current increases over a defined value the comparator K_3 locks a new switching-on the transistor. (But it doesn't make a premature switching-off which would be dangerous). So the output current is kept under a defined value by a prolongation the duration of the regulation delay Δt.

e) The undervoltage protection (comparator K_4) must hinder a new switching-on, while the supply voltage of the control circuits is too low. If the transistor was driven by a low gate-to-source voltage it could cause an imperfect switching with dangerous losses in the switched-on state.

The shaping circuits (in front of the RS flip flop) create a short pulse of logical zero when a continuous logical zero comes into their inputs. It guarantees that the active triggering signals (logical zero) for the inputs of RS flip flop are enough time-separed. That's why no hazards are enabled, although the used comparators could overshoot (one of the inputs set or reset has always the passive logical one value).

4. Conclusions

On the base of this description a converter was constructed. The relations useful for designing will be deduced in the part 2 of this article.

The input voltage of the constructed converter was 300 V, output power 200 W. Resonant frequency 300 kHz and the resonant current amplitude 1,5 A. The minimum duration of switching cycle about 5 μs (200 kHz). The control delay in range of 0.5 μs to 90 μs. The output voltage was controllable in range 10 V to 204 V at the output current 1 A, which is from 3 to 68 % U_D. A MOSFET was used. The switching losses were negligible becouse the heating of the transistor cover corresponded almost to the calculated resistance losses.

The described system became a base for creating a new converter with a transformer, which contains next 4 commutating transistor switching at a zero voltage. It was constructed with simmilar parameters, the controllability of output voltage was better. Now it's worked on a power version (5 kW) for arc welding.

References

[1] CHEN, J. -IOINOVICI, A: Switching - Mode DC-DC Converter with Switched-Capacitor-Based Resonant Circuit, IEEE Transaction on circuits and systems - I : Fundamental theory and applications, Vol. 43, No. 11, November 1996

About author

Pavel VOREL was born in Brno, Czech republic, in 1973. He received the Ing (MSc) from the Technical university of Brno, Dept. of Radioelectronics in 1996. His research interests include switching converters especially in power applications.