KVASIRESONANT DC-DC CONVERTER WITH SWITCHING AT ZERO CURRENT - PART 2

Pavel VOREL
Dept. of Radioelectronics
Technical University of Brno
Purkyňova 118, 602 00 Brno
Czech Republic

Abstract

A kvasiresonant DC - DC converter and its control circuits were proposed in the part 1 of the article. The relations useful for design of the converter will be deduced in this part 2. Relations and their numbers of the part 1will be accepted.

Keywords

switching losses, resistance losses, resonance, transistor, diode, choke coil, inductor, capacitor, controlling, pulse delaying

1. The design of the power circuit (useful relations)

1.1 The resonant current amplitude

The amplitude I_{RES} must realize the basic condition (7). Let's choose:

$$I_{RES} = 1{,}2 I_{OUT\max} \tag{12}$$

I_{OUTmax} means the maximum allowed output current.
If we have chosen higher I_{RES}, we would need a lower L_R and higher C_R (see later) for a given resonant frequency. When L_R is lower, the duration of t_1 is shorter (relation (3)) and the maximum reachable output voltage is higher. (in the time interval t_1 is the u_{Cr} zero.)

1.2 The values of L_R and C_R

This values are binded by relations for f_{RES} and I_{RES}.

$$f_{RES} = \frac{1}{2\pi\sqrt{L_R C_R}} \tag{13}$$

$$\frac{U_D}{I_{RES}} = \sqrt{\frac{L_R}{C_R}} \tag{14}$$

By using (12), (13) and (14) we deduce:

$$C_R = \frac{1{,}2 I_{OUT\max}}{2\pi U_D f_{RES}} \tag{15}$$

$$L_R = \frac{1}{4\pi^2 f_{RES}^2 C_R} \tag{16}$$

1.3 The maximum output voltage

Let's indicate the duration of a switching cycle t_C. The minimum t_C value (for the maximum output voltage) is given by relation:

$$t_{C\min} = t_1 + \frac{T_{RES}}{2} + t_X + t_2 \tag{17}$$

The duration of t_1, t_X and t_2 (see (3), (7), (10)) are dependent on the I_{OUT}. That's why the t_{Cmin} is dependent too. There is the dominant influence of t_2.

The integral of voltage u_{Cr} in the time of one switching cycle is (indicated A):

$$A = \int_a^c u_{Cr}\,dt \tag{18}$$

u_{Cr} is defined by function (6) in the interval (a,b) and by function (11) in the interval (b,c). For a,b,c see the fig.2 in the part 1. After solving the integral we get:

$$A = U_D\left[\frac{T_{RES}}{2} + t_X - \frac{\sin 2\pi f_{RES}\left(\frac{T_{RES}}{2} + t_X\right)}{2}\right] + U_D\frac{t_2\left(1 - \cos 2\pi f_{RES}\left(\frac{T_{RES}}{2} + t_X\right)\right)}{2} \tag{19}$$

The value of A depends on t_1, t_X and t_2 again, which means on I_{OUT}.

Now the maximum output voltage:

$$U_{CrAV\max} = \frac{A}{t_{C\min}} \tag{20}$$

The $U_{CrAVmax}$ is almost independent on I_{OUT}. However let's calculate the $U_{CrAVmax}$ by using the I_{OUTmax}. It's the worst case - thanks the short t_2 the influence of t_1 (where u_{Cr} is zero) gets an importance and the maximum output voltage is the lowest. We can notice: $U_{CrAVmax} < U_D$ in every case.

1.4 The necessary range of regulation delay

The maximum delay Δt_{max} corresponds to the minimum output voltage at the minimum output current, becouse the output voltage is given by a relation:

$$U_{CrAV} = \frac{A}{t_1 + \frac{T_{RES}}{2} + t_X + \Delta t} \tag{21}$$

From where:

$$\Delta t_{max} = \frac{A_{max}}{U_{CrAV\,min}} - \left(t_1 + \frac{T_{RES}}{2} + t_X + t_2\right) \tag{22}$$

The A becomes A_{max} just at the minimum I_{OUT} (see (19), (3), (7), (10)). The resultat: Before calculating (22) we calculate t_1, t_2, t_X and A_{max} by using the minimum I_{OUT} (needed relations (3), (7), (10) and (19)).

1.5 The power dimensioning of the transistor

1.5.1 Resistance losses (in a switch-on state)

The loss power is:

$$P_1 = R_{DSon} \cdot I^2_{Drms} \tag{23}$$

The relation assumes a MOSFET. R_{DSon} is the resistnce in the switch-on state, I_{Drms} is the root-mean-square value of the current i_{Lr} flowing through the transistor.

$$I^2_{Drms} = \frac{1}{t_{C\,min}} \int_a^b i^2_{Lr} dt = \frac{1}{t_{C\,min}} \int_0^{t_1} \left(\frac{I_{OUT\,max}}{t_1} t\right)^2 dt + \frac{1}{t_{C\,min}} \int_0^{\frac{T_{RES}}{2}+t_X} \left(I_{RES} \sin 2\pi f_{RES} t + I_{OUT\,max}\right)^2 dt \tag{24}$$

After solving:

$$I_{Drms\,max} = \sqrt{\frac{1}{t_{C\,min}}(E + F + G)} \tag{25}$$

$$E = \frac{I^3_{OUT\,max}}{3} t_1 \tag{26}$$

$$F = \left(\frac{T_{RES}}{2} + t_X\right) \cdot \left(I^2_{OUT\,max} + \frac{I^2_{RES}}{2}\right) \tag{27}$$

$$G = \frac{I_{OUT\,max} I_{RES}}{\pi f_{RES}} \left(1 - \cos 2\pi f_{RES}\left(\frac{T_{RES}}{2} + t_X\right)\right) - \frac{I^2_{RES} \sin 4\pi f_{RES}\left(\frac{T_{RES}}{2} + t_X\right)}{8\pi f_{RES}} \tag{28}$$

1.5.2 Switching losses

The switching losses appear only by switching-on in this converter. The course of i_{Cr} (resp. i_D) in the duration t_1 is:

$$i_D = I_{OUT} \frac{t}{t_1} \tag{29}$$

(We assume a linearity neglecting the influence of imperfect switching state in the duration of switching process.)

Let's assume a linearly increasing conductivity drain--source (g_{DS}) in the duration of switching process. In fact the course of g_{DS} is less advantageous.

$$g_{DS} = \frac{t}{t_{on}} \cdot \frac{1}{R_{DSon}} \tag{30}$$

where t_{on} is the duration of switching process.

The energy converted into heat in one switching process is:

$$W_{on} = \int_0^{t_{on}} \frac{i^2_D}{g_{DS}} dt \tag{31}$$

By using (29) and (30) and solving the integral we get:

$$W_{on} = \frac{I^2_{OUT} \cdot t^3_{on}}{2t^2_1} \cdot R_{DSon} \tag{32}$$

Then the switching power losses:

$$P_{on} = \frac{W_{on}}{t_C} = \frac{I^2_{OUT} \cdot t^3_{on}}{2t^2_1} \cdot R_{DSon} \cdot \frac{1}{t_C} \tag{33}$$

The maximum P_{on} corresponds to the maximum of I_{OUT} and minimum t_{Cmin} (maximum output voltage). If we use a transistor with $t_{on} < t_1$ then the P_{on} is in practice very low thanks the t^3_{on}. ($P_{on} = 2$W at $I_{OUT} = 20$A, $t_C = 5\mu$s, $t_{on} = t_1 = 500$ns, $R_{DSon} = 0{,}1\Omega$)

The total power losses are:

$$P_{tot} = P_1 + P_{on} \tag{34}$$

1.6 The voltage and current dimensioning of the transistor

The maximum D-S voltage:

$$U_{DSm} = U_D \tag{35}$$

The peak drain current (see the part 1, fig. 2, course of i_{Lr}):

$$I_{Dm} = I_{RES} + I_{OUT} \tag{36}$$

the worst case (maximum) of the average value of drain current:

$$I_{DAV\max} = \frac{1}{t_C} \cdot \int_z^b i_{Lr} dt \tag{37}$$

It's not necessary to solve this integral when we appreciate following:
The power input of the converter:

$$P_1 = U_D \cdot I_{AV} \tag{38}$$

The reason for that relation is the constant U_D.
The output power is:

$$P_2 = U_{CrAV} \cdot I_{OUT} \tag{39}$$

At the theoretical efficiency 100% the P_1 equals to P_2. That's why we can write:

$$I_{DAV\max} = \frac{U_{CrAV\max} \cdot I_{OUT\max}}{U_D} \tag{40}$$

1.7 The dimensioning of the diode D_1

The maximum reverse voltage:

$$U_{Rm} = U_D \tag{41}$$

the peak forward current by (36), average forward current by (40)
The power losses:

$$P_Z = U_F \cdot I_{DAV\max} \tag{42}$$

where U_F is the forward voltage.

1.8 The dimensioning of the diode D_0

The maximum reverse voltage:

$$U_{RM} = 2U_D \tag{43}$$

the peak forward current:

$$I_{FM} = I_{OUT\max} \tag{44}$$

the average forward current:

$$I_{FAV} = I_{OUT} - I_{DAV} \tag{45}$$

Its worst case comes at I_{OUTmax} and U_{OUTmin}. Then by using (40) for I_{DAV} we get:

$$I_{FAV\max} = I_{OUT\max} - \frac{U_{CRAV\min} I_{OUT\max}}{U_D} \tag{46}$$

the power losses:

$$P_Z = U_F \cdot I_{FAV\max} \tag{47}$$

where U_F is the forward voltage.

1.9 The design of the inductivity L_F

The inductivity of choke L_F influences the ripple of the current I_{OUT} which must be low becouse of the described principe of the converter, becouse of the output voltage-ripple and the electromagnetic radiation.

The worst case for the ripple of I_{OUT} comes, when the rise of current I_{OUT} (in the duration of $u_{Cr} > 0$) is highest and it is:

$$\Delta i_{OUT} = \frac{1}{L_F} \int_a^c u_{CR} dt = \frac{A}{L_F} \tag{48}$$

The maximum ripple Δi_{OUTmax} corresponds to the A_{max}. It comes at the minimum I_{OUT}. We calculate the A_{max} by using (3), (7), (10) and finally (19) with I_{OUTmin}. Then the L_F will be from (48):

$$L_F = \frac{A_{\max}}{\Delta i_{OUT\max}} \tag{49}$$

We choose the Δi_{OUTmax} several % of I_{RES}, not to damage slightly the operating of the converter.

At $I_{OUT} > I_{OUTmin}$ its ripple will be lower (becouse of A). For a higher output voltage it will be lower too. The minimum I_{OUT}-ripple we get in a full action of the converter, at U_{OUTmax} and I_{OUTmax}.

2. Conclusions

The basic power circuit of this converter was modified (it's not described in this article) to hinder the dependence of the u_{Cr}-pulse-width on I_{OUT}. It enabled to construct a simple and more reliable control system with a constant switching frequency. The regulation contains in dropping of switching pulses.
This new converter became a base for creating a converter with transformer. It was designed and constructed as a power source for arc welding (max. 120 A, 4500 W). Its switching frequency is 150 kHz and the weight of the whole device is 5,5 kg. It was designed to enable a continuous consumption.

References

[1] CHEN, J. -IOINOVICI, A: Switching - Mode DC-DC Converter with Switched-Capacitor-Based Resonant Circuit, IEEE Transaction on circuits and systems - I : Fundamental theory and applications, Vol. 43, No. 11, November 1996

About author

Pavel VOREL was born in Brno, Czech republic, in 1973. He received the Ing (MSc) from the Technical university of Brno, Dept. of Radioelectronics in 1996. His research interests include switching converters especially in power applications.