KVASIRESONANT DC-DC CONVERTER WITH SWITCHING AT ZERO CURRENT - PART 2

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Abstract

A kvasiresonant DC - DC converter and its control circuits were proposed in the part 1 of the article. The relations useful for design of the converter will be deduced in this part 2. Relations and their numbers of the part 1 will be accepted.

Keywords

switching losses, resistance losses, resonance, transistor, diode, choke coil, inductor, capacitor, controlling, pulse delaying

1. The design of the power circuit (useful relations)

1.1 The resonant current amplitude

The amplitude $I_{RES}$ must realize the basic condition (7). Let’s choose:

$$I_{RES} = 1.2 I_{OUT_{max}}$$  \hspace{1cm} (12)

$I_{OUT_{max}}$ means the maximum allowed output current. If we have chosen higher $I_{RES}$, we would need a lower $L_R$ and higher $C_R$ (see later) for a given resonant frequency. When $L_R$ is lower, the duration of $t_1$ is shorter (relation (3)) and the maximum reachable output voltage is higher. (in the time interval $t_1$ is the $u_{OC}$ zero.)

1.2 The values of $L_R$ and $C_R$

This values are binded by relations for $f_{RES}$ and $I_{RES}$:

$$f_{RES} = \frac{1}{2\pi \sqrt{L_R C_R}}$$  \hspace{1cm} (13)

$$\frac{U_D}{I_{RES}} = \sqrt{\frac{L_R}{C_R}}$$  \hspace{1cm} (14)

By using (12), (13) and (14) we deduce:

$$C_R = \frac{1.2 I_{OUT_{max}}}{2\pi U_D f_{RES}}$$  \hspace{1cm} (15)

$$L_R = \frac{1}{4\pi^2 f_{RES}^2 C_R}$$  \hspace{1cm} (16)

1.3 The maximum output voltage

Let’s indicate the duration of a switching cycle $t_c$. The minimum $t_c$ value (for the maximum output voltage) is given by relation:

$$t_{c_{min}} = t_1 + \frac{T_{RES}}{2} + t_x + t_2$$  \hspace{1cm} (17)

The duration of $t_1$, $t_x$ and $t_2$ (see (3), (7), (10)) are dependent on the $I_{OUT}$. That’s why the $t_{c_{min}}$ is dependent too. There is the dominant influence of $t_2$.

The integral of voltage $u_{OC}$ in the time of one switching cycle is (indicated $A$):

$$A = \int u_{OC} \, dt$$  \hspace{1cm} (18)

$u_{OC}$ is defined by function (6) in the interval (a,b) and by function (11) in the interval (b,c). For a,b,c see the fig.2 in the part 1. After solving the integral we get:

$$A = U_D \left[ \frac{T_{RES}}{2} + t_x - \frac{\sin 2\pi f_{RES} \left( \frac{T_{RES}}{2} + t_x \right)}{2} \right]$$  

$$+ U_D \left[ t_2 \left( 1 - \cos 2\pi f_{RES} \left( \frac{T_{RES}}{2} + t_x \right) \right) \right]$$  \hspace{1cm} (19)

The value of $A$ depends on $t_1$, $t_x$ and $t_2$ again, which means on $I_{OUT}$.

Now the maximum output voltage:

$$U_{OC_{max}} = \frac{A}{t_{c_{min}}}$$  \hspace{1cm} (20)
The $U_{CV \text{max}}$ is almost independent on $I_{OUT}$. However let's calculate the $U_{CV \text{max}}$ by using the $I_{OUT \text{max}}$. It's the worst case - thanks the short $t_s$ the influence of $t_i$ (where $u_C$ is zero) gets an importance and the maximum output voltage is the lowest. We can notice: $U_{CV \text{max}} < U_D$ in every case.

### 1.4 The necessary range of regulation delay

The maximum delay $\Delta t_{\text{max}}$ corresponds to the minimum output voltage at the minimum output current, because the output voltage is given by a relation:

$$ U_{CV} = \frac{A}{t_i + \frac{T_{RES}}{2} + t_x + \Delta t} \quad (21) $$

From where:

$$ \Delta t_{\text{max}} = \frac{A_{\text{max}}}{U_{CV \text{max}}} - \left( t_i + \frac{T_{RES}}{2} + t_x + t_s \right) \quad (22) $$

The $A$ becomes $A_{\text{max}}$ just at the minimum $I_{OUT}$ (see (19), (3), (7), (10)). The result: Before calculating (22) we calculate $t_i$, $t_s$, $t_x$ and $A_{\text{max}}$ by using the minimum $I_{OUT}$ (needed relations (3), (7), (10) and (19)).

### 1.5 The power dimensioning of the transistor

#### 1.5.1 Resistance losses (in a switch-on state)

The loss power is:

$$ P_i = R_{DS\text{on}} \cdot I_{D\text{rms}} \quad (23) $$

The relation assumes a MOSFET. $R_{DS\text{on}}$ is the resistance in the switch-on state, $I_{D\text{rms}}$ is the root-mean-square value of the current $i_d$ flowing through the transistor.

$$ I_{D\text{rms}}^2 = \frac{1}{t_{C\text{min}}} \int_{0}^{t_i} \left( I_{OUT \text{max}} \cdot t \right)^2 dt + \frac{T_{RES}}{2} \int_{0}^{t_{C\text{min}}} \left( I_{RES} \sin 2\pi f_{RES} t + I_{OUT \text{max}} \right)^2 dt $$

After solving:

$$ I_{D\text{rms\,max}} = \frac{1}{t_{C\text{min}}} \left( E + F + G \right) \quad (25) $$

$$ E = \frac{I_{OUT \text{max}}^3}{3} t_i \quad (26) $$

$$ F = \left( \frac{T_{RES}}{2} + t_x \right) \left( I_{OUT \text{max}}^2 + I_{RES}^2 \right) \quad (27) $$

$$ G = \frac{I_{OUT \text{max}}}{\pi f_{RES}} \left( 1 - \cos 2\pi f_{RES} \left( \frac{T_{RES}}{2} + t_x \right) \right) - \frac{I_{RES}^2}{8\pi f_{RES}} \frac{\sin 4\pi f_{RES} \left( \frac{T_{RES}}{2} + t_x \right)}{8\pi f_{RES}} \quad (28) $$

#### 1.5.2 Switching losses

The switching losses appear only by switching-on in this converter. The course of $i_C$ (resp. $i_D$) in the duration $t_s$ is:

$$ i_D = \frac{t}{t_i} \quad (29) $$

(We assume a linearity neglecting the influence of imperfect switching state in the duration of switching process.)

Let's assume a linearly increasing conductivity drain-source ($g_{DS}$) in the duration of switching process. In fact the course of $g_{DS\text{on}}$ is less advantageous.

$$ g_{DS} = \frac{t}{t_{on}} \frac{1}{R_{DS\text{on}}} \quad (30) $$

where $t_{on}$ is the duration of switching process.

The energy converted into heat in one switching process is:

$$ W_{on} = \int_{0}^{t_{on}} I_{D}^2 \cdot dt \quad (31) $$

By using (29) and (30) and solving the integral we get:

$$ W_{on} = \frac{I_{OUT}^2 \cdot t_{on}^3}{2t_i^2} \cdot R_{DS\text{on}} \quad (32) $$

Then the switching power losses:

$$ P_{on} = \frac{W_{on}}{t_C} = \frac{I_{OUT}^2 \cdot t_{on}^3}{2t_i^2} \cdot R_{DS\text{on}} \cdot \frac{1}{t_C} \quad (33) $$

The maximum $P_{on}$ corresponds to the maximum of $I_{OUT}$ and minimum $t_{C\text{min}}$ (maximum output voltage). If we use a transistor with $t_{on} < t_i$, then the $P_{on}$ is in practice very low thanks the $t_{on}^3$ ($P_{on} = 2W$ at $I_{OUT} = 20A$, $t_C = 5\mu s$, $t_{on} = t_i = 500ns$, $R_{DS\text{on}} = 0,1\Omega$)

The total power losses are:

$$ P_{tot} = P_i + P_{on} \quad (34) $$
1.6 The voltage and current dimensioning of the transistor

The maximum D-S voltage:
\[ U_{DSm} = U_D \]  
(35)

The peak drain current (see the part 1, fig. 2, course of \( i_L \)):
\[ I_{DM} = I_{RES} + I_{OUT} \]  
(36)

The worst case (maximum) of the average value of drain current:
\[ I_{DAV_{\text{max}}} = \frac{1}{t_C} \int_0^b i_L \, dt \]  
(37)

It is not necessary to solve this integral when we appreciate following:
The power input of the converter:
\[ P_1 = U_D \cdot I_{AV} \]  
(38)

The reason for that relation is the constant \( U_D \).
The output power is:
\[ P_2 = U_{CR\text{max}} \cdot I_{OUT} \]  
(39)

At the theoretical efficiency 100% the \( P_1 \) equals to \( P_2 \).
That’s why we can write:
\[ I_{DAV_{\text{max}}} = \frac{U_{CR\text{max}} \cdot I_{OUT_{\text{max}}}}{U_D} \]  
(40)

1.7 The dimensioning of the diode \( D_1 \)

The maximum reverse voltage:
\[ U_{Rm} = U_D \]  
(41)

the peak forward current by (36), average forward current by (40)

The power losses:
\[ P_2 = U_F \cdot I_{DAV_{\text{max}}} \]  
(42)

where \( U_F \) is the forward voltage.

1.8 The dimensioning of the diode \( D_0 \)

The maximum reverse voltage:
\[ U_{RM} = 2U_D \]  
(43)

the peak forward current:
\[ I_{RM} = I_{OUT_{\text{max}}} \]  
(44)

the average forward current:
\[ I_{FAV} = I_{OUT} - I_{DAV} \]  
(45)

Its worst case comes at \( I_{OUT_{\text{max}}} \) and \( U_{OUT_{\text{min}}} \). Then by using (40) for \( I_{DAV} \) we get:
\[ I_{FAV_{\text{max}}} = I_{OUT_{\text{max}}} - \frac{U_{CR\text{min}} \cdot I_{OUT_{\text{max}}}}{U_D} \]  
(46)

the power losses:
\[ P_2 = U_F \cdot I_{FAV_{\text{max}}} \]  
(47)

where \( U_F \) is the forward voltage.

1.9 The design of the inductivity \( L_F \)

The inductivity of choke \( L_F \) influences the ripple of the current \( I_{OUT} \) which must be low because of the described princip of the converter, because of the output voltage-ripple and the electromagnetic radiation.

The worst case for the ripple of \( I_{OUT} \) comes, when the rise of current \( I_{OUT} \) in the duration of \( u_C > 0 \) is highest and it is:
\[ \Delta I_{OUT} = \frac{1}{L_F} \int_0^c i_C \cdot \Delta u_C \, dt = \frac{A}{L_F} \]  
(48)

The maximum ripple \( \Delta I_{OUT_{\text{max}}} \) corresponds to the \( A_{\text{max}} \). It comes at the minimum \( I_{OUT} \). We calculate the \( A_{\text{max}} \) by using (3), (7), (10) and finally (19) with \( I_{OUT_{\text{min}}} \). Then the \( L_F \) will be from (48):
\[ L_F = \frac{A_{\text{max}}}{\Delta I_{OUT_{\text{max}}}} \]  
(49)

We choose the \( \Delta I_{OUT_{\text{max}}} \) several % of \( I_{RES} \) not to damage slightly the operating of the converter.

At \( I_{OUT} > I_{OUT_{\text{max}}} \) its ripple will be lower (because of \( A \)). For a higher output voltage it will be lower too. The minimum \( I_{OUT} \)-ripple we get in a full action of the converter, at \( I_{OUT_{\text{max}}} \) and \( I_{OUT_{\text{min}}} \).

2. Conclusions

The basic power circuit of this converter was modified (it’s not described in this article) to hinder the dependence of the \( u_C \)-pulse-width on \( I_{OUT} \). It enabled to construct a simple and more reliable control system with a constant switching frequency. The regulation contains in dropping of switching pulses.

This new converter became a base for creating a converter with transformer. It was designed and constructed as a power source for arc welding (max. 120 A, 4500 W). Its switching frequency is 150 kHz and the weight of the whole device is 5,5 kg. It was designed to enable a continuous consumption.

References


About author

Pavel VOREL was born in Brno, Czech republic, in 1973. He received the Ing (MSc) from the Technical university of Brno, Dept. of Radioelectronics in 1996. His research interests include switching converters especially in power applications.