A PC CONTROLLED FILTER

Sigfredo Pagel, Fernando Pérez Fontán
Dept. de Tecnol. de las Comunicaciones
ETSE de Telecomunicación de Vigo
Campus Universitario
Vigo - ESPAÑA
E-mail: spagel @tsc.uvigo.es,
fpfontan @tsc.uvigo.es

Michel Van Looy
Hoger Instituut der Kempen

Abstract

In this paper we present a switched capacitor filter design using the SC22324 IC, which is fitted with an E^2PROM. It contains four digitally programmable switched-capacitor filter sections, in order to obtain different responses. The SC22324 also contains the on-chip RAM. We'd like to explain, how could the on-chip RAM controlled via a PC. In this way the chip may be used afterwards with a menu where the user may select the wanted parameters.

Keywords

low-pass filter, switched-capacitor (SC), interface, biquad-section, random access memory (RAM)

1. Introduction

Some time ago, we supervised a final student project involved with the switched capacitor filter chip SC22324. Once the student developed his project: "Programming and practical realization of switched-capacitor elliptic filters", he consequently programmed the chip into a fixed filter configuration by storing filter coefficients in the on-chip Electrically Erasable Programmable Read Only Memory (E^2PROM). Then he developed an electronic circuit, so that the chip could be tested. The necessary equipment to program the chip was provided by Sierra Semiconductor.

One of the sixteen different transfer functions, given in the z-domain, can be realized with each section of the chip. So, to realize a certain response, it has to be choosen one specific transfer function. We also need to know the value of the coefficients of the transfer function. Depending on the restrictions to the Bode plot, one

transfer function might not be enough. In that case it will be necessary to combine two or more, maximum up to four, transfer functions. The choice of the transfer function(s) and the value of each coefficient computation can be done by the BIQUAD.EXE, program supplied by Sierra.

As we said before, the SC22324 also contains an on-chip Random Access Memory (RAM). It would be even more interesting now, to have the chance to program the on-chip RAM. This would therefore enable the chip to be used afterwards for didactic purposes.

A personal computer will be used to program the on-chip RAM. A specific interface will be necessary because the personal computer has not the same technology as the chip. The development of the interface, with an array of optocouplers, will be discussed later. Now, it will be explained how the actual chip should be programmed. Finally will be given a very brief description about the program itself. The programming language Turbo Pascal 5.0 was used to realize the program.

2. The SC22324

The block diagram of the programmable universal filter is shown below in figure 1.
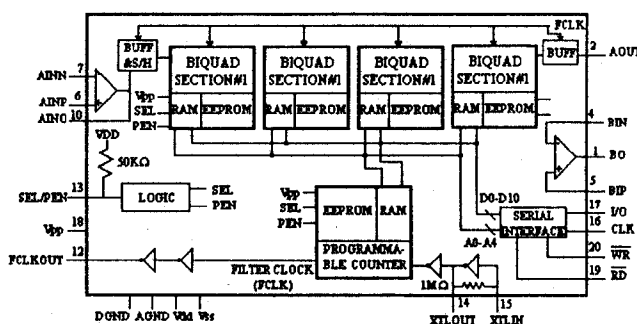

Fig. 1. Block diagram of the SC2234

2.1 General Description

The chip consists of four independently programmable biquad sections which may be configured through digital programming to achieve filter responses of $8th$ order or less. Each chip has an uncommitted operational amplifier at the input to facilitate implementation of an anti-aliasing section to eliminate aliasing effects in the subsequent switched-capacitor filters. The output of the op amp is followed by a buffer section that acts as a sample and hold (S/H) stage. The buffer feeds the signal to the biquad stages. The four

biquad sections can be configured as one, two, three or four cascaded sections. The output of the last cascaded stage is connected to an output buffer which drives the output pin. At the output there is another uncommitted op amp which can be used to implement a smoothing filter for removing the clock noise from the output signal.

The clock for the filter is supplied from an on-chip oscillator that needs an external crystal with an internal programmable counter. *The counter can be programmed through the serial interface by an 8 bit word.*

The chip use a four pin serial interface for communication (for pin descriptions see Handbook Sierra Semiconductor). Sixteen bits are shifted into the chip, where five bits constitute the destination's address and eleven bits the data. The bidirectional input/output (I/O) pin allows reading back the contents of the internal registers for diagnostic purposes.

2.2 Biquad Sections

Each biquad filter section can be programmed to achieve one of the following functions: band-pass, low-pass, low pass notch, high-pass, high-pass notch, notch and all-pass filter responses. Any combinations of these sections can be used to form 2nd, 4th, 6th or 8th order filters. The block diagram of the programmable biquad is shown in figure 2.
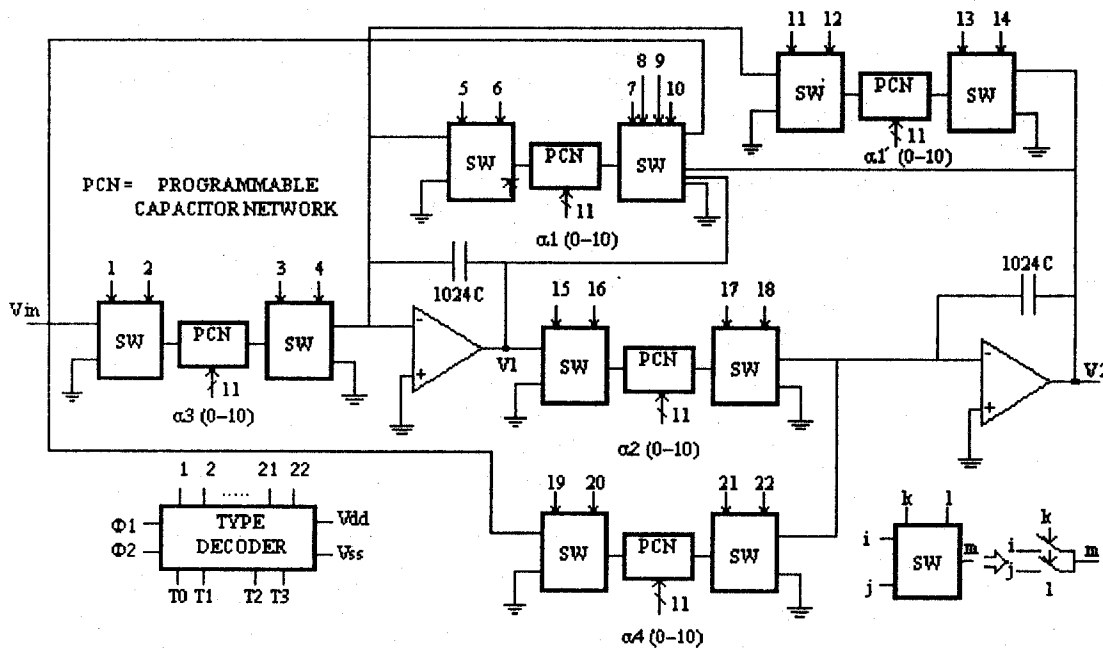

Fig. 2. Programmable biquad

The biquad is first programmed by a four bit word T0-T3 (D0-D3) into the appropriate configuration. Subsequently five eleven bit coefficients define the transfer function. The former section can be programmed into one of the sixteen possible types. Table 1, Ref. 1, pp. 584 shows the controls bits and the corresponding filter type, for instance:

D3	D2	D1	D0	Filter Type	Name
0	0	1	0	Band-pass Type 1	BP1
0	0	0	0	Notch Type 1	N1
0	1	1	1	Notch Type 2	N2

Table 1. Some programmable biquad types

Some of the sixteen z-domain transfer functions biquad types are given in table 2, Ref. 1, pp. 585, for instance expression (1).

Each of the five coefficients that define the filter transfer function is made up of eleven bits. These bits are loaded into each section through the serial interface.

$$H(z) = \frac{-\alpha 4.\left[1 + \left((\alpha 2.\alpha 3/\alpha 4) - 2\right)z^{-1} + z^{-2}\right]}{1 + (\alpha'1.\alpha 2 + \alpha 1.\alpha 2 - 2)z^{-1} + (1 - \alpha 1.\alpha 2)z^{-2}}$$

(1)

$H(z) = V_1 / V_{in}$ where V_1, V_{in} are shown in figure 2.

2.3 Coefficient Storage Unit

The biquad section needs 59 bits for programming, out of which, 55 bits are for the five filter coefficients and four bits are for the filter type. The programming bits are loaded into the chip through the serial interface and stored in temporary registers. After the filter design

is completed and the response meets the specifications, the programming bits can be transferred into non-volatile E^2 memory for permanent storage. The storage unit for one biquad section is shown in figure 3. The details of one bit storage is shown in figure 4. The source of the control bits for the biquad sections can be switched between the temporary registers and E^2 memory by a signal labeled SEL. The E^2PROM can be programmed when the Programmable Enable (PE) is made high. The PE signal is controlled through the SEL/PEN pin, which accepts a tri-level input signal.
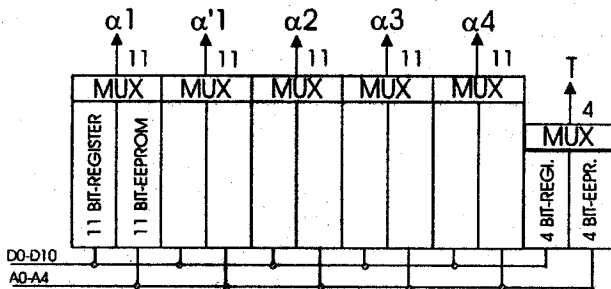

Fig. 3. Storage unit for programming bits in a single biquad section

In the normal mode, SEL/PEN changes between DGND and V_{DD}, which controls the selection between the temporary registers and the E^2PROM. By setting SEL/PEN=0V on select the temporary registers and the SEL/PEN=V_{DD} (5 V) selects the E^2PROM as the source of the filter control bits. The pin has an internal pull up, so that if it is left floating, the E^2PROM will be selected. When SEL/PEN pin is connected to V_{SS} (-5V) the E^2 program enable signal PE will be activated. The actual programming takes place when V_{PP} (the E^2 programming voltage) is ramped from V_{SS} (-5V) to a high voltage in the range of 12.5-13.5 V. When this happens the contents of the temporary registers are transferred to the E^2PROM. After the programming is completed V_{PP} should be returned to V_{SS} (-5 V). The E^2 programming timing waveforms are shown in Ref. 1 (figure 4, page 586).

2.4 Serial Interface

The filter programming data is stored in the internal temporary register through a four pin serial interface. When WR goes low, sixteen bits of data are shifted serially into the chip through the I/O pin. The sixteen bits constitute eleven bits of programming data and five bits of destination address. The data is sampled on the rising edge of the shift clock (clk). When WR goes high, the contents of the memory location selected by the five bit destination address is updated by the eleven bit data. For proper operation of the interface there has to be exactly sixteen shift clock pulses within the WR high-to-low and low-to-high transition period. After data is latched into the selected register, the internal timing automatically loads the contents of the same location back into the serial interface shift register so that it can be read back. However, the data that is loaded back can be selected between the temporary register or the E^2 memory by controlling the SEL/PEN pin. This feature is useful for diagnostic purposes. Every reading of a selected location should be proceeded by a writing into the same location. To read the data out the RD signal should be pulled low. After sixteen clock pulses all the data inside the shift register will be clocked out of the I/O pin. The data appears at the output, on the rising edge of the shift clock (clk). To avoid any conflicts, the falling edge of the RD signal should be at least eight crystal clock periods away from the rising edge of WR. The same rule applies to consecutive write cycles. The serial interface diagram is shown in figure 5.
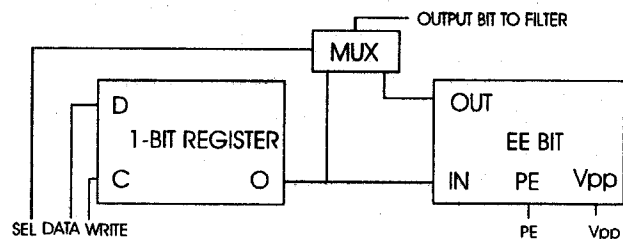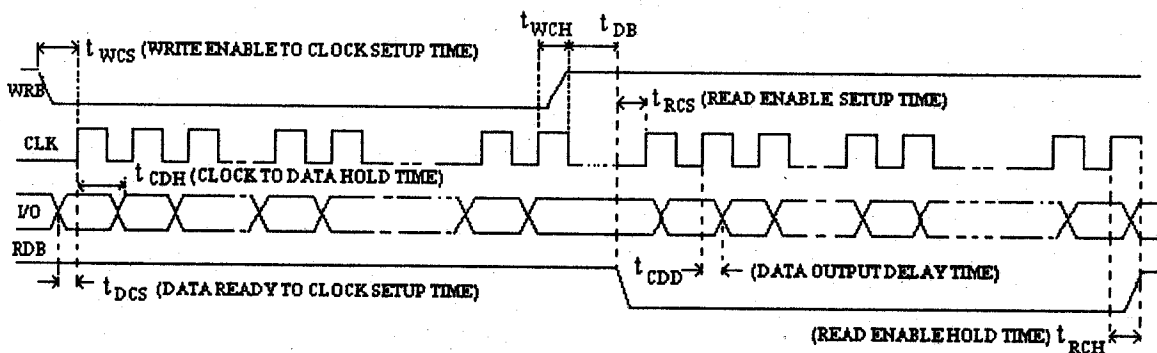

Fig. 4. Bit storage unit

Fig. 5. Serial interface timing diagram

A2	A1	A0	DATA
0	0	1	$\alpha1$ (Filter coefficient, D0-D10)
0	1	0	$\alpha'1$ (Filter coefficient, D0-D10)
0	1	1	$\alpha2$ (Filter coefficient, D0-D10)
1	0	0	$\alpha3$ (Filter coefficient, D0-D10)
1	0	1	$\alpha4$ (Filter coefficient, D0-D10)
1	1	0	T (Filter type, D0-D3)

Table 2. Filter coefficient and type address location

The five address bits A0-A4 are divided into two groups, A3, A4 and A0, A1, A2. The first group selects the biquad section and the second group address the filter coefficients and type of the selected biquad section. A map of the memory locations is shown in tables 2 and 3. As shown in figure 6, the address A4=A3=A2=A1=A0=0 selects the programmable counter and a two bit register that contains the number of the biquad sections according to table 4. Out of the 32 possible address locations, 25 are utilized and 7 locations are unused.

A4	A3	SECTION
0	0	1
0	1	2
1	0	3
1	1	4

Table 3. Biquad section address location

SHIFTED IN LAST   SHIFTED IN FIRST

| A0 | A1 | A2 | A3 | A4 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 |

→ DATA
→ ADDRESS OF BIQUAD SECT.
→ ADDRESS OF FILTER COEFF.
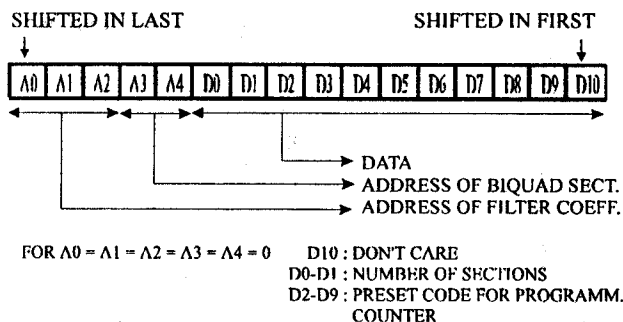
FOR A0 = A1 = A2 = A3 = A4 = 0   D10 : DON'T CARE
                                  D0-D1 : NUMBER OF SECTIONS
                                  D2-D9 : PRESET CODE FOR PROGRAMM.
                                          COUNTER
Fig. 6. Address/Data allocations for the input bits

NUMBER OF SECTIONS	D1	D0
1	0	0
2	0	1
3	1	0
4	1	1

Table 4. Number of biquad sections

2.5 Programmable Counter

The filter clock is derived from an on-chip oscillator and a programmable counter. The counter is shown in figure 7. The presetable counter is at the

address location A4=A3=A2=A1=A0=0 and it is programmed by the eight bit word D2-D9 from the serial interface shift register.
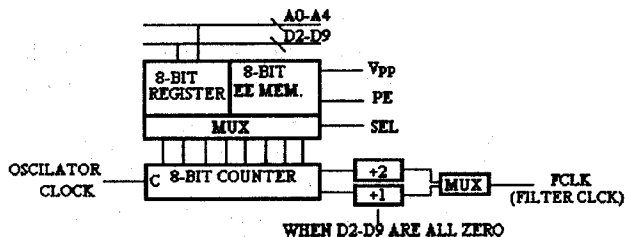

Fig. 7. Programmable counter

The output of the programmable counter is divided by two before it is applied to the filter.

D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D/R
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	1	506
0	0	0	0	0	0	1	0	508

Table 5. Two examples of programmable counter divide ratios (D/R) versus control codes

In Table 5 are shown examples of divide ratios. It is always an even number (except when $D_2 - D_9$ are all 0). It ranges from 2 to 510 in increments of two. When $D_2 - D_9$ are all 0 the divide ratio is 1.

For further details see Reference 1: CMOS Integrated Circuit Data Book - Sierra Semiconductor SC22324.

3. A Programming Example

The example consists of a band pass filter of type I (BPI) with $\alpha_1 = 33$, $\alpha_1' = 3$, $\alpha_2 = 7$, $\alpha_3 = 1365$ and α_4 which doesn't occur in the filter equation (2).

$$H(z) = \frac{-\alpha_2\alpha_3 z^{-1}\left(1 - z^{-1}\right)}{1 + \left(\alpha_1'\alpha_2 + \alpha_1\alpha_2 - 2\right)z^{-1} + \left(1 - \alpha_1\alpha_2\right)z^{-2}} \quad (2)$$

The biquad is first programmed by a four bit word (T0-T3) into the appropriate configuration (type - BPI) , table 1.

Then five eleven bit coefficients define the transfer function (2....6), tables 2, 3. The coefficients are illustrated in table 6, where row 7 D2 - D9 correspond to the divide ratio, table 5.

	A0	A1	A2	A3	A4	T0 D0	T1 D1	T2 D2	T3 D3	D4	D5	D6	D7	D8	D9	D10
1	0	1	1	0	0	0	1	0	0	X	X	X	X	X	X	X
2	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
3	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0
4	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0
5	0	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1
6	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X
7	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	X

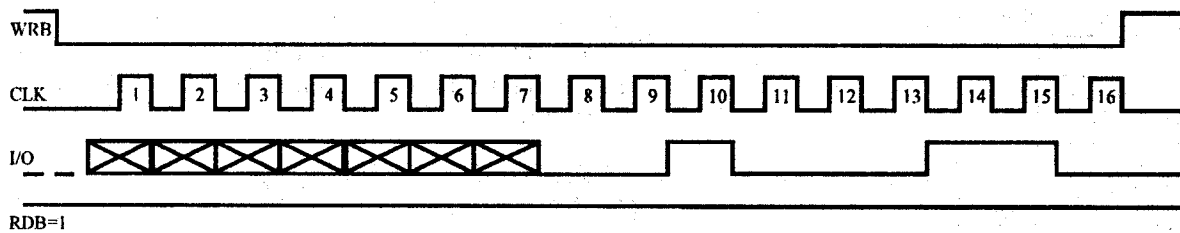Table 6. Coefficients of an example

Fig. 8. Serial interface timing diagram

4. Interface

Provided that the technology of the SC22324 is CMOS and the technology of the computer output port is TTL, it will be necessary a special interface from TTL to CMOS. An easy way to solve this problem is to use a pull-up resistor of 3K3. Because of safety reasons, optocouplers are used.

A typical optocoupler interface circuit is shown in figure 9. The worst-case design process should include consideration of data rates, power supply variations, component tolerances and temperature ranges as well as the characteristics of the digital logic families.

A suitable optocoupler for the interface circuit is the 4N25. The 4N25 has some interesting specifications like high direct current transfer ratio and high-speed switching times.
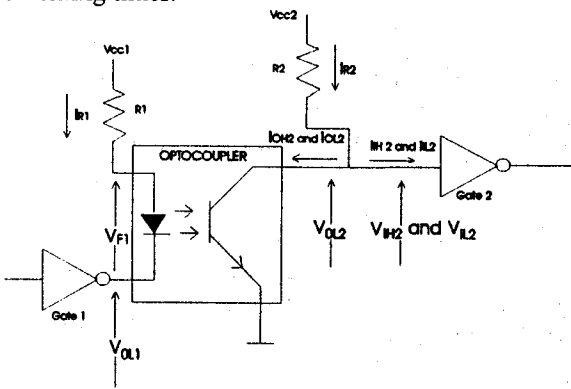

Fig. 9. Optocoupler interface circuit

The CMOS specifications with 5 V supply = V_{CC2} are :

$$V_{IH(min)} = 0.7 \, V_{CC} = 3.5 \, V$$

$$V_{IL(max)} = 0.2 \, V_{CC} = 1V$$

The TTL specifications are :

$V_{IL(max)} = 0.8 \, V$	$I_{OH(max)} = 400 \, \mu A$
$V_{IH(min)} = 2 \, V$	$V_{OL(typ)} = 0.2 \, V$
$I_{IL(max)} = -1.6 \, mA$	$V_{OL(max)} = 0.4 \, V$
$I_{IH(max)} = 40 \, \mu A$	$I_{OL(max)} = 16 \, mA$
	$V_{OH(min)} = 2.4 \, V$

Programming the SC22324 will be done through the parallel output gate of the personal computer. Since there are 8 outputs and only three are needed to program the chip, the other five are taken as the supply voltage V_{CC1}. This is done to minimize the voltage drop of "V_{CC1}". Remind also that the output port of the personal computer is a special buffered output. It can sink and source more current with less deviation towards the worst case specifications.

Tests with the output port of the computer pointed out that for a current of 10 mA, no significant voltage drop was measured. Therefore $V_{CC1(min)}$, which is the same as $V_{OH(min)}$ for TTL, was taken as 4 V. For V_{CC2} was a deviation of 5 % brought into account and the CMOS gate was considered to be ideal. This means that both I_{IH2} and I_{IL2} are zero.If the values of here above are used to compute the values of R_1 (max) and R_1 (min) for I_F = 10 mA then we get resp. 346 Ω and 313 Ω. R_2 (min) is

then 3950 Ω and $R_{2(max)} = \infty$. For R_1 330 Ω was taken and for R_2 4K7.

5. The Program

The program which we developed for the SC22324 IC is written in Turbo Pascal 5.0. The block diagram is illustrated in figure 10.
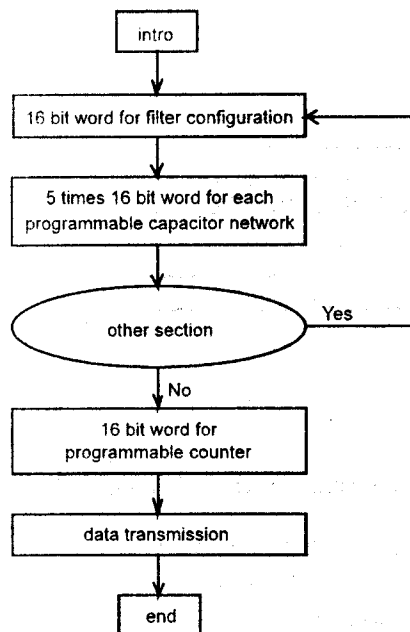

Fig. 10. Block diagram of the program

Each biquad is first programmed into the appropriate configuration with a sixteen bit word. After this, the biquad needs five more sixteen bit words for each programmable capacitor network. Depending on how many biquads are going to be used this process is repeated.

Afterwards data is needed for the programmable counter. Once this is done the data transmission can start.

The data transmission takes place through the parallel port of the computer. For proper operation of the interface, there has to be firstly, exactly sixteen shift clock pulses within the WR high-low-high transition period. Secondly there has to be at least eight crystal clock periods between each sixteen bit word and finally the serial input timing conditions, Ref. 1 page 589., should be taken into account. Therefore delays are provided in the program.

6. A Filter Design Example

Here we propose, as an example, the design of a low-pass Cauer filter with the following specifications:

Passband limit:	3400 Hz
Passband ripple:	0.1 dB
Stopband limit:	4600 Hz
Stopband attenuation:	32 dB

We also use the 3.579545 MHz common American TV color burst crystal. The filter clock sampling frequency will be chosen as 128000 Hz (divide ratio=28).

First of all, we will run the BIQUAD.EXE file supplied by Sierra Semiconductor. The program's final goal is the filter parameters storage in a on-chip E^2PROM. But now we are only interested in the first step of it in order to obtain the biquad sections coefficients. We first get the filter's order n=6 and then the section's transfer function coefficients (Table 2 Ref. 1, page 585):

Type	a1	a'1	a2	a3	a4
N2	190	190	67	26	67
N2	94	118	214	291	214
N1	155	199	158	197	569

The BIQUAD.EXE file also leads to the filter response.

Here in Fig. 11 we will represent the magnitude vs. frequency. There are three transmission zeros but in the present graph we may see only two.
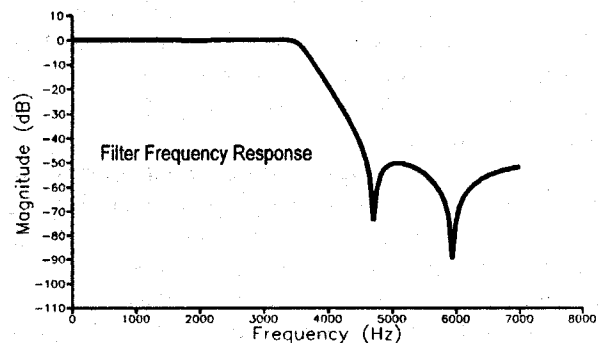

Fig- 11. Filter magnitude vs. frequency response

The next step in this design consists of the SC22324 RAM programming through the parallel output gate of the personal computer. Remember that this work has been developed having in mind a didactic purpose.

The program sc22324.pas, we wrote in Turbo Pascal 5.0 for this purpose, will now be applied and the data transfer through the parallel port of the computer to the printed board (figure 11) will take place.

The sixth order elliptic filter is now ready to work. To change parameters, we may quickly re-program the chip.

7. The Board Layout

The printed board, which is shown in figure 12, includes also a +5 / -5 V power supply, an input limiter in order to protect the chip and the optocouplers interface.
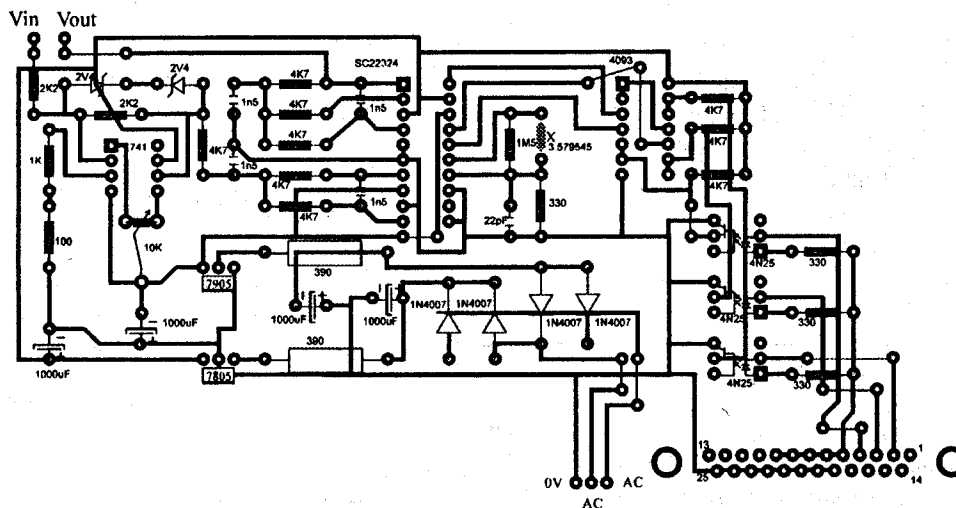

Fig. 12. The print with components

The components and their value are also visible.

Remark that pins 2-9 are used to program the chip via the parallel output port of the personal computer with the address 378H.

8. Conclusion

The main goal, programming the RAM of the SC22324, so that it can be used for didactic purposes, was achieved by using a personal computer, an interface and an adjusted print.

To program the chip, an executable file was developed which should be runned on a personal computer. The parallel output port with the address 378H is the link to the interface.

A special interface was needed since the technology of the personal computer is TTL and the one of the chip is CMOS. The interface consisted of optocouplers.

Finally the adjusted print was developed and tested.

References

[1] CMOS Integrated Circuit Data Book. Sierra. 1991.

[2] Ananda Mohan, P. V. Ramachandran, V. Swamy, M. N. S. Switched Capacitor Filters, Theory Analysis and Design. Prentice Hall (UK), 1995.

[3] F. Bailleu, Y. Blanchard, P. Loumeau, H. Petit, J. Porte. Capacités Commutées et applications. Dunod (Paris), 1996.

[4] S. Pagel Lindow. Sintesis de Filtros Eléctricos y Electrónicos. Norgráfica. Vigo. Spain, 1995.

About authors...

Sigfredo PAGEL LINDOW was born in Buenos Aires, received Dipl. Ing. degree in telecommunications engineering (1972) from the Engineering Faculty of La Plata (Argentina). He worked as researcher for more than ten years (1977-89) at CNIE (Space Commission of Argentina) in several communications and Landsat satellite projects. He is currently a Professor in Circuit Theory at the Telecommunication School of the University of Vigo (Spain).

Fernando PÉREZ FONTÁN was born in Vilagarcia de Arousa (Spain), received Dipl. Ing. degree in telecommunications engineering from the Engineering School of Madrid (Spain) where he also received the Ph.D. degree in telecommunications engineering. He worked as Project Engineer at Marconi and Telefónica in Spain. He is representative from Spain at the Management Committee of the COST 255 Project. He is currently a Professor in Mobile Communications at the Telecommunication School of the University of Vigo (Spain).

Michel VAN LOOY was born in Belgium, received Ing. degree in telecommunications (Electronics) engineering from the Katholieke Industriele Hogeschool Der Kempen. He worked also as student scholarship in the ERASMUS program.