HIGH-LEVEL ANALOGUE FAULT SIMULATION USING LINEAR AND NON-LINEAR MODELS

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Abstract

A novel method for analogue high-level fault simulation (HLFS) using linear and non-linear high-level fault models is presented. Our approach uses automated fault model synthesis and automated model selection for fault simulation. A speed up[1] compared with transistor-level fault simulation can be achieved, whilst retaining both behavioural and fault coverage accuracy. The suggested method was verified in detail using short faults in a 10k state variable bandpass filter.

Keywords

analogue testing, analogue fault simulation, fault modelling, operational amplifiers, CAD

1. Introduction

Due to the trend of combining analogue and digital circuits on one chip, analogue testing has gained more and more interest in the recent years. Analogue testing strongly influences time-to-market and time-to-profit and is unfortunately still a major bottleneck in developing mixed-signal ICs.

Analogue fault simulators potentially provide the ability to assure and optimise functional test sets, and allow use of efficient structural test techniques. The first analogue fault simulators work exclusively at transistor-level [1, 2]. Generated faulty netlists are simulated sequentially with a standard analogue simulator, resulting in a very CPU intensive process which is not viable for modern analogue and mixed-signal ICs. To overcome this problem fault macromodels were developed e.g. [3, 4]. However, although the achieved speed up, the published models are not accurate for all faults. We show how accurate high-level analogue fault simulation using both linear and non-linear high-level models together is possible. The proposed approach provides both the required accuracy and speed up and we describe an algorithm for selecting the most appropriate model.

[1] speed up = high level simulation time/transistor-level simulation time

2. High-level fault modelling

Previous work on linear fault macromodels for op amps are presented in [3, 4]. These are basic fault models and can not cover every kind of faulty behaviour, in particular their output impedance is modelled with a linear resistor, so they cannot model certain loading effects due to faults. In [5] a linear fault model for inverting and non-inverting amplifiers are presented. A non-linear model can be built just by replacing the linear controlled sources with non-linear ones. Again certain types of faults can not be modelled in this way, because the output impedance is a linear function. Non-linear high-level fault models and statistical fault simulation are described in [6], however, unlike our work only one type of model is used.

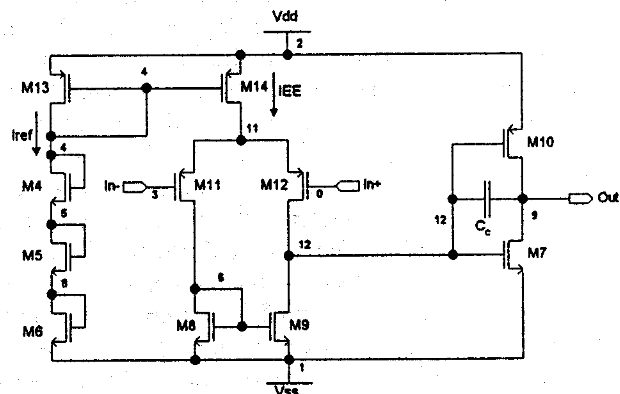

Fig. 1: Two stage CMOS operational amplifier

Fig. 1 shows the schematic of the two-stage CMOS op amp used as an example in this paper. 19 possible short faults are simulated at transistor-level. Since, M4, M5 and M6 are designed identically (a drain to source short on these transistors are equivalent), only 17 faults are simulated at high-level. 9 out of 17 short faults cause stuck-at behaviour at the output node, therefore 53% of the investigated faults result in stuck-at faults. 6 faults shift the input offset voltage, 7 faults have a non-linear impedance which can be well modelled with a non-linear controlled capacitor and 3 faults cause an out-of specification fault. For only 6 faults the output impedance is independent from the differential input voltage and can be modelled with a linear resistor. Some faults favour linear models, whereas other faults require non-linear models. A detailed discussion on how to develop linear and non-linear fault models is beyond the scope of this paper, however it can be found in [7].

3. High-level analogue fault simulation algorithm

First, the faults are categorised for the purpose of modelling. Four groups of faults are defined: For group 'A' sufficient simplifications can be made to use a linear model, or where the dc and ac parameters show a linear behaviour over a wide range of operation. For group 'B' dc parameters are non-linear, however the ac parameters (poles and zeros) can be linearized. For such faults a non-linear model is inserted which implements the non-linear dc behaviour, but with fixed poles and zeros (linear ac behaviour). Situations can occur, where both dc and ac parameters behave non-linearly. These types of faults form group 'C'. Here more complex non-linear models have to be used, where both parameter sets are modelled non-linearly. Group 'D' contains faults where the model topology (structure) is not able to model the faulty behaviour. This worst case scenario did not occur in the example circuit. Within each group, faults with similar behaviour are collapsed. The parameterization of the linear models is performed in the linear region and in both saturation regions of the fault free op amp.

For the example only 8 stuck-at faults and 3 out-of-specification faults were simulated with linear fault models. For one stuck-at fault and for all of the other faults the filter is simulated with non-linear fault models.

At the simulated operating points, given by transistor-level operating point analysis of the whole circuit, the parameterization of the linear high level fault models is performed.

After such pre-processing steps the actual high-level fault simulation is performed according to Fig. 2. First a decision is made on whether to use a linear or a non-linear fault model according to the fault categories. In both cases a transistor-level operating point analysis is performed on the whole circuit. For a linear fault model the operating point information is used to make sure that the linear model is in the region for which the model was parameterized. If this holds true the parameterized model is used, otherwise a check is made to see if the faulty behaviour can still be simulated with a linear model. If so, new parameters are derived, however, if this check fails a non-linear fault model have to be used. The operating point analysis further can be used for convergence aid for the non-linear models. After these checks the faulty high-level model is injected.

Fault free op amps in the remaining circuit are checked to determine if they are either in one of the saturation regions or in the linear region. If this is the case, a linear model is inserted, otherwise, a non-linear one is inserted (Fig. 2).

After the injection of high-level fault models the actual fault simulation is performed. During fault simulation it has to be ensured that the operating region for which the linear model was designed is never violated. A warning mechanism can be implemented for this purpose with a simple if-else statement [5] in any analogue hardware description language. Instead of asserting a warning message, the linear model could be also exchanged with a non-linear model (Fig. 2). Then the simulation continues with a non-linear model, when the region for which the linear model was designed for is violated.

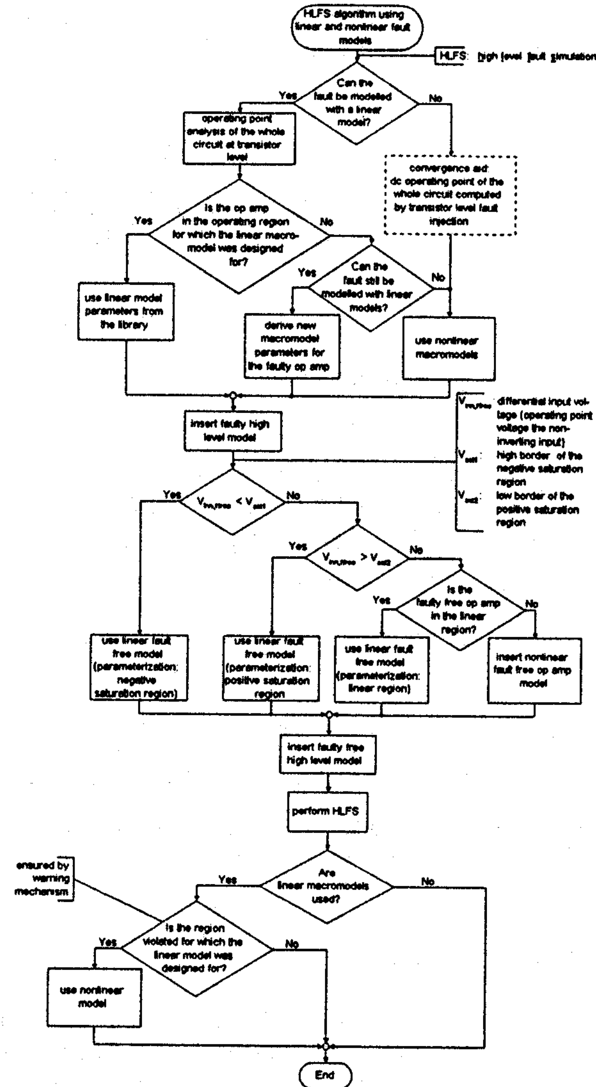

Fig. 2: High level fault simulation algorithm using linear and non-linear models

4. Performance

Fig. 3 and Fig. 4 show the state variable bandpass filter and the achieved speed up, respectively. It can be seen that the highest speed up is achieved when only linear models are used for both the faulty and the fault free op amps. If only dc parameters are modelled the speed up is always higher than a model that uses dc and ac parameters. When non-linear models are used for the faulty and fault free op amps, it is possible that the high-level simulation is not much faster than the transistor-level simulation due to convergence difficulties (we commend on this later). The output impedance of the

fault free op amps was modelled with a non-linear controlled resistor (zout=f(input voltage)). When a convergence aid is provided with a transistor-level operating point analysis in conjunction with the high-level fault method the speed up could be improved. Note in case c) and d) of Fig. 4 only dc parameters are modelled.

The HLFS achieved the desired accuracy and the high level fault coverage exactly matches the fault coverage obtained at transistor-level.

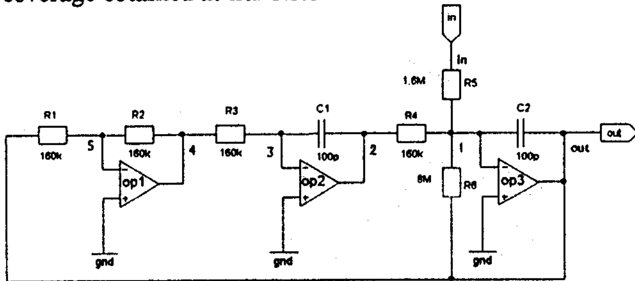

Fig. 3: 10k state variable bandpass filter

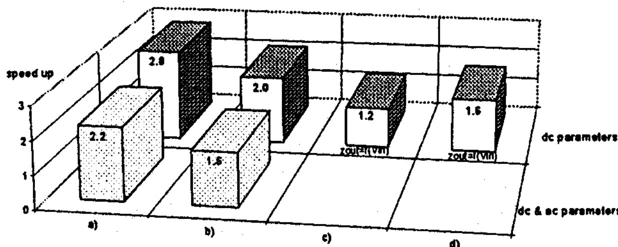

Fig. 4: Achieved speed up:
a) linear faulty and fault free op amp model,
b) non-linear faulty op amp model and linear fault free model,
c) non-linear faulty and fault free op amp model without convergence aid
d) non-linear faulty and fault free op amp model with convergence aid

5. Conclusions

The best speed up was achieved when only linear models were used, however, linear fault models can only be used for certain types of faults. The best simulation efficiency in the case of a 10k state variable bandpass filter is achieved with a combination of linear and non-linear fault models. We also applied our technique to a commercial, 68 transistor bipolar I-V amplifier and achieved a speed up 5 using non-linear model. The greater speed up was due to the relation of large number of transistors compared with the model complexity. A commercial analogue simulator was used to simulate the behavioural models, which supports analogue HDL. This simulator uses a Newton Raphson method for solving sets of non-linear equations. Certain non-linear functions can not be solved efficiently with such a method and this limited the speed up of the non-linear models. Therefore even better results are expected if the proposed non-linear models are used in conjunction with analogue fault simulators optimised for this process.

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Ernst Bartsch was born in Passau'74, Germany. He received his Dipl.-Ing (FH) degree from the Fachhochschule Regensburg (Germany) in 1997. Ernst is currently a MSc candidate in electronic engineering at the University of Hull (U.K.). His research concerns improvements in analogue fault simulation through high level modelling. Therefore analogue and mixed-signal designs were investigated.

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In January'99 Ernst started to work as a research assistant in the Engineering Department of the University of Cambridge (U.K.). His research interest involves mobile communication, single-chip CMOS radio design and wireless LAN

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