MODELLING OF MODERN ACTIVE DEVICES FOR SIMULATION OF ANALOG CIRCUITS IN PSPICE

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Abstract

Suitable models of the modern active components and functional blocks, namely new types of current conveyors, operational and transimpedance amplifiers, in several appropriate levels, using analog behavioral modelling are given in this paper.

Keywords

Analogue circuit, operational amplifier, transimedance amplifier, current conveyor, modelling, simulation, CAD.

1. Introduction

Modelling and CAD simulation is effective way to test and design any circuit. Specially in discussed high frequency region and in current mode, where new active components and functional blocks are used, which macro models are not known for now, in contrast to the standard operational amplifier, where all major producers are providing PSpice-based macromodels [1], [2].

The recent progress of the analogue technology has bred several modern active devices, i. e. the monolithic IC active components and functional blocks. They are versatile and powerful building blocks for many signal-processing applications, with higher frequency operation and wider dynamic range, comparing with the classical opamp. Such devices are e. g. the transimpedance opamps, the transadmittance opamps, the current-feedback opamps, the full current opamps, the voltage and current buffers and the current conveyors, especially CC II, CC II+/-, ICCII, DVCC, FDCC, UCC, etc.

All these devices can be simulated on transistor level, component by component, what is rather complicated. Here is better to use an analog behavioral modelling (ABM), providing by PSpice [2]. In this case the real device is described in terms of its network functions as a mathematical relationship and/or a lookup table. Several levels of suitable models for all above devices are given in this paper.

Good model is a powerful tool. Then many design problems can be quickly identified by simulation. What assumes that the model level and accuracy is adequate and trade-off.

2. First level ideal models

In the first level a model of the ideal device is taken. This representation reflects main base specifications only (gain, buffering etc.). The model usually consists of controlled sources only (VCVS, CCCS, VCCS and CCVS). As a illustrative example an ABM model of the ideal multi-port universal current conveyor (UCC) [3] suitable for the PSpice is given in Fig.1. There the voltage buffering is simulated by the voltage controlled voltage sources (*E1*, *E2*), with gains *E=1* and the current conveying with the dual current controlled current sources (*F1, F2*), where parameter *F=1*. The model of level 1 will be used in many cases of the simulation as a first step of the controlling analysis of the designed circuit to study main properties and functions only.

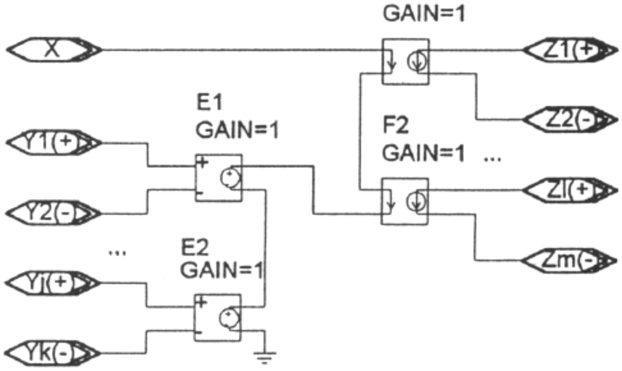


Fig. 1 First level ABM model of the universal multi-port current conveyor

3. Second level resistive models

In the second level an important attribute of the real device is taken into account, namely the driving input/output resistances, tracking and buffering errors. The model can be completed with DC sources, simulating offset and drift, using adequate multi-run temperature analysis.

As an example resistive ABM model of a novel functional block titled differential voltage current conveyor with balanced output (DVCC) [4] is given in Fig. 2.

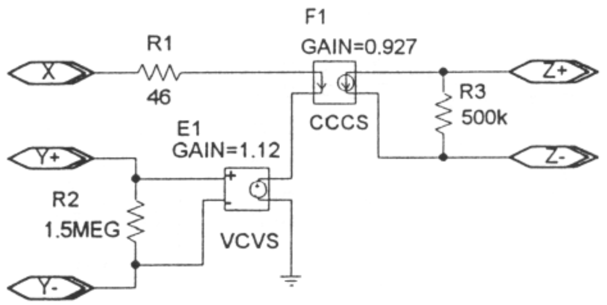


Fig. 2 Second level resistive model of the real conveyor DVCC

There the model of level 1 is completed with corresponding resistors R_X, R_Y and R_Z (Fig. 2). Note that the value of the R_X plays most important role in practical applications.

Research has indicated that the errors among the main nonidealities of the real DVCC are the concrete values of the voltage and current gains (E/F) or the buffering errors *(ΔE, ΔF)*

$$E = 1 \pm \Delta E, F = 1 \pm \Delta F. \tag{1}$$

In high precision signal processing applications, the effect of these errors must be reduced as possible. This problem can be solved taken in the model of Fig. 2 the gains *(E, F)* not equal one, but some real values given by (1). Note usually is

$\Delta E > \Delta F$.

Assessment and evaluating of absolute and or relative errors must be given there. For this purpose we can ingeniously employ utilities of the PSpice simulator, namely multiple simulation and parameter sweep (using STEP statement) or Monte Carlo simulation and or Worst-case tolerance analysis, randomly selecting parameters values.

This model can be completed with DC sources simulating voltage/current offset and drift using adequate multi-run temperature analysis, which is possible in PSpice, where the temperature is stepped through a list of values.

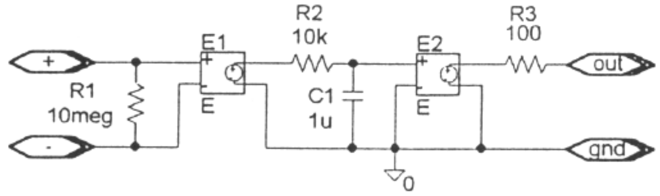


Fig.3 Simple model approximating the frequency dependent voltage gain of the standard opamp

4. Frequency dependent model of level three

Studying very much important frequency responses of the given circuits (AC Analysis), suitable frequency dependent models of employed devices may be used. These models of level 3 approximate the driving impedances and especially the frequency dependent transfer functions.

A simple example of such model is given in Fig. 3 for the well-known classical operational amplifier. There port resistances are modelling by R_1 and R_3, the voltage gain by the VCVS $E_1=A_0$ ($E_2=1$) and standard frequency response (with one dominant pole) is simulating by a RC-low pass cell (R_2, C_1) between the VCVS's.

Note that in PSpice the frequency dependent transfer functions *E(ω)* or *F(ω)* can be better modelled by adequate ABM blocks titled ELAPLACE or GLAPLACE, what are the Laplace defined (using variable s) frequency dependent sources FD-VCVS and FD-VCCS respectively. Such an example is given in Fig. 4 for a model of the above DVCC (resistive model in Fig. 2).

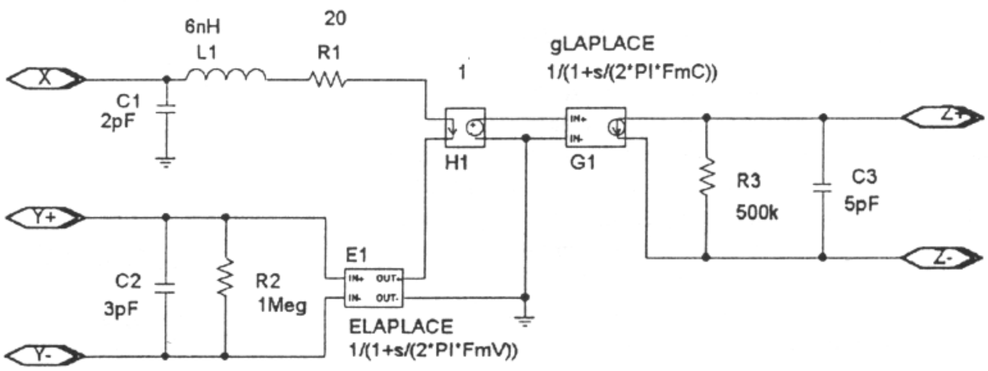


Fig. 4 Frequency dependent model (level 3) of the conveyor DVCC using Laplace ABM blocks

There the frequency dependent voltage buffering *E(ω)* is simulated by the following mathematical relationship

$$E(s) = \frac{1}{1 + s\tau_v}, \qquad \tau_v = \frac{1}{2\pi f_{mv}}. \tag{2}$$

The block is describing the approximation of the real voltage buffering between ports Y and X, with one dominant pole and the cut-off (–3 dB) frequency f_{mV}, which can be adjusted during the simulation.

The real frequency dependent current conveying between ports X and Z must be modelling by a suitable cascade combination of two blocks, due to that a Laplace CCCS is not in the PSpice. Namely there are the standard CCVS (with gain $H=1$) and the GLAPLACE block (what is a VCCS) with the Laplace transfer function given by similar eq's as the (2), where the cut-off current frequency f_{mC} is defined.

This model can be completed with the port impedances (Z_X, Z_Y, Z_Z), namely adding frequency dependent elements C and L (Fig. 4).

The above models with the Laplace sources (Fig. 4) are more suitable for the AC analysis [2], on the other hand, in the Transient analysis [2] it is better to use the principle given in Fig. 3. Using this way a modification of the frequency dependent model of the real DVCC (Fig. 4) is given in Fig. 5.

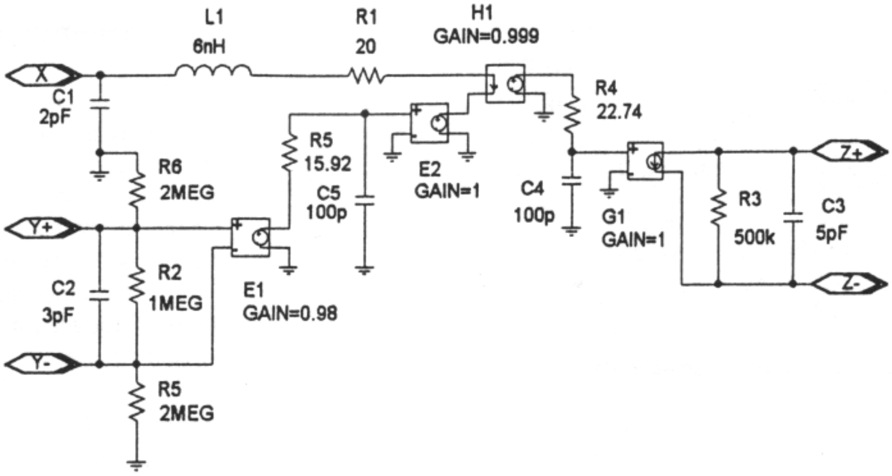


Fig. 5 Modification of the level 3 model (Fig. 4) of the real DVCC

The other level 3 model namely of the real transimpedance amplifier was proposed in Fig. 6. There the transfer function has three poles, namely at:

fp1 = 12 kHz, fp2 = 70 MHz, fp3 = 300 MHz.

5. Nonlinear model of level four

The real active elements must be some time considered as a nonlinear blocks specially for transient analysis with larger amplitude of the signals. Therefore the linear small-signal model of level 3 can be added by a limiting nonlinear subcircuit, usually consists of some diodes and transistors. One simple example for standard operational amplifier is given in Fig. 7.

Note a block diagram of the nonlinear model for the HF buffer amplifier (e.g. EL 2001C). There a nonlinear output stage is linked to a linear part, which consists of two VCVS and RC low-pass filter.

6. Professional models of level five

Some manufacturers of the active devices give also the detailed models of level 5, usually titled macromodels [2]. There the major subcircuits are simulated in detail on the transistor level (e.g. the difference amplifier stage in the opamp. [2]). Unfortunately these macromodels are rather complicated. There are more nodes and components for some kids, especially in an evaluation version of the PSpice. Furthermore for the new devices they are not known in this time.

7. Valuation of the models

Comparison of the models given above is illustrated on simple example namely on the noninverting amplifier with the transimpedance opamp AD 844. The results of the AC and Transient analysis are shown in Fig. 8a and Fig. 8b respectively. Note good compliance between our model of the level 3 (Fig. 6) and the level 5 professional macro model [5] in the AC analysis (Fig. 8a), where these curves are surely identical in this case

In the Transient analysis (Fig. 8b) the compliance is not so good, but the model of the level 3 can be applicable in many cases, too.

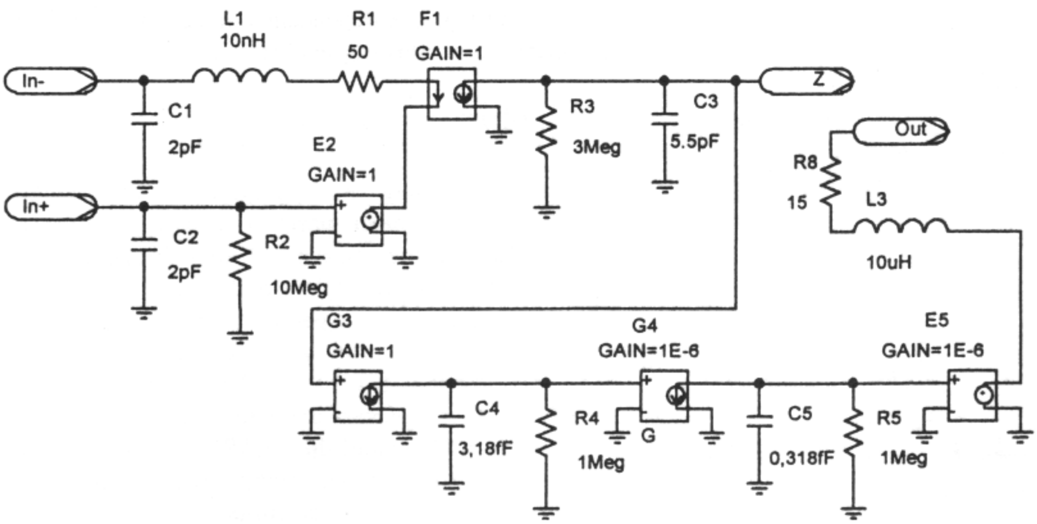


Fig. 6 Level 3 model of the transimpedance amplifier

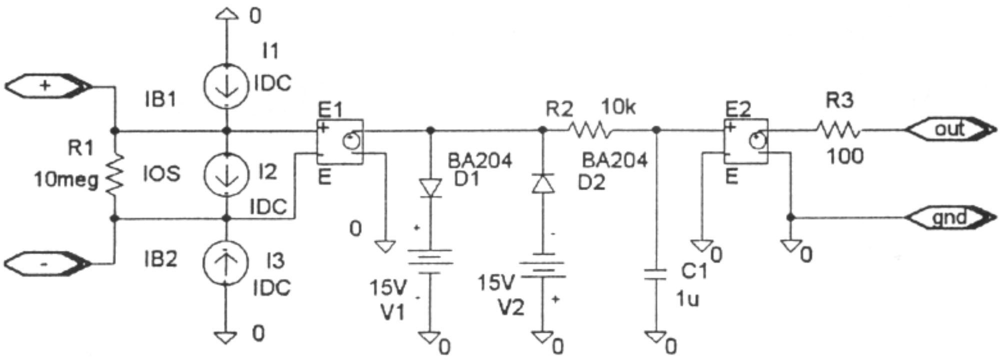
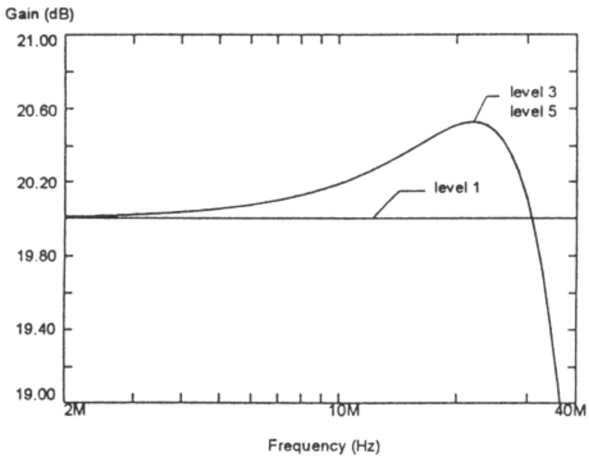


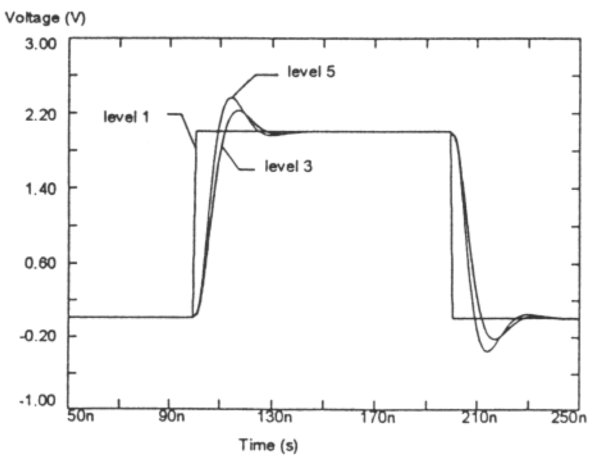
Fig. 7 Nonlinear (level 4) model of the standard opamp.

8. Conclusion

The models given above are suitable for analysis of modern ARC filters and other circuits of analogue signal processing. The aim is accurate modelling with reduced complexity.



a)



b)

Fig. 8 Simulation of the noninverting amplifier with the transimpedance opamp using modelling in several levels a) magnitude responses (obtained in AC analysis), b) pulse responses (obtained in Transient analysis)

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About author...

Tomáš DOSTÁL was born in Brno, in 1943. He received degrees CSc. (Ph.D) and DrSc. in electrical engineering from the Brno University of Technology in 1976 and 1989 respectively. From 1973 to 1978, and from 1980 to 1984, was with Military Academy Brno, from 1978 to 1980 with Military Technical College Baghdad. Since 1984 he has been with the Brno University of Technology, where he is now Professor of Radio-Electronics. His present interests are in the circuit theory, filters, switched capacitor networks and circuits in current mode.