# DIGITAL REALIZATION OF THE TEST SIGNAL GENERATOR SIN$^2$ 20$T$

Václav ŘÍČNÝ
Dept. of Radio Electronics
Brno University of Technology
Purkyňova 118, 612 00 Brno
Czech Republic

## Abstract

*The paper deals with the digital implementation of the generator of test signal sin$^2$ 20T. This function has a limited spectrum in the luminance and chrominance areas of the color composite signal. The signal is frequently used for measurements of the transmission channels in color television technology. The paper arises from the contribution [1].*

## Keywords

Test generator, measuring TV transmission channel

## 1. Introduction

Time response and corresponding spectrum (magnitude) of function sin$^2$ 20$T$ (applicable for TV standards CCIR D,B) are shown on Fig.1. This known test signal consists from the superposition of 2 additive components:

a) chrominance harmonic carrier signal (Fig.1a) of frequency $f_c$ = 4.43361875 MHz (for the TV standard PAL), which is amplitude modulated by modulating function 0.5 sin$^2$ $\omega_0 t$ = 0.5 sin$^2$ ($2\pi f_0 t$); $f_0 = f_h$ /20 = 6.10$^6$ Hz /20, i.e. 300 kHz ($f_h$ is threshold frequency of TV channel),

b) low-frequency luminance signal component in the form 0.5 sin$^2$ $\omega_0 t$ (Fig.1a).

The test signal is usually used for the properties of the transmission channels measurements in colour TV technique. Course of attenuation characteristic and cross time delays of the luminance and chrominance components can be evaluate from time response of this test signal on the measured channel output. Methods of these evaluations are described in [3 ], e.g.

## 2. Digital generation of the test signal sin$^2$ 20$T$

Principle of digital generation of measuring the signal sin$^2$ 20$T$ is apparent from the block diagram in the Fig. 2. Generation of the pulses sin$^2$ 20$T$ has to run periodically with a view to necessity of this signal display by the standard oscillograph.

The generator consists of the these functional blocks:

- frequency stable harmonic generator GCCS of the carrier chrominance signal,
- frequency stable generator GCP of clock pulses for the function control of the counter C and decoder DEC,
- counter C,
- decoder DEC of the digital representation of the signal samples 0.5 sin$^2$ $\omega_0 t$,

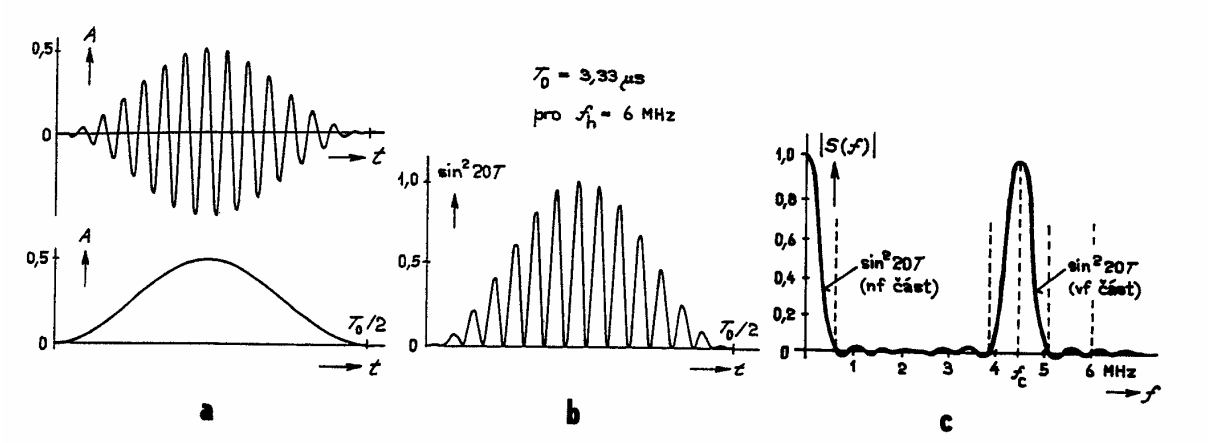


**Fig. 1** Time response of the components (a), composite signal (b) and corresponding spectrum magnitude | $S$(f)| (c) of the signal sin$^2$ 20$T$

- digital-analogue converter DAC,
- analogue low-pass filter ALPF,
- amplitude modulator AM,
- summing amplifier SA,
- control circuit CC.

Detailed description of the particular functional blocks is out of the scope of the paper. Reaching desired accuracy of the generated signal 0.5 sin$^2$ $\omega_0 t$ (better than 1%), number of samples has to be higher than $n_s$ = 20 in the half time period $T_0/2$ = 1.66 μs of this pulse. Hence, desired sampling frequency $f_s = (T_0 /2\ n_s)^{-1} = 1.66 \cdot 10^{-3}/20 \cong$ 12.00 MHz. The average value $\Delta_{ar}$ (maximum value $\Delta_{mr}$) of the relative deviation related to the ideal time response of the modulation function sin$^2$ $2\pi f_0 t$ is $\Delta_{ar} \cong 0.5$ % ($\Delta_{mr} \cong 1$ %) in the case of 5-bit representation of every sample and with application of the 4$^{th}$ order Butterworth low-pass filter on the generator output.

## 3. Structure of partial functional blocks

**1.** *Frequency stable generators* GCCS (4.4336 MHz) and GCP (12 MHz)

These generators have been realized by means of the integrated circuit QO105BIC (monolitic oscillators which are controlled by built-in crystal).

**2.** *Counter* C and *decoder* DEC

Counter and decoder work with a special code (blocks are realized together by means of the programmable gate arrays GAL 16V8). The block controlling function of the following digital-analog converter DAC has been proposed as counter with synchronous reset. It works with the special code, whose truth table is stored in the programmable gate arrays GAL 16V8. Logic functions have been optimized by means of the design system EASY ABEL. Block C is timed by clock pulses from the clock generator GCP.

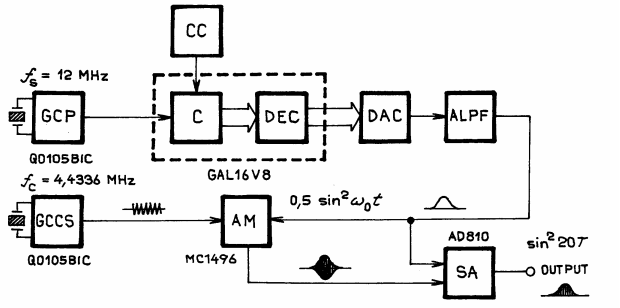


**Fig. 2** Block diagram of digital realization of the generator sin$^2$20$T$

**3.** *Digital - analog converter* DAC

In order to get simple and low-cost connection, the converter DAC is realized as simple resistive network and a summing connection of the broad-band operational amplifier AD 810. Conversion accuracy of converter depends on the stability of the supply voltage for the counter C and on the accuracy of all resistors in the resistive network. Principle of this converter is depicted in Fig. 3. Values of resistors in the resistive network are proposed with respect to the values of the output resistance of the integrated circuit GAL 16V8 and their fluctuations. All resistors ($R_1$, $R_2$, ..., $R_5$) are by means of three accurate resistors connected in series. Analog signal 0.5 sin$^2$ $\omega_0 t$ on the output of this converter is sampled in the form "sample and hold" by means of 20 samples with 10 symmetric values of output voltage. Tab. 1 shows input data code generated by block C – DEC.

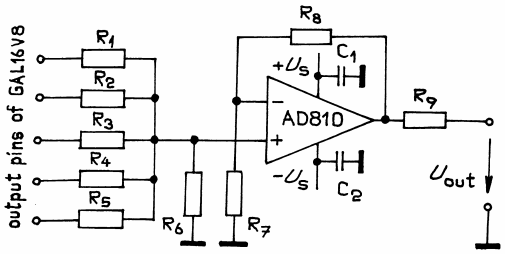


**Fig. 3** Principle of the converter DAC

**4**. *Output analog low-pass filter* ALPF

The filter is realized as 4$^{th}$ order Butterworth low-pass filter (cut-off frequency 500 kHz). It is proposed for the characteristic impedance $Z_0$ = 75 Ω.

| order of sample (after reset) | output level of pins DEC (input code for DAC) | signal level on DAC output |
|---|---|---|
| 1 | 0 0 0 0 0 | 0,00 |
| 2 | 0 0 0 0 1 | 0,09 |
| 3 | 0 0 0 0 1 | 0,09 |
| 4 | 0 0 0 1 1 | 0,36 |
| 5 | 0 0 0 1 1 | 0,36 |
| 6 | 0 0 1 1 1 | 0,67 |
| 7 | 0 0 1 1 1 | 0,67 |
| 8 | 0 1 1 1 1 | 0,91 |
| 9 | 0 1 1 1 1 | 0,91 |
| 10 | 1 1 1 1 1 | 1,00 |
| 11 | 1 1 1 1 1 | 1,00 |
| 12 | 0 1 1 1 1 | 0,91 |
| 13 | 0 1 1 1 1 | 0,91 |
| 14 | 0 0 1 1 1 | 0,67 |
| 15 | 0 0 1 1 1 | 0,67 |
| 16 | 0 0 0 1 1 | 0,36 |
| 17 | 0 0 0 1 1 | 0,36 |
| 18 | 0 0 0 0 1 | 0,09 |
| 19 | 0 0 0 0 1 | 0,09 |
| 20 | 0 0 0 0 0 | 0,00 |

**Tab. 1** Input code and appropriate output signal levels of D/A converter DAC

**5.** *Amplitude modulator* AM

This block is realized by means of the integrated circuit Philips MC 1496.

**6.** *Summing amplifier* SA

The block is realized by means of the integrated broadband operational amplifier AD 810 (Analog Devices) in the summing and non-inverting connection and serves as impedance connector with output impedance 75 Ω.

**7.** *Control circuit* CC

The circuit generates a periodic reset signal for counter C since the numeric generation of the signal $\sin^2 20T$ has to be generated periodically with a view to the requirement to display this signal by means of the standard oscillograph.

# 4. Conclusion

A proposed conception of the generator represents a relatively simple and modern resolution of the enough accurate generation of the signal $\sin^2 20T$. Function of the designed device has been verified by means of computer simulations. Subsequently, a complete design of the circumferential connection with modern integrated circuits for the technical realization of the functional specimen has been realized. The realized device can be used for laboratory education and for experimental activities.

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# References

[1] ŘÍČNÝ, V. Digital Realization of the $\sin^2 2T$ Generator. In: Proceeding of the 11th International Scientific Conference RADIOELEKTRONIKA 2001. Brno: FEI VUT, 2001

[2] JANEČKA, V. Generator of signals $\sin^2 T$ and $\sin^2 2T$. Diploma thesis. Brno: FEI VUT, 1999

[3] SVATOŠ, J. Electronics of TV devices. Praha: FEL ČVUT, 94.

# About author

**Václav Říčný** was born in 1937. He is professor and vice-dean at the Faculty of Electrical Engineering and Computer Sciences of the Technical University in Brno. His research interests include TV technology, video signal processing and applications of the light sensitive CCD sensors for measuring techniques.