The DVB Channel Coding Application Using the DSP Development Board MDS TM-13 IREF

Tomáš KRATOCHVÍL, Martin SLANINA

Dept. of Radio Electronics, Brno University of Technology, Purkyňova 118, 612 00 Brno, Czech Republic

kratot@feec.vutbr.cz

Abstract. *The paper deals with the implementation of the channel coding according to DVB standard on DSP development board MDS TM-13 IREF and PC. The board is based on Philips Nexperia media processor and integrates hardware video ADC and DAC. The program libraries features used for MPEG based video compression are outlined and then the algorithms of channel decoding (FEC protection against errors) are presented including the flowchart diagrams. The paper presents the partial hardware implementation of the simulation system that covers selected phenomena of DVB baseband processing and it is used for real time interactive demonstration of error protection influence on transmitted digital video in laboratory and education.*

Keywords

Digital video, digital television, channel coding, forward error correction, MPEG, Nexperia DSP.

1. Introduction

Channel coding of digital video data stream and utilization of error correction codes is defined in DVB standard. The system that can evaluate the efficiency of protection codes on digital video and its quality can be hardware implemented in a laboratory using multimedia DSP. This work deals with the previous simulation applied in Matlab and presented in [1].

2. DSP Nexperia Development Board

The MDS TM-13 IREF [2] is a PCI bus board for real time video, audio and telecommunications processing. It uses the 180 MHz Philips PNX-1300 DSP processor (called Nexperia) that is 32 bit fixed and floating point VLIW (Very-Long Instruction Word) processor with integrated video and audio interfaces. The development board provides video I/O in both CVBS and Y/C (S-video) formats, stereo audio I/O and telecommunications I/O through a modem interface and DAA (2-wire phone line).

The Nexperia processor is programmed in C or C++ using an optimizing compiler and scheduler (called NDK) that include operations for efficient real time video processing. The DSP also has a built image co-processor and variable length decoder (VLD) used in MPEG video compression. The architecture overview of the DSP is shown in Fig. 1 and the comprehensive features overview of all parts is available in [3].

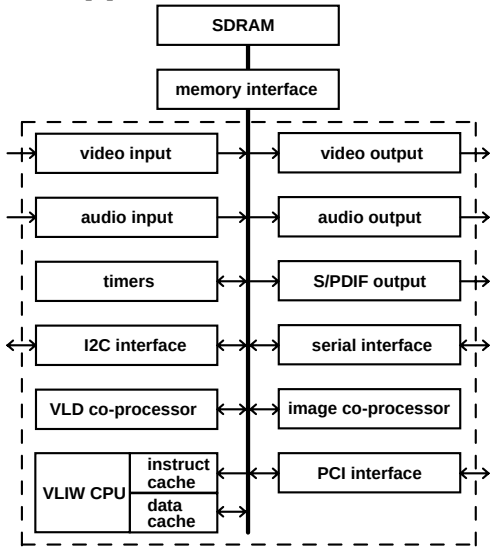

Fig. 1. The DSP Nexperia PNX-1300 architecture.

2.1 Digital Video Capture and Processing

The development board operates with the video input and reads a digital video data stream from an off-chip source into the main memory, it accepts CCIR656-compliant device with 8-bit parallel 4:2:2 YUV (8 x 27 Mbps). The video output provides a digital YUV data stream to off-chip video subsystems vice-versa to video input. Gathering bytes from the separate Y, U, V planes stored in SDRAM generates the output signal. The image coprocessor unit off-loads the CPU of cycle-consuming image processing tasks such as copying image from SDRAM to a host video frame buffer. The VLD unit operates as memory-to-memory coprocessor to decode Huffman-encoded MPEG-1 and MPEG-2 video data streams. Details are available in [4].

2.2 Used MPEG Based Encoder and Decoder

The Nexperia processor operates with the IADK application libraries. These are basic input and output video and audio codecs [5]. The libraries are available option

used with a development board and it also contains MPEG (Motion Picture Expert Group) encoders and decoders:

- *MPEG encoder and decoder Lib* (according to ISO/IEC 11172-2 and 13818-2) - provides a set of functions. It produces the MPEG-1 video streams from pictures separated from YUV (4:2:0) pixel data blocks (I and P – frames support, variable/constant bit rate, free definition of quantizer). MPEG decoder accepts the MPEG-1 and MPEG-2 MP@ML.
- *MPEG program and transport stream demux Lib* (according to ISO/IEC 11172-1 and 13818-1) - extracts the stream of MPEG audio and video, recognizes the IDs of streams and corresponding PES (Packetized Elementary Stream) start codes and parses PES packets, the demultiplexer receives a single MPEG-2 transport streams, scans the incoming PES, extracts the PIDs (Packet Identifiers) of video and audio, and starts decoding the stream.

Generally, the MPEG family standards are used as an effective tool for coding audio and video signals. The MPEG-1 and MPEG-2 may both reduce the temporal correlation so that a greater coding efficiency is achievable. Used libraries present standard solution of multimedia and digital video compression.

3. Digital Video Channel Coding

The principal of the channel coding in digital video transmission deals with the redundancy information that is added to the source-coded digital signal in the channel encoder. Two relevant methods of error protection in the transmission of digital video and digital television according to standard DVB are FECs (forward error corrections) by block Reed-Solomon code (FEC1) and convolution code (FEC2) with interleaving.

The RS (255, 239) was chosen which processes a data block of 239 symbols and can correct up to 8 symbol errors by calculating 16 redundant correction symbols. As an MPEG-2 packet is 188 bytes long, the code was shortened, i.e. the first 51 information bytes were set to zero and not transmitted at all. In this way the RS (204, 188) code is generated. After the outer code a convolution interleaver with depth $I = 12$ is used. From the frame length of the outer code with $n = 204$ the base delay results as $M = n/I = 17$. Finally a convolution code is applied to the interleaved symbols. Its rate $R = m/n$ - where m is the number of input bits and n of output bits - is equal to 1/2, the constraint length is $K = 7$ [6].

3.1 FEC1 Decoder Implementation

The RS code is symbol-oriented. The correction is not only in the error recognition and its replacement. The whole wrong symbol should be replaced. The symbol protection deals with the finite set of numbers (8bps with 256 elements) and its arithmetic uses Galois field.

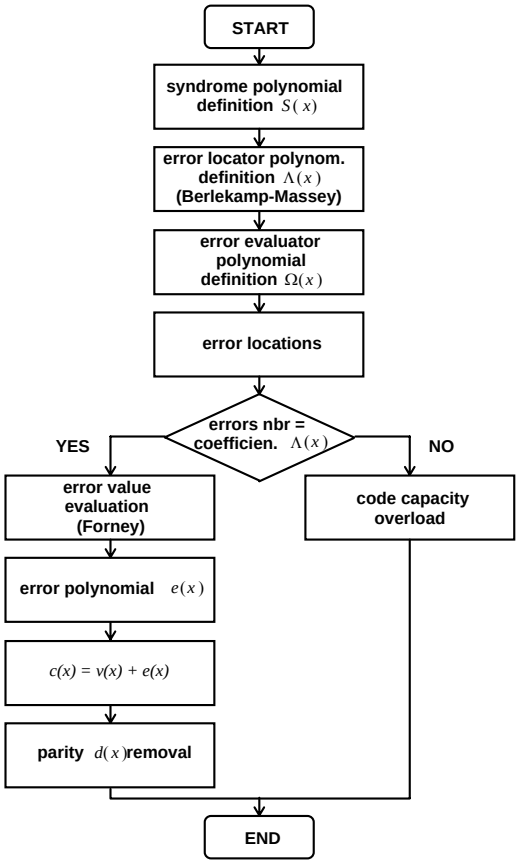

Fig. 2. Implemented FEC1 decoder flowchart diagram.

The decoder (Fig. 2) [7] deals with the word $v(x)$ that was received after transmission. The code word $c(x)$ is overlaid with the errors that are represented by the word $e(x)$ (all words are polynomials). The polynomial of a received code can be figured out in roots of generator polynomial $g(x)$ used in transmitter and these roots are powers of the primitive element α. The computation of the syndrome $S(x)$ means an enumeration of $v(x)$ in powers of the primitive polynomial α. The syndrome contains the location numbers and unknown values of errors. Error locator polynomial $\Lambda(x)$ roots are the inversion of location numbers. Error evaluator polynomial $\Omega(x)$ is exactly related with the position and value of single errors. The error locator polynomial method evaluation uses iterative technique in approximation of the locator polynomial. The values of errors are obtained by Forney algorithm that operates with the $\Lambda(x)$ and $\Omega(x)$. With the knowledge of the error values and error position the error polynomial $e(x)$ can be evaluated. After the errors removal the parity check could be done. If the number of errors is not equal to error locator polynomial coefficients the code capacity is overload and the decoder will fail.

3.2 FEC2 Decoder Implementation

The convolution code is binary oriented and a correction of binary errors is possible only with bit inversion after the error localization. The efficiency of a convolution code depends on the length of the used shift register in a coder and its content determines the state of the coder.

Viterbi algorithm of the decoder (in Fig. 3) [7] is a wide-spread decoding technique of convolution codes. A decoder receives the code sequence and creates an estimated message *v*' of a code word *v*. This estimation minimizes Hamming distance between the received sequence *r* and the transmitted sequence *v* (it seeks for such a code word that is different at least positions). To find this code word the trellis diagram is searched through and the paths that don't lead to the minimal Hamming distance are removed. Only one path is reserved for one state at each moment. If the coder was in an initial state, only one path remains after the search. If the initial state is unknown, the path with the minimal Hamming distance is selected. The branch metric is evaluated for each time t and each state $S(t)$ and it is equal to Hamming distance of the received bit sequence to the other sequences in the same state. The path metric μ for each subsequent state $S(t)$ is equal to the sum of the branch metric and the path metric of the previous state $S(t\text{-}1)$.

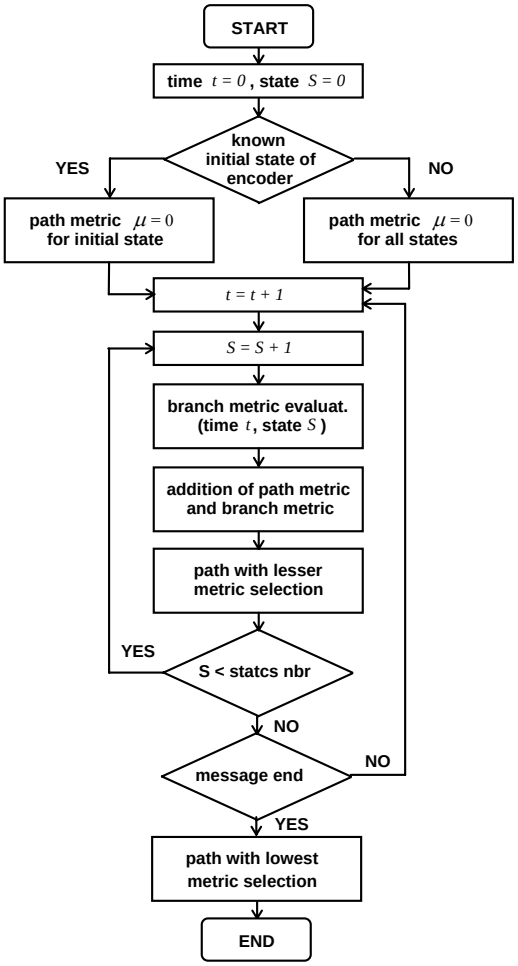

Fig. 3. Implemented FEC2 decoder flowchart diagram.

The Viterbi algorithm procedure at a glance:

- if the initial state S is known, the path metric is set to $\mu = 0$,
- for each state $S(t+1)$ the branch metrics of all incoming branches are determined and added with a path metric of a previous state. The lesser path metric is selected for the state $S(t+1)$,
- at the end of a trellis diagram (after the metric determination for the last input bits) the decoded word with the minimal path metric is chosen.

A deeper theory, mathematics description and equations of the outlined RS and the convolution decoder algorithm are available in [7], [8], [9] and also in references quoted there.

4. Digital Video Compression, Coding and Transmission in the Laboratory

The setup of experimental transmission of digital video in the laboratory is in Fig. 4.

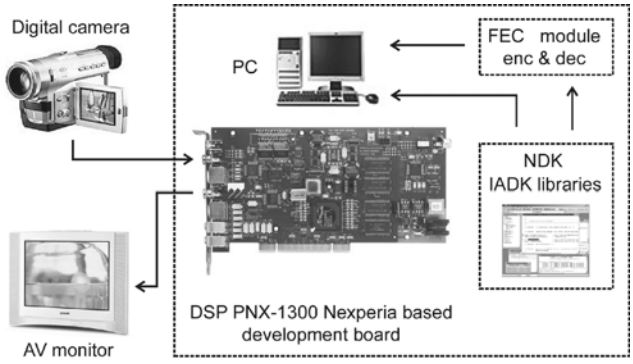

Fig. 4. The illustrative setup of an experimental digital video transmission in the laboratory.

The video source is a standard camera with the analog video output connected to DSP development board that has integrated ADC encoder SAA7121. After the conversion the digital video samples YUV are available. The output digital video is converted by the DAC decoder SAA7113 and an analog output is displayed on any AV monitor. The DSP development board is forced by the PC and NDK (Nexperia Development Kit) including the MPEG libraries IADK operates in real time. The FEC1 and FEC2 encoders and decoders are external modules and provide the channel coding of multimedia and packet data video stream. The computational time and the real time processing depend on a PC performance.

5. Conclusion

The experimental application of channel coding of multimedia digital video using DSP development board TM-13 IREF was presented in this paper. The channel coding provides the resistance against errors during the transmission of coded video data. These errors are occurred in transmission media and they are usually caused by any perturbation. The described transmission uses the model that makes the definition of the random errors of digital data. The observer can evaluate the errors on the AV monitor screen in spatial area (visual information) and the subsequent subjective evaluation of video quality is possible. Due to block based MPEG compression the image

artefacts are easy visible according to an amount of errors that are imposed on transmitted packets of a digital video stream. The channel model parameters have not been discussed yet. The model of the perturbation should be defined more exactly (limited bandwidth) and motivates to future research work.

Acknowledgements

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References

[1] KRATOCHVÍL, T. Utilization of Matlab for Digital Image Transmission Simulation Using the DVB Error Correction Codes. *Radioengineering*, 2003, vol. 12, no. 4.

[2] *MDS TM-13 IREF Datasheet*. Momentum Data System, Inc., www.mds.com, 2002.

[3] *Data Book, PNX1300 Series Media Processor*. Philips Semiconductor Inc., www.semiconductors.philips.com, 2002.

[4] RICHARDSON, I. E. G. *Video Codec Design, Developing Image and Video Compression system*. John Wiley & Sons, Ltd., 2002.

[5] *IADK 1.0 SP 1 Release notes.* Philips Semiconductor Inc., 2002.

[6] RIEMERS, U. *Digital Video Broadcasting, The Family of International Standards for Digital Television* (second edition). Springer, 2004.

[7] SLANINA, M. *Implementation of Image Transmission and Channel Coding FEC in Area DVB.* M.Sc. student project, FEEC BUT, Brno, 2004 (in Czech).

[8] WICKER, S. B., BHARGAVA, V. G. *Reed Solomon Codes and Their Applications.* IEEE Press, 1994.

[9] JOHANNESSON, R., ZIGANGIROV, K. S. *Fundamentals of Convolution Coding.* IEEE Press, 1999.

About Authors…

Tomáš KRATOCHVÍL was born in Brno, in 1976. He received the M.Sc. degree in electronics and telecommunications from the Brno University of Technology in 1999. From 1999 he is a Ph.D. student at the Department of Radio Electronics, from 2001 employed as an assistant professor here. His research interests include digital television and video technique area, modeling of the transmission through the transmission channel models, real time video capturing and application of modern compression methods on DSP, video codec design etc. He is a supervisor of the Junior research grant project of the Grant Agency of the Academy of Sciences of the Czech Republic (2003-2004), IEEE member.

Martin SLANINA was born in 1981. He is a master degree student of electronics and telecommunications at the Brno University of Technology. In 2005 he will finish his study with diploma work "*Implementation of image transmission and channel coding FEC in area DVB*".

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