

# Static and Dynamic Nonlinearity of A/D Converters

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**Abstract.** *The dynamic range of broadband digital system is mostly limited by harmonics and spurious arising from ADC nonlinearity. The nonlinearity may be described in several ways. The distinction between static and dynamic contributions has strong theoretical motivations but it is difficult to independently measure these contributions. A more practical approach is based upon analysis of the complex spectrum, which is well defined, easily measured, and may be used to optimize the ADC working point and to somehow characterize both static and dynamic nonlinearity. To minimize harmonics and spurious components we need a sufficient level of input noise (dither), which destroys the periodicity at multistage pipelined ADC, combined with a careful analysis of the different sources of nonlinearity.*

## Keywords

Dynamic and static nonlinearity, ADC, dynamic range, harmonics, spurious.

## 1. Introduction

ADC is often the most critical and performance-limiting component in broadband systems with high dynamic range. If harmonics and spurious signals may be neglected, it may attain a SNR of up to 150 dBFS/ $\sqrt{\text{Hz}}$ , which compares with the SNR figure of the best analog circuits. The reduction of performances is mostly related with ADC nonlinearity. Even today, it is hard to achieve a spurious free dynamic range (SFDR) higher than 100 dBFS. That is why it is important to measure and analyze the ADC nonlinearity, and to search ways to minimize its influence.

## 2. ADC Nonlinearity

Integral nonlinearity (INL) and hysteresis are often used to characterize the ADC nonlinearity [1-5]. These parameters are appropriate at low working frequencies or when the dynamic nonlinearity is small and frequency-independent. Usually, this is not the case for broadband systems. Some other description of ADC nonlinearity may be:

- Static and dynamic nonlinearity. This is the best description for system design and ADC modeling, but it does not translate into a direct measuring technique.
- Contributions to nonlinearity classified according to its sources such as: limited slew rate of sample-and-hold or input amplifier; periodicity at multistage pipelined ADC; coupling between analog and digital part, glitch feed-through, ... These descriptions assist the manufacturer in determining where the performance bottleneck is, and the user in selecting the appropriate working point of an acquisition system. But, again, these contributions are difficult to measure and analyze separately.
- Hard and soft ADC nonlinearity as the nonlinearity that corresponds to low order and high order harmonics terms [6], respectively.
- Analysis of the complex spectrum of the error signal at the output. This spectrum is easily measured, and it describes the quality of the acquisition system. The in-phase harmonic terms correspond to INL while the out-of-phase harmonic terms correspond to hysteresis.
- Other descriptions, not discussed here are: Bidimensional histogram [7]; Code-previous code domain [4]; Phase-plane [8, 5].

### 2.1 ADC with Only Static Nonlinearity

This ADC is a nearly ideal case, which is fully described by its input/output transfer function. The transfer function in graphic form is the INL; numerically, it is described with a Taylor or Fourier expansion. It defines unambiguously the output signal for a given input signal. The complex output spectrum may be computed from INL, and vice versa [9, 10]. In fact, in this case, the INL is independent from the choice of the input signal and all error signals are in phase with the input signal and yield harmonic terms. This may be simply demonstrated by a Taylor expansion of the transfer function. The output signal  $y$  is given by:

$$y = \sum_{i=0}^n a_i x^i \quad (1)$$

where  $x$  is the input signal. If the input signal is harmonic,  $\cos(\omega t)$ , then the output signal is:

$$y = \sum_{i=0}^n a_i \frac{1}{2^i} \sum_{k=0}^i \binom{i}{k} \cos \omega t (i - 2k). \quad (2)$$

The output signal is the sum of in phase terms only and the number of harmonics corresponds to order of the Taylor expansion.

## 2.2 ADC with Static and Dynamic Nonlinearity

Real ADC has always dynamic nonlinearity, which is usually the dominant contribution in broadband applications. We have two transfer functions: one for input signal going up  $y \uparrow(x)$ , and for input signal going down  $y \downarrow(x)$ . Mean level between them represents INL, and one half of their difference is the hysteresis [3].

Moreover, these transfer functions are now dependent upon the signal (frequency, amplitude, shape) and the sampling frequency. Dynamic nonlinearity contributes to both hysteresis and INL. This may be seen in the case of an ideal ADC with limited slew rate, which yields a “pure” dynamic nonlinearity. A limited slew rate produces both in-phase and out-of-phase error relative to the input signal. The in-phase error corresponds to INL and out-of-phase error corresponds to hysteresis. In a real ADC with both static and dynamic nonlinearity, the INL is given by the static nonlinearity plus the in-phase portion of the dynamic nonlinearity. Hysteresis is given by the out-of-phase portion of the dynamic nonlinearity.

Two issues have to be addressed when precise definitions of complex spectrum and hysteresis are sought. The in-phase and out-of-phase terms are defined relative to an input signal, but we analyze the distorted output of the ADC with some phase shift relative to the input. This phase shift is usually neglected, but this is no longer possible with significant dynamic nonlinearity. When computing the hysteresis, data should be sorted according to the slope (positive or negative) of the input signal slope. With sizable distortions, slopes of corresponding input and output signal may be different, and we need first to compute the slope of the output carrier signal [9], so that only the phase shift problem remains.

Today, the favorite way of describing the nonlinearity of ADC's is through INL and hysteresis. However, in a real ADC, both parameters are uniquely defined only for a specified input signal. For this reason a description based upon the complex spectrum may be better from the user point-of-view. Moreover, one should consider that:

- Complex spectrum provides the fundamental system parameters. SFDR is the basic parameter which determines the level of ghost signals. The level of error signals may be derived from INL and hysteresis only through computations; it follows that these parameters are not suitable to define a criterion of acceptance for a system, or for its optimization.

- Measurements of INL and hysteresis are based upon histograms, which require a substantially higher number of data points relative to the complex spectrum.
- Histograms for hysteresis require knowledge of the slope (positive/negative) of the input signal. However, the slope concept is no longer meaningful when we are undersampling, or near the Nyquist frequency. On the other hand, the complex spectrum is well defined also under these circumstances.

## 3. Spurious Free Dynamic Range of Acquisition Systems

Optimizing the SFDR is the main task of any design. The spurious signals may be distinguished into those due to the ADC and those due to the rest of the system. Before measuring the ADC contribution, the spurious due to the system must be reduced or suppressed. Among the most common reason of system non-ideality we may quote the following:

- Coupling between the analog and digital parts. Such coupling may be due to ground loops, insufficient decoupling, and others problems of PCB design. A white noise of low level (rms around 2 LSB) with no dc component should be applied to the ADC input signal to test this coupling. We measure the output noise as a function of sampling frequency; if the output noise increases with increasing the sampling frequency, the coupling exists.
- Imperfections of sampling frequency. Any jitter of sampling frequency produces error signals. A modulation of sampling frequency yields sidebands around the carrier [12]. Another evidence of jitter is a noise level which linearly increases with increasing input frequency.
- Problems with power supply, which may cause both coupling and jitter.

### 3.1 How to Increase the SFDR of ADCs

The ways to increase the SFDR of an ADC are:

- Dither, or sufficient input noise. An ideal ADC needs a minimum of 0.35 LSB rms of noise, or the quantization error appears as a spurious [6]. A higher noise may also minimize spurious given by DNL, but attention should be paid in suppressing any periodicity. For this reason, in multistage pipelined ADC the last bit of the first stage must be randomized with sufficient level of dither or noise [13]. Dither or noise chiefly minimizes spurious given by static nonlinearity and has much less influence upon dynamic nonlinearity.
- ADC data post processing. Some methods have been tested to minimize harmonic distortion by data post

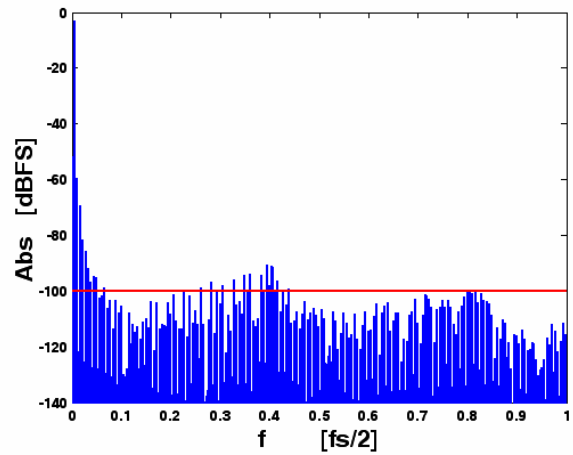
processing [14, 15]. Practical applications are limited to dominant static nonlinearity or to narrow area of input signal and measurement parameters.

- Optimal working point of ADC. SFDR as a function of input signal frequency ( $f_{in}$ ) and amplitude, sampling frequency ( $f_s$ ) and ratio  $f_{in}/f_s$  may be used to optimize the working point. Unfortunately, the relevant information is seldom given with the ADC specifications, and the user should find it himself.
- Summing the data of several synchronized ADC connected in parallel. This is an expensive method, which may be used only in top level systems.

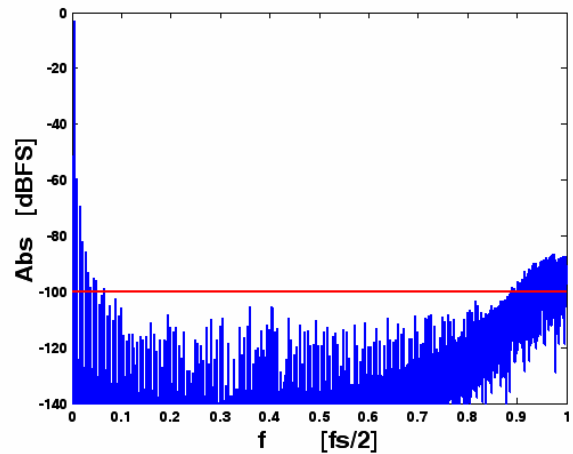
### 4. Measurement

The following measurements were carried out with a home made, two-channel acquisition system [16] with two AD6644 (Analog Devices, 14 bits,  $f_s$  up to 66 MHz). We give only data for a single channel, since the other channel behaves similarly. Our carrier was a pure harmonic at 90.031425 MHz with amplitude 3dB below full scale (FS), with or without a dithering noise, passband filtered with an rms of 512 LSB. We were in the undersampling mode, and sampling achieved the frequency conversion. The sampling frequency  $f_s$  was coherent with the input; we used 29.982720 or 59.96544 MHz, that will be quoted as  $f_s=30$  and  $f_s=60$  MHz in the following. The two sampling frequency allow the measurement of sample and hold nonlinearity. With 30 MHz the influence of sample and hold is minimal (*Beat frequency test*), with 60 MHz the influence is maximal (*Envelope test*). The dynamic range according to noise for this carrier was 135.3 dBFS/ $\sqrt{\text{Hz}}$  at sampling frequency 30 MHz and 137.9 dBFS/ $\sqrt{\text{Hz}}$  at sampling frequency 60 MHz. Corresponding jitter of sampling signal was 1.3 ps (30 MHz) and 1.2 ps (60 MHz). The data with  $f_s=60$  MHz were decimated by two before the processing, to achieve identical data format and the same occurrence of harmonics. For hysteresis computation, the histograms were sorted according to the sign of the aliased carrier slope.

The main aim of the measurement was to test the dynamic nonlinearity of sample and hold. According to [13] and our experience with older ADCs, the dynamic nonlinearity of sample and hold may be the most important source of spurious. With given measurements, based on undersampling applications, the other important nonlinearity (input amplifier and DNL) have the same occurrence in all measurements and the contribution of sample and hold may be analyzed. Such analysis of sample and hold nonlinearity in basic Nyquist band is nearly impossible. Some secondary aim was to test the achievable dynamic range at the broadband direct digital receiver with carrier round 90 MHz.



a) The input signal is pure harmonic, amplitude FS-3 dB.



b) The input with an analog band pass dither of 512 LSB rms amplitude.

Fig. 1. Power of harmonics terms,  $f_s=30$  MHz. The noise level is -130 dBFS, the carrier is at 0.055  $[f_s/2]$ .

Harmonics	Mean power, [dBc]			
	2÷5	6÷10	11÷30	31÷50
S , 30 MHz	-70.2	-92.3	-101.7	-99.6
S+D, 30 MHz	-70.3	-93.1	-103.2	-109.5
S , 60 MHz	-80.2	-88.1	-94.5	-96.0
S+D, 60 MHz	-75.4	-88.9	-98.7	-106.4
Mean out of phase power [dBc]				
S , 30 MHz	-70.7	-97.3	-104.9	-113.0
S+D, 30 MHz	-70.7	-97.1	-105.2	-118.9
S , 60 MHz	-88.0	-90.0	-96.9	-101.7
S+D, 60 MHz	-78.9	-90.9	-100.6	-111.8

Tab. 1. Mean power of harmonics terms in given area. S- input is pure harmonic signal; S+D – input is harmonic signal with dither.

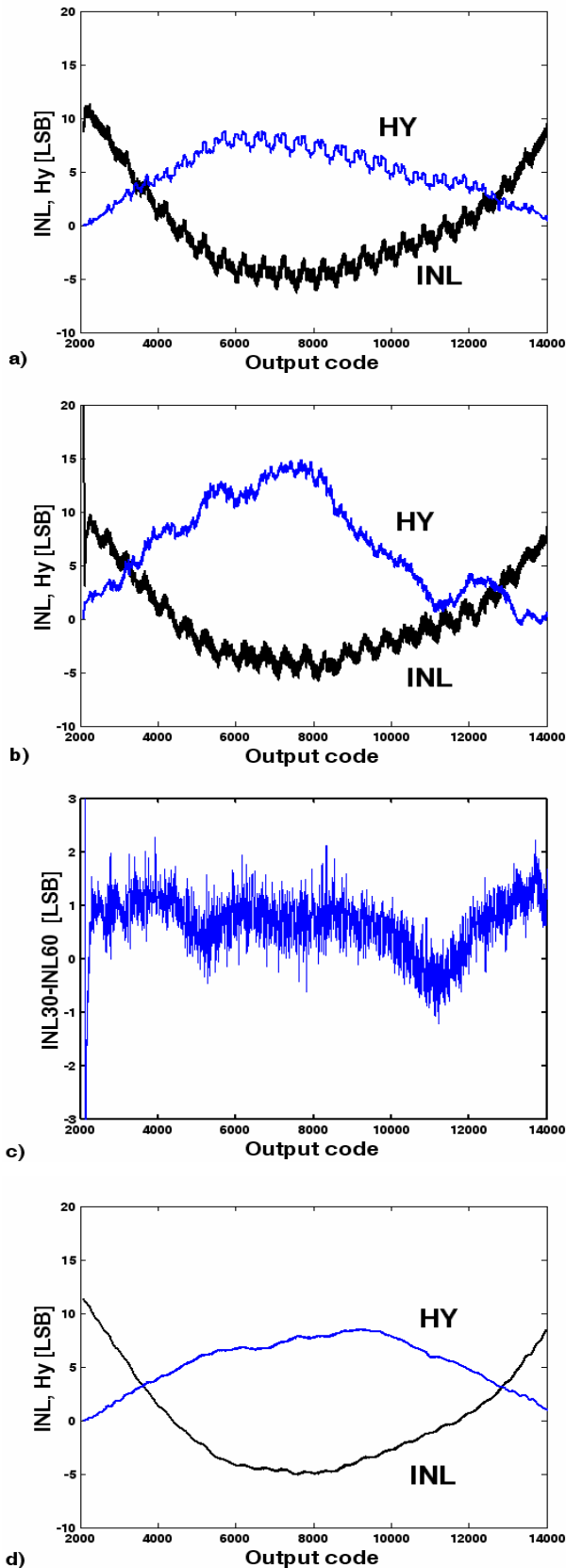


Fig. 2. INL and hysteresis. a)  $f_s=30$  MHz; b)  $f_s=60$  MHz; c) The difference between INL at  $f_s=30$  MHz and INL at  $f_s=60$  MHz; d) Dither and  $f_s=30$  MHz. During the data processing first the dither was filtered out and after that the corresponding histograms were computed.

## 5. Discussion

The ADC nonlinearity produces high order harmonic terms. In Fig. 1 the harmonics terms up to 200<sup>th</sup> are visible. The amplitude of hysteresis is comparable with INL amplitude and the power of out-of-phase terms is comparable with the power of in-phase terms, so significant dynamic nonlinearities are demonstrated by this measurement. The periodicity given by two last stages of this 3 stage pipelined ADC is remarkable on INL and hysteresis with  $f_s=30$  MHz (Fig. 2a). This periodicity is partly randomized if  $f_{in}$  is near to odd multiple of  $f_s/2$  (Fig. 2b). In this case the influence of dynamic nonlinearity of sample and hold is maximal and this nonlinearity partly randomizes periodicity.

With a sufficient level of dither the periodicity on INL and hysteresis disappears (Fig. 2d) and amplitudes of higher order harmonic terms are lower (Fig. 1b, Tab. 1.). About 10 dB attenuation is achieved from 20<sup>th</sup> harmonics. The amplitudes of low order harmonic terms (up to 5<sup>th</sup>) do not depend on dither, if  $f_{in}$  is near to an even multiple of  $f_s/2$ . If  $f_{in}$  is near to an odd multiple of  $f_s/2$ , the amplitudes depend on dither and they are higher. This is because the dither of a high level affects the nonlinearity due to the sample and hold, which adds to the other non-linear effects. With our ADC, the sample and hold nonlinearity tends to compensate the nonlinearity due to low order harmonic terms. The result is that the amplitude of low order harmonic term without dither is lower at  $f_s=60$  MHz than at  $f_s=30$  MHz.

The long term and short term reproducibility and stability were tested before [17]. Here, we address the problem of increasing the SFDR by post-processing. The basic prerequisite is a constant distortion over a sufficiently wide interval of input signal parameters. To test this condition, we subtracted two complex spectra from different measurements. In the difference plot, the attenuation of harmonics is less than 100 dB only with  $f_s=30$  MHz: 2<sup>nd</sup> harmonics  $-90$  dB, the others more than  $-100$  dB, at all others differences attenuation from 2<sup>nd</sup> to 4<sup>th</sup> harmonics is less than 80 dB. With  $f_s=60$  MHz the dynamic nonlinearity is significant; in this case, some post correction would be advisable only in a very narrow area of input signal, and has no practical relevance.

The dynamic nonlinearity is mostly apparent from hysteresis and out-of-phase harmonic terms. INL and in-phase harmonic term are somehow affected by dynamic nonlinearity. Therefore, the exact contribution of static and dynamic nonlinearity can not be determined with the measurements given here. Fig. 2c demonstrates that INL at  $f_s=30$  and  $f_s=60$  MHz are essentially the same; in fact, the nonlinearity of the input amplifier (verified by the dependence upon  $f_{in}$  and input amplitude) gives the main contribution in both cases.

The low order and high order harmonic terms should be analyzed independently. They differ: i) in the origin; ii) in the behavior in the presence of dither; iii) in the risk they pose to the system performance. The high order harmonics

terms have lower amplitudes, but the number of terms is nearly unlimited and they are spread over all Nyquist bands. Since we have more spurious than harmonics, they are potentially more difficult to handle.

The basic ADC nonlinearity (input amplifier, sample and hold, DNL) are of the comparable weight at this ADC and supposed carrier 90 MHz. The achievable SFDR is -100 dBFS. About 10 dB better SFDR may be achieved in basic Nyquist band, but such a design has other disadvantages in an analog part.

## 6. Conclusion

Harmonics and spurious are still limiting factors in broadband digital systems. Minimization of harmonic terms should be based upon a faultless system design, a sufficient level of input noise or dither, and on an optimal working point of ADC. Some ADC post correction has sense if, and only if, the dominant ADC nonlinearity is static.

The analysis and optimization should be based before all on complex spectrum, although the INL and hysteresis are preferable to compare ADC standards. The high order and low order harmonic terms should be analyzed independently since these terms differ in origin and behavior. The same holds true for static and dynamic ADC nonlinearity.

## Acknowledgements

The research described in the paper was supported by the Czech Grant Agency under grant No. 102/02/0553.

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