# X-Band PLL Synthesizer

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**Abstract.** *This paper deals with design and realization of a PLL synthesizer for the microwave X−band. The synthesizer is intended for use as a local oscillator in a K−band downconverter. The design goal was to achieve very low phase noise and spurious free signal with a sufficient power level. For that purpose a low phase noise MMIC VCO was used in phase locked loop. The PLL works at half the output frequency, therefore there is a frequency doubler at the output of the PLL. The output signal from the frequency doubler is filtered by a band-pass filter and finally amplified by a single stage amplifier.*

## Keywords

Microwave PLL synthesizer, phase locked loop, low phase noise, local oscillator, X-band.

## 1. Introduction

The PLL synthesizer is intended for use as a local oscillator in the K−band downconverter for a satellite receiver. The local oscillator (LO) signal directly affects the properties of an intermediate frequency (IF) signal and consequently the quality of the received information. If the LO signal had some spurious spectral components, it may cause conversion of unwanted signals to IF. A phase noise of the LO causes a distortion of the converted signal, especially in the case of phase modulation. Therefore, it is important to achieve a low phase noise, and a spurious free signal of the local oscillator.

The best results can be obtained with a dielectric resonator oscillator [1], especially if it is phase-locked [2]. However, components for dielectric resonator oscillator design are not commonly available. Therefore, we decided to design a low cost solution using commercially available integrated circuits.

## 2. Conception and Design of the PLL Synthesizer

The block structure of the whole PLL synthesizer is shown in Fig. 1. A VCO running at a half of the desired output frequency was available. Therefore, the PLL works

at 5.976 GHz and its frequency is multiplied by two to achieve 11.952 GHz. Unfortunately this compromise brings in phase noise degradation of the output signal by 6 dB compared to the PLL signal.

The phase locked loop is designed using monolithic microwave integrated circuits produced by Hittite Microwave Corporation. The HMC431 voltage controlled oscillator running on the frequency of 5.976 GHz is phase locked to a reference signal at 119.52 MHz. The reference signal is generated by the 5th overtone quartz oscillator. This promises a low phase noise close to the carrier. Signals from the reference oscillator and the feedback loop come to inputs of the digital phase-frequency detector (PFD) HMC439. The PFD is intended for use in low noise PLL applications because of its ultra low phase noise floor. The output signal of the PFD is filtered by the active loop filter utilizing the fast and low noise operational amplifier THS4031. The VCO delivers about 2 dBm of output power to a microstrip directional coupler. The coupled signal is used as feedback and it is divided by a divider chain with the total division ratio of 50. This results in the frequency of 119.52 MHz according to the reference signal. Two divide-by-5 HMC438 and one divide-by-2 HMC364 low noise dividers are used.
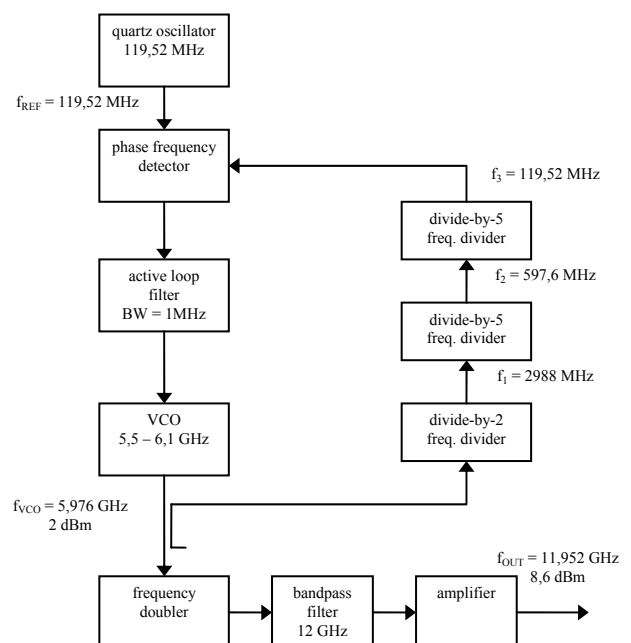


**Fig. 1.**   The block structure of the PLL synthesizer.

## 2.1 The Loop Filter Design

Outside the loop bandwidth, the noise of the free-running VCO is the dominant noise contributor. The VCO phase noise is suppressed inside the loop bandwidth. According to [3] the loop filter bandwidth was designed to be 1 MHz (see Fig. 2). This should ensure a minimal phase noise of the PLL.
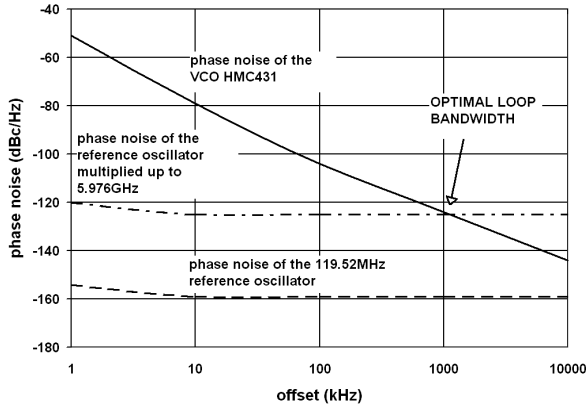


**Fig. 2.** The choice of the loop bandwidth.

Fig. 3 shows an active loop filter with an op-amp. *PD D OUT* and *PD U OUT* are differential outputs of the phase detector.
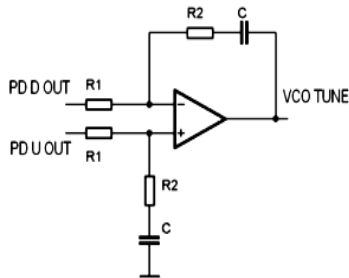


**Fig. 3.** The active loop filter.

Our system is a second order type II PLL. The natural frequency $\omega_n$ and damping factor $\xi$ are given by:

$$\omega_n = \sqrt{\frac{K}{\tau_1}} \,, \ \xi = \frac{\tau_2}{2}\sqrt{\frac{K}{\tau_1}} \tag{1), (2}$$

with $K = \dfrac{K_\phi \cdot K_V}{N}$ . $\tag{3}$

$K_\Phi$ is the phase detector gain and $K_V$ is the VCO tuning sensitivity. Time constants

$$\tau_1 = R_1 C \ \text{ and } \ \tau_2 = R_2 C \tag{4), (5}$$

are based on the active loop filter components. $N$ is the divide ratio between the VCO and the phase detector. The loop bandwidth $B_{3dB}$ is given by:

$$B_{3dB} = \frac{\omega_n}{2\pi}\sqrt{2\xi^2 + 1 + \sqrt{\left(2\xi^2+1\right)^2 + 1}} \ . \tag{6}$$

For our application the following values were given:

$K_V = 558 \cdot 10^6$ rad/s/V,

$K_\Phi = 0.318$ V/rad .

The damping factor $\xi$ is a measure of stability of the PLL and it influences the settling time of the loop. In the case of our local oscillator, there is no need of a short settling time. Therefore the damping factor was chosen to be $\xi = 1$, to avoid stability problems.

Now, if we know the values of $\xi$ and $B_{3dB}$, we can (from equation (6)) calculate the natural frequency $\omega_n$. Then for known $K_\Phi$, $K_V$ and $N$, we calculate $K$ from (3) and the time constants $\tau_1$ and $\tau_2$ from (1) and (2). If $R_1$ is chosen to be 400 $\Omega$, then $C$ and $R_2$ are left to be calculated from (4), (5). The resulting values are $C = 1.5$ nF and $R_2 = 580$ $\Omega$.

The steady-state phase error, caused by op-amp input offsets or other imbalances, results (on the phase detector output) in error pulses of a large amplitude and a short duration. This signal can cause nonlinear saturation in the amplifier, reducing its gain bandwidth. This effect is undesirable to wide bandwidth PLLs. One solution is to prefilter the error pulses before they reach the active filter by inserting a RC low-pass filter by splitting $R_1$ and adding $C_C$ (see Fig.4). The capacitor value $C_C = 390$ pF was calculated from:

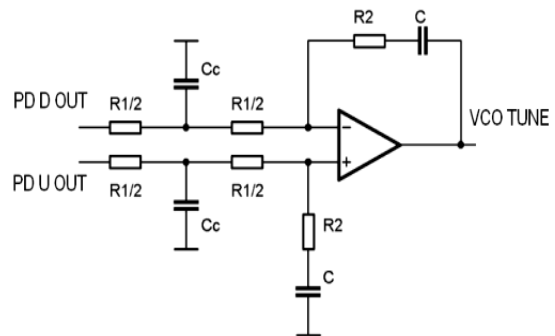$$C_C = \frac{4}{10 \cdot \omega_n \cdot R_1} \tag{7}$$



**Fig. 4.** The active loop filter with the pre-integrator.

## 2.2 Directional Coupler, Frequency Doubler, Band-Pass Filter and Amplifier Design

The directional coupler consists of quarter wavelength microstrip coupled lines. The coupling loss is approximately 12 dB which, ensures an excitation power of about -10 dBm at the input of the frequency divider. The unused gate is terminated using a characteristic impedance and RF ground (Fig. 5).

An active frequency doubler utilizing one MGF1302 GaAs FET was designed to multiply the PLL frequency by 2. The frequency doubler simulated conversion gain is about 0.3 dB. To obtain a clear output spectrum, the resulting signal is filtered by a band-pass filter. The filter consists of two coupled half−wave resonators and its insertion loss is only 0.6 dB at the center frequency of

11.952 GHz. The filtered signal is amplified by a single stage amplifier. The amplifier is designed using MGF1303 with a simulated gain of 8.4 dB. The total conversion gain of the frequency doubler, band-pass filter and amplifier is 7.9 dB. The simulated output power of the PLL synthesizer is almost 10 dBm. More detailed information about the design can be found in [4].
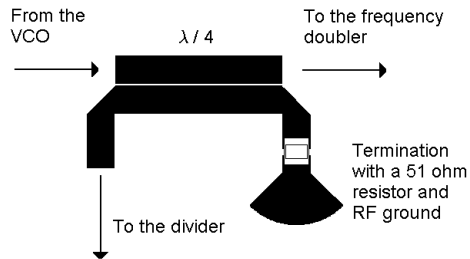


**Fig. 5.** Microstrip directional coupler.

Fig. 7 shows a photograph of the PLL synthesizer without the reference quartz oscillator. The reference oscillator is attached to the synthesizer via the SMA connector. The PLL synthesizer PCB material is the microwave substrate DiClad 870 with gold metallization.
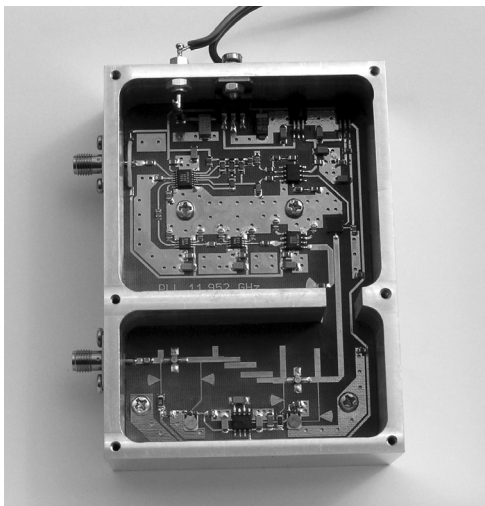


**Fig. 7.** The X-band PLL synthesizer.

## 3.  Measured Results

Overall phase noise of the PLL synthesizer was predicted in terms of the loop filter bandwidth, phase noise floor of the frequency dividers and free running VCO phase noise. The dashed line in Fig. 8 shows the estimated phase noise of the PLL synthesizer. Numerical values are given in Tab. 1.

The direct spectrum analyzer phase noise measurement method was available. RF spectrum analyzers measure spectral density directly, provided that the phase noise of the source under test is significantly its AM noise. Limitations of this direct method are phase noise of the spectrum analyzer LO, dynamic range and resolution [1].
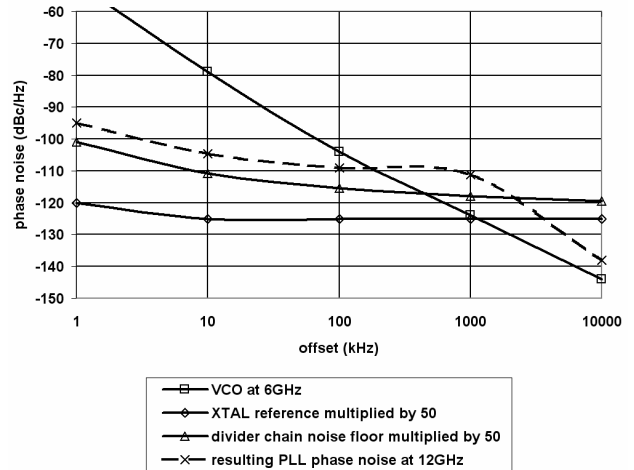


**Fig. 8.** The estimated phase noise of the PLL synthesizer.

| $f_{offset}$ (kHz) | phase noise (dBc/Hz) |
|---|---|
| 1 | -95 |
| 10 | -105 |
| 100 | -109 |
| 1000 | -111 |
| 10000 | -138 |

**Tab. 1.** The estimated phase noise.

Fig. 9 shows the spectrum of the output signal close to the carrier measured using HP E7404A spectrum analyzer. We can see that the spectrum is without any spurious components. Power level of the carrier is 8.6 dBm, which is only 1.4 dB less than the simulated value.
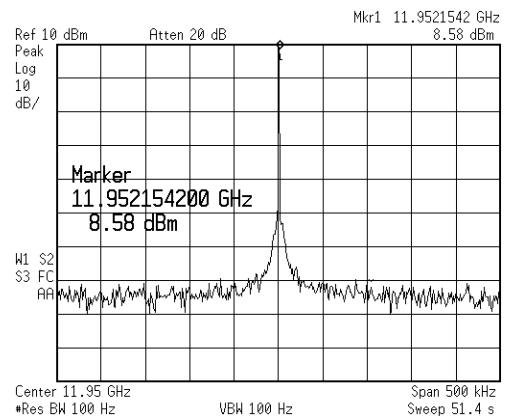


**Fig. 9.** The measured spectrum of the output signal – SPAN 500 kHz, RBW 100 Hz, 10 dB/div.

Fig. 10 shows the spectrum of the output signal from 1 GHz to 13 GHz. It is obvious that there is only one undesirable signal at the frequency of 5.976 GHz. It is the fundamental frequency of the VCO, suppressed by 28 dB compared to the PLL synthesizer's first harmonic. There are no more spurious spectral components in wide bandwidth so we can say that the spectral purity is much better than in the case of a signal source realized by means of multiplying a quartz oscillator (see Fig. 11).
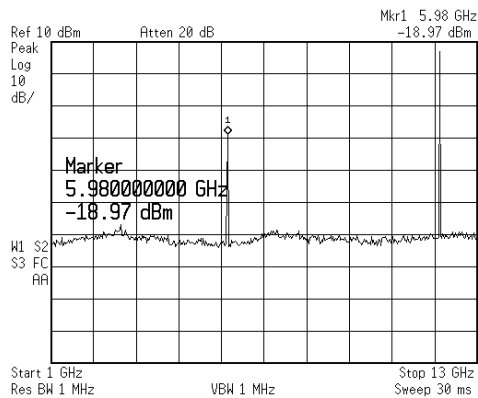
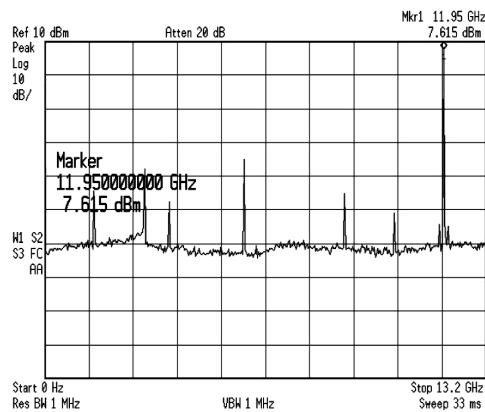**Fig. 10.** Spectrum of the PLL synthesizer from 1 GHz to 13 GHz.



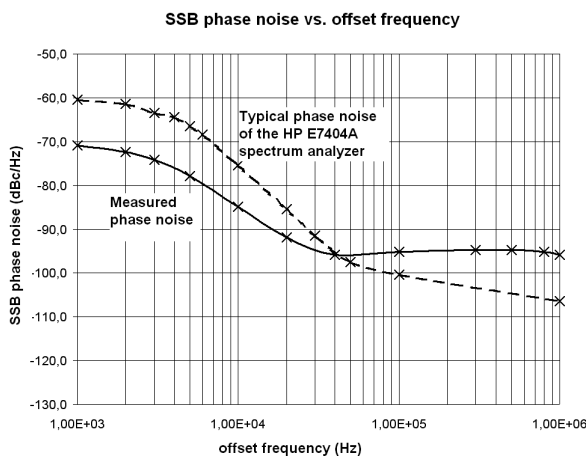**Fig. 11.** The spectrum of a multiplied quartz oscillator.



**Fig. 12.** The typical phase noise of the HP E7404A and the measured phase noise of the PLL synthesizer at 12 GHz.

As we can see in Fig. 12, the measurement is distorted because of the spectrum analyzer LO phase noise. The dashed line shows a typical phase noise of the HP E7404A at a center frequency of 12 GHz [5]. The solid line shows our phase noise measurement results. At offset frequencies lower than 40 kHz, we have measured even lower phase noise than the typical spectrum analyzer LO phase noise. Therefore we can say that we have measured the most likely phase noise of the spectrum analyzer LO. Hence we can assume that the phase noise of the PLL synthesizer is lower than -71 dBc/Hz at an offset frequency of 1 kHz and lower than -85 dBc/Hz at 10 kHz.

| Output frequency | 11.952 | GHz |
|---|---|---|
| Output power | 8.6 | dBm |
| Estimated phase noise $f_{offset}$ = 1 kHz | -95 | dBc/Hz |
| $f_{offset}$ = 10 kHz | -105 | |
| Reference signal frequency | 119.52 | MHz |
| Supply voltage | +12 | V |
| Supply current | 510 | mA |

**Tab. 2.** X-band PLL synthesizer - main characteristics.

## 4. Conclusion

In this paper the design and realization of the local oscillator for the K−band downconverter is presented. The LO consists of the PLL synthesizer and the reference quartz oscillator. The output frequency of the PLL synthesizer is 11.952 GHz with a power level of approx. 8.6 dBm. Phase noise measurement has shown the phase noise to be lower than -71 dBc/Hz at the offset frequency of 1 kHz. We estimate that the true value is -95 dBc/Hz at this offset. The output signal spectrum is clean and there are no spurious signals close to the first harmonic. The realized PLL synthesizer meets the design requirements and can be used as a low-phase-noise local oscillator.

## Acknowledgements

## References

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