# Novel Optimization Method of Active Frequency Multiplier Utilizing Harmonic Terminating Impedances with DGS

*Petr KUTÍN, Miroslav KASAL*

Dept. of Radio Electronics, Brno University of Technology, Purkyňova 118, 612 00 Brno, Czech Republic

kutin@feec.vutbr.cz, kasal@feec.vutbr.cz

**Abstract.** *A novel method for the optimization of the active frequency multiplier utilizing the harmonic terminating impedances with the defected ground structures (DGS) has been developed. Furthermore, a new type of the low-pass filter with DGS for the higher harmonic suppression will be reported. Experimental conversion gains (14.52 dB for the doubler, 5.56 dB for the tripler and 0.43 dB for the quadrupler) and real power-added efficiency (32.76 % for the doubler, 10.15 % for the tripler and 1.42 % for the quadrupler) have been attained. To our knowledge, in the considered frequency range, these results represent the best performance reported up to date for the active frequency multipliers utilizing the low-cost BJTs.*

## Keywords

Frequency multiplier, defected ground structure, DGS, harmonic terminating, low-pass filter, optimization.

## 1. Introduction

A lot of papers have been published on the topic of the active frequency multipliers. At microwave frequencies, these techniques usually employ a nonlinear device generating the desired multiple of the fundamental input frequency. Two main problems have been solved. A set of optimal bias/drive regimes of operation [1]-[4] is the first problem and a choice of the proper harmonic terminating for the improving of the frequency multiplier performance [5]-[9] is the second problem.

Gopinath et al. [1] utilized a detailed $I_{ds}$ model for the FET, which describes the influence of various aspects of the nonlinear device on its multiplying behavior. Maas [2], on the other hand, applied a generic piecewise linear transconductance (PLT) model, where only $I_{ds}$ clipping effects are considered, to develop a generalized multiplier biasing and drive criteria. Maas's approach is consistent with the findings of [1], in which the $I_{ds}$ clipping contribution is the most significant factor affecting harmonic generation. However, another development [3] has demonstrated an alternative tripler-bias arrangement, which has the potential to perform with significantly better results than would be predicted by the earlier theoretical models. This improvement has been explained analytically, but it has not been shown conclusively whether it is the true optimum or whether further improvements are even possible. Moreover, it also casts some doubt on conclusions drawn regarding frequency doublers in the conventional analysis. O'ciardha et al. [4] combine the best of the Gopinath et al. and Maas techniques. The goal has been to study and, if necessary, to refine the multiplier design criteria of Maas by applying the PLT model in a more generalized and more extensive harmonic analysis.

In many frequency multiplier design approaches, the operating performance is improved by the proper selection of input and output circuit terminating impedances at the fundamental and the harmonic frequencies. Rauscher [5] performed a detailed study of the doubler behavior based on the fundamental frequency drive level, the device output terminating impedance at the fundamental frequency, and the device input terminating impedance at the second harmonic frequency. He concluded that the optimal output load at the fundamental frequency is a short-circuited stub at an optimal distance from the FET drain. The FET model in Rauscher's study used approximations and only the simulated data were employed in the conclusion on the output termination effects. Experimental circuits built by Rauscher based on his analysis provide responses which required trimming and tuning screws to approximate simulations. In pursuit of the optimal performance, it is important that the analysis contains both the simulated and the measured data. The measured results show the practicality of the designs and the accuracy of the models which contain approximations. Camargo [6] performed the most in-depth research in this area, concluded that the optimum MESFET doubler operation is obtained when the drain is terminated at the fundamental frequency by purely reactive circuit which resonates the transistor's output capacitance. Borg et al. [7] suggested that the optimum terminating impedance for the bipolar multiplier is a short circuit at the fundamental frequency. Thomas et al. [8] presented a quantitative optimization analysis of the active multiplier conversion gain and the spectral purity as governed by the

fundamental and the harmonic terminating impedances and regions of nonlinearity. Johnson et al. [9] presented the novel design and optimization techniques for the frequency triplers. Accurate CAD techniques are utilized to develop bias, input power, input network and output network configurations for the optimum third harmonic response. As a result, the microwave frequency tripler is developed, which exhibits an unprecedented level of conversion gain 3.67 dB with 3 GHz input frequency.

Recently, there has been an increasing interest in studying the defected ground structure (DGS) provides a rejection band in some frequency range and circuit size reduction due to increase of effective inductance of a transmission line. The DGS is realized by etching only a few areas on the ground plane under the microstrip line and gives a significant advantage in applicability to microwave circuits, such as filters, dividers, couplers, amplifiers and oscillators [10]-[15].

This paper includes advanced techniques for the set of optimal bias/drive regimes of the operation using the modified nonlinear model of a bipolar transistor, the detailed study of harmonic termination of a bipolar transistor and its implementation with DGS. A new type of the low-pas filter with DGS, which improves a spectral purity, has been developed as well. Three types of active microwave frequency multipliers were considered, the frequency doubler, the tripler and the quadrupler. Measured results for the proposed frequency multipliers correspond to simulations. The Ansoft Designer simulator, which combines the harmonic balance analysis with the full wave analysis for the planar circuits, was used for all simulations.

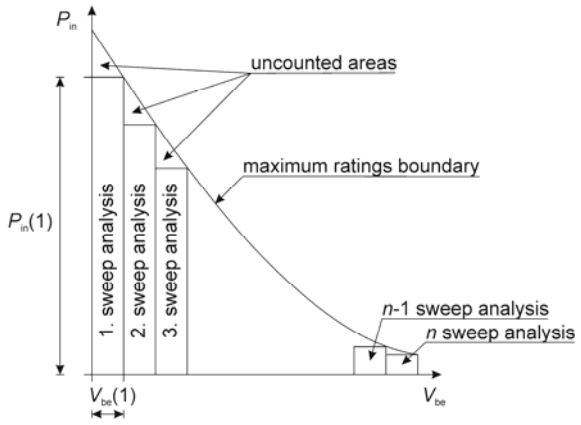


**Fig. 1.** Principle of the optimal bias/drive regimes of operation analysis for a single-ended active frequency multiplier.

## 2. Optimal Bias/Drive Regimes of Operation Analysis

The method for the optimal bias/drive levels determination is based on the graphical representation (2D or 3D) of the desired parameter of the frequency multiplier. The most important parameters of the frequency multipliers are the output power $P_{out}\langle H_m\rangle$, the real transducer gain $TG\langle H_m\text{-}H_n\rangle$ and the real power-added efficiency $PAE\langle H_m\text{-}H_n\rangle$. Independent variables are the emitter voltage $V_{be}$, the collector voltage $V_{ce}$ and the input power $P_{in}$. Principle of this method is shown in Fig. 1. To avoid errors a simulation needs to be counted under the maximum rating boundary line. Each analysis consists of the series of smaller sweep analysis touching the boundary. There are uncounted areas which can be eliminated by increasing the number of the sweep analyses, but this is time consuming and it complicates set up of the complete analysis. A harmonic balance simulator and an accurate nonlinear model of the transistor are needed for this analysis. The example of the output power simulation for the second harmonic frequency of the bipolar transistor is shown in Fig. 2. The input and output termination of the transistor is 50 Ω.

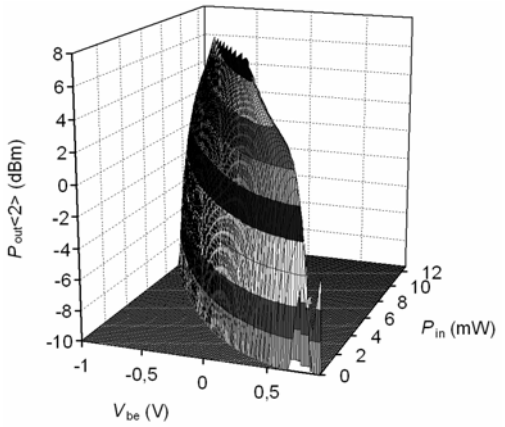


**Fig. 2.** Example of the output power simulation of the second harmonic frequency for the bipolar SiGe transistor BFP540 with 1 GHz input frequency and $V_{ce} = 2.5$ V. The input and output termination of the transistor is 50 Ω.

## 3. Harmonic Termination Analysis

In literature, there are too many opinions how to optimally terminate a frequency multiplier, but there is a widespread belief that one of the best type of harmonic termination is a short circuit (often realized as λ/4 open stub for the desired harmonic). The nearly ideal short circuit with the theoretical value of the impedance $Z_{in} = 0{,}99e^{j180°}$ was chosen as a test harmonic termination. For finding the optimal harmonic termination, a set of simulations of the short circuit combinations were performed. The example of the test circuit for the frequency doubler harmonic termination analysis is shown in Fig. 3. There is only one combination activated, the short circuit for the second harmonic at the input (simultaneously open circuit for the fundamental) and short circuit for the fundamental at the output (simultaneously open circuit for the second harmonic). The optimal bias/drive regimes of operation analysis for each of combination were performed to obtain the maximum possible value of the desired parameter. In the simulations, the fundamental at the input and the desired harmonic at the output were considered as an open circuit for all harmonic

terminations. All terminations, with the theoretical values of impedances, were straightly joined to the nonlinear model of the transistor. For more accurate results this model includes the model of the SOT343 package. As example the optimal harmonic termination analysis results for the frequency doubler are shown in Fig. 4, Fig. 5 and Fig. 6.

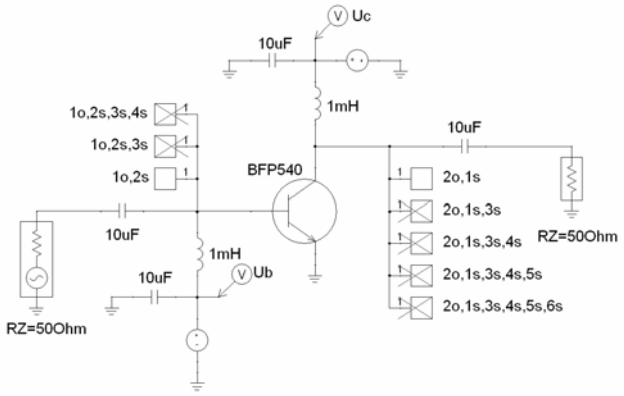


**Fig. 3** Optimal harmonic termination analysis test circuit for the frequency doubler (o – open circuit, s – short circuit).

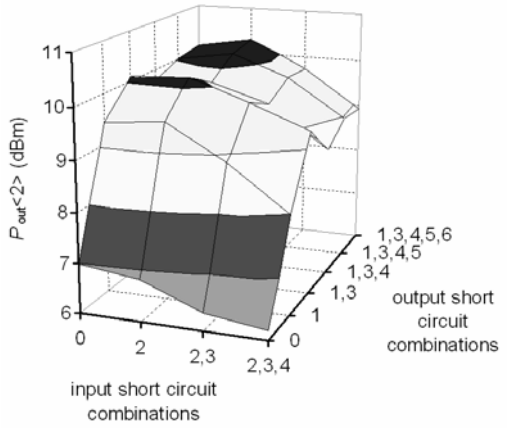


**Fig. 4.** Optimal harmonic termination analysis results for $P_{out}\langle 2\rangle$ of the frequency doubler (SiGe transistor BFP540).

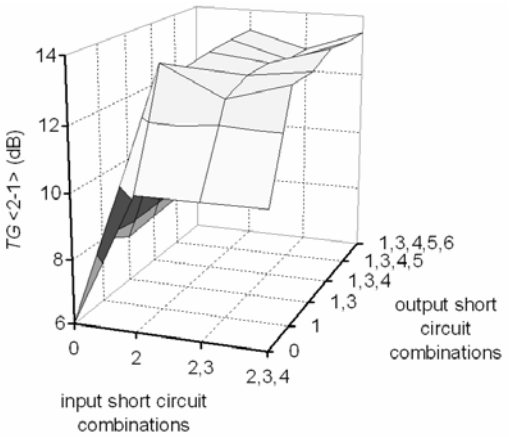


**Fig. 5.** Optimal harmonic termination analysis results for $TG\langle 2\text{-}1\rangle$ of the frequency doubler (SiGe transistor BFP540).

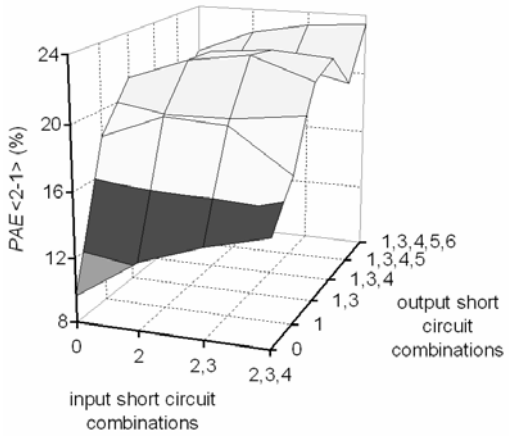


**Fig. 6.** Optimal harmonic termination analysis results for $PAE\langle 2\text{-}1\rangle$ of the frequency doubler (SiGe transistor BFP540). The short circuit for the second harmonic at the input (simultaneously open circuit for the fundamental) and short circuit for the fundamental at the output (simultaneously open circuit for the second harmonic) is the combination which leads to the most significant progression of the parameters.

Tab. 1 shows the chosen optimal combinations of the harmonic termination for the three types of multipliers which are trade off between the best performance and the simplicity of the viability. For example the optimal combination for the frequency doubler, the short circuit for the second harmonic at the input and short circuit for the fundamental at the output, is the simplest combination of harmonic termination, in comparison with no harmonic termination case, which leads to the most significant progression of the frequency multiplier performance (see Fig. 4, Fig. 5 and Fig.6). Evidently there are some other combinations leading to the better absolute values but its viability is incomparably complicated and improvement of performance compared with the chosen combination is not so significant.

| **s – Short Circuit**<br>**o – Open Circuit** | **Input and Output Combinations of Harmonic Termination** | |
|---|---|---|
| **Type of Multiplier** | **Input Network** | **Output Network** |
| **Doubler** | **1o,2s** | **1s,2o** |
| **Tripler** | **1o,3s** | **1s,2s,3o** |
| **Quadrupler** | **1o,4s** | **1s,2s,3s,4o** |

**Tab. 1.** Optimal harmonic termination analysis results for the frequency doubler, the tripler and the quadrupler.

# 4. Input and Output Networks for Active Frequency Multipliers

Some of conclusions, which are introduced above, are very similar or the same as the earlier published results (in particular for the frequency doubler), but the realization of the majority part of the terminating combinations by the standard microstrip technology are very unsuitable or even impossible. A new technique for this reason has been developed. Examples of the two type output networks reali-

zed by the microstrip technology combined with the defected ground structure are shown in Fig. 7 and Fig. 8. All combinations of the impedance terminations mentioned above (Tab. 1) can be implemented this way.

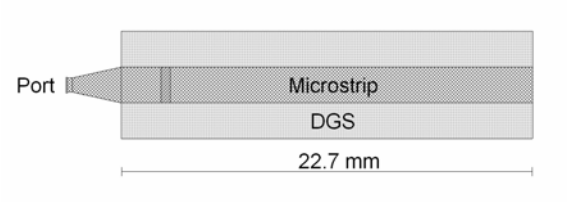


**Fig. 7.** Short circuit for the fundamental and the open circuit for the second harmonic. This frequency doubler output network utilizes a microstrip technology combined with the defected ground structure which is more than twice shorter than the conventional λ/4 (53.45 mm) open microstripline.

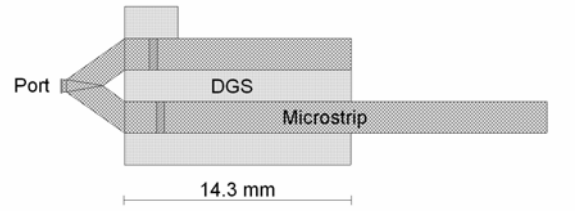


**Fig. 8.** Short circuit for the fundamental and the second harmonic and simultaneously the open circuit for the third harmonic for the tripler output network utilizing a microstrip technology combine with DGS.

## 5. Low-Pass Filter

To accomplish good spectral purity, a new type of low-pass filter has been developed. The combination of the modified conventional stepped impedance LPF with DGS gives great results. The filter and its equivalent model are shown in Fig.9. The photo of the realized low-pass filter for the frequency doubler (the top and the bottom side view) is shown in Fig. 10. The measured s-parameters of this filter denote an acceptable attenuation in the pass-band and the perfect rejection in the stop-band (see Fig. 11).

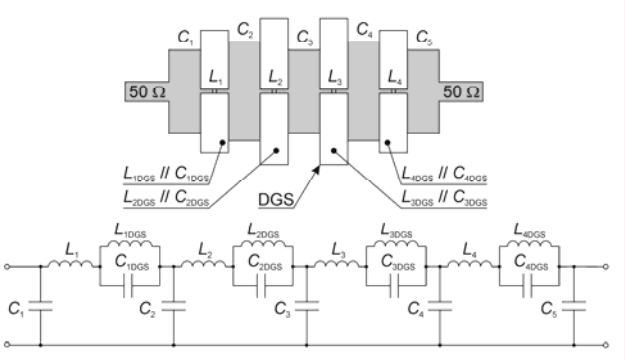


**Fig. 9.** New type of the low-pass filter with the defected ground structure and its equivalent model.

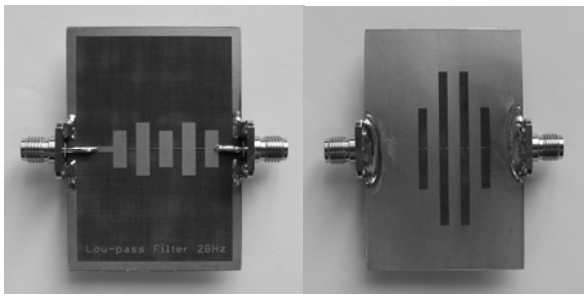


**Fig. 10.** Realized 2 GHz low-pass filter with DGS (the top and the bottom side view). The substrate Arlon DiClad 870 ($\varepsilon_r = 2.33$) with the thickness 0.02" was used for the realization.

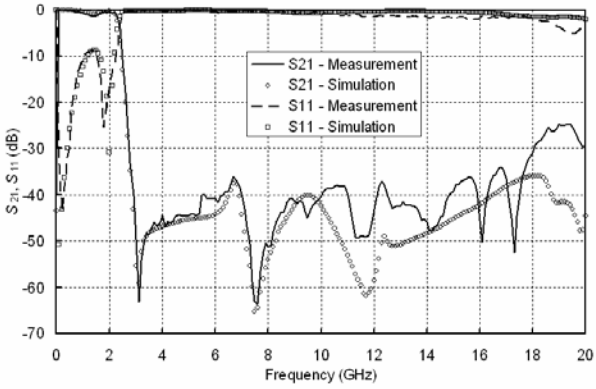


**Fig. 11.** Measured and simulated s-parameters of 2 GHz low-pass filter with DGS. Attenuation for 2 GHz, 3 GHz, 4 GHz, 5 GHz and 6 GHz is 0.53 dB, 49.62 dB, 44.43 dB, 44.40 dB and 40.89 dB respectively.

## 6. Implementation and Measurement

The low cost bipolar SiGe transistor BFP620 (Infineon Technology) was chosen as an active device for the test circuits. The more accurate nonlinear model of the transistor BFP620 in comparison to BFP540 (used for the theoretical investigation in chapters 2 and 3) was the reason of the change. Inaccuracy of the nonlinear model of BFP540 is not so significant and conclusions from the chapters 2 and 3 are valid. The frequency doubler, the tripler and the quadrupler have been realized and measured. An example of the realized frequency tripler with DGS is shown in Fig. 12. The comparison of the measured and the simulated parameters ($P_{out}\langle 3\rangle$, $TG\langle 3\text{-}1\rangle$, $PAE\langle 3\text{-}1\rangle$ and $S_{11}$) of the tripler are shown in Fig. 13 and Fig. 14. The measured output power spectrum is shown in Fig. 15. All of the techniques described above, an optimal bias/drive regimes of operation analysis, the input and the output networks with DGS and a new type of the low-pass filter with DGS (which has no significant influence to the harmonic termination at the output), were used for these advanced multipliers. In addition the load-pull analysis for the desired harmonic at the output and the impedance matching for the fundamental at the input were used for further improvement of the multiplier performance. The best performances for each of them are shown in Tab. 2.

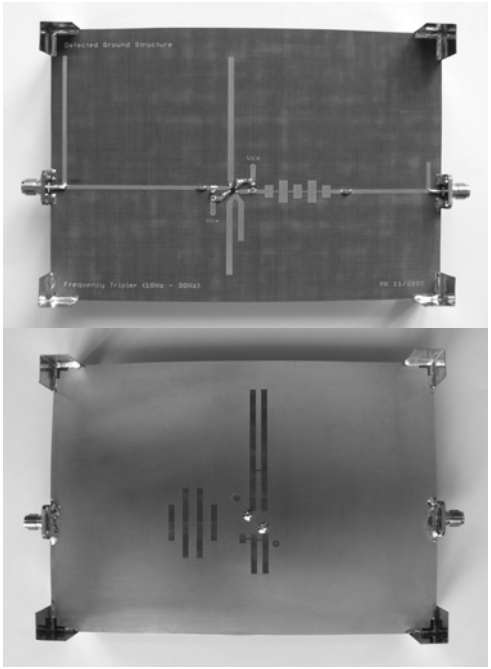

**Fig. 12.** Realized advanced frequency tripler (from 1 GHz to 3 GHz) utilizing the defected ground structure. The substrate Arlon DiClad 870 ($\varepsilon_r$ = 2.33) with the thickness 0.02" was used for the realization.

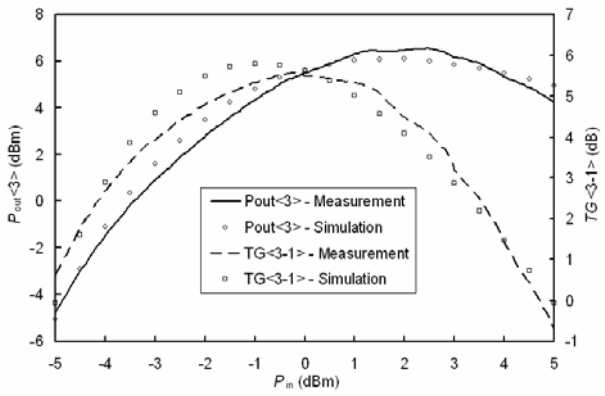


**Fig. 13.** Comparison of the measured and the simulated $P_{out}\langle 3\rangle$ and $TG\langle 3\text{-}1\rangle$ for the frequency tripler with BFP620 ($V_{ce}$ = 2.5 V, $V_{be}$ = 0 V).

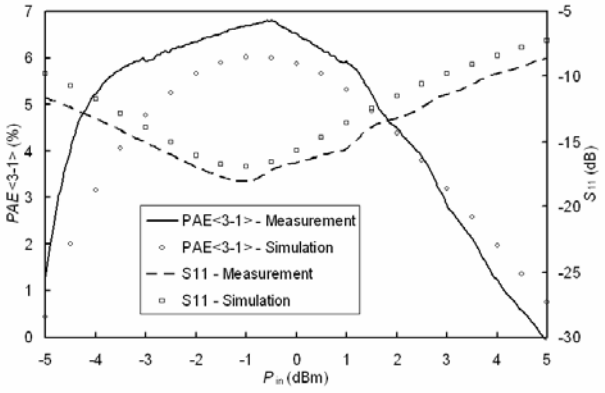


**Fig. 14.** Comparison of the measured and the simulated $PAE\langle 3\text{-}1\rangle$ and $S_{11}$ for the frequency tripler with BFP620 ($V_{ce}$ = 2.5 V, $V_{be}$ = 0 V).

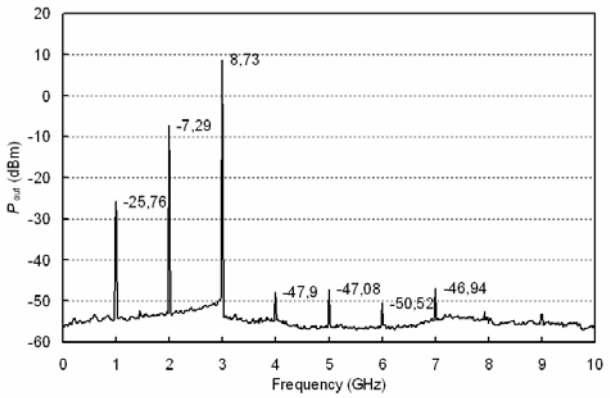


**Fig. 15.** Measured output power spectrum for the frequency tripler with BFP620 ($V_{ce}$ = 2.5 V, $V_{be}$ = -0.6 V, $P_{in}$ = 4 dBm).

| Type of Multiplier | $P_{out}\langle Hm\rangle$ | $TG\langle Hm\text{-}Hn\rangle$ | $PAE\langle Hm\text{-}Hn\rangle$ |
|---|---|---|---|
| **Doubler** | **13.14 dBm** | **14.52 dB** | **32.76 %** |
| **Tripler** | **10.01 dBm** | **5.56 dB** | **10.15 %** |
| **Quadrupler** | **3.48 dBm** | **0.43 dB** | **1.42 %** |

**Tab. 2.** Best performances for proposed active multipliers.

# 7. Conclusion

This paper describes results of the detailed study of a novel design technique for the active frequency multipliers. New optimal bias/drive regimes of operation analysis, the input and the output circuits with DGS and a new type of the low-pass filter with DGS have been developed. Experimental results demonstrate the best performance reported up to date for the active frequency multipliers utilizing BJTs with 1 GHz input frequency.

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## About Authors...

**Petr KUTÍN** was born in 1978 in Vysoké Mýto, Czech Republic. He received his master's degree in electrical engineering from the Brno University of Technology in 2002. At present, he is a PhD student at the Department of Radio Electronics, Brno University of Technology. His research interests are microwave circuits design, optimization and measurements.

**Miroslav KASAL** (born in 1947 in Litomyšl, Czech Republic) graduated in communication engineering from the Faculty of Electrical Engineering, Brno University of Technology, in 1970. In 1984 he obtained his PhD degree in metering engineering. He was the head of the NMR Department and Electronics Laboratory of the Institute of Scientific Instruments, Academy of Science of the Czech Republic (1991-2002). Since 2002 he has been with the Department of Radio Engineering, Faculty of Electrical Engineering and Communication, Brno University of Technology, as associate professor. Dr. Kasal is a senior member of the IEEE. He has authored or coauthored a number of papers in scientific journals and conference proceedings. In 2004 he received the Award of the Rector of the Brno University of Technology and the SIEMENS Prize for research.

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