Simple and Low-Cost Realization of RDS Encoder

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Abstract. *This paper presents a simple and easy way of realization of RDS encoder. Autonomous equipment which is capable to generate wanted data stream, modulate that data stream and mixed generated signal with stereo or mono FM composite multiplex signal is simulated and produced.*

Parts of encoder are described, simulated and measured. The use of RDS makes FM receivers more user-friendly. With this simple and cheap RDS encoder, smaller FM broadcasters have a chance to improve business ability.

Keywords

FM, RDS, D/A Converter, ATmega8, MFB filter, DSB-SC.

1. Introduction

After initial EBU-RDS research, the next goal was to realize RDS autonomous equipment with Atmel microcontroller which will be able to generate a RDS stream without PC assistant.

Subcarrier of the RDS signal is amplitude-modulated by the shaped and bi-phase coded signal. To achieve compatibility with ARI system, RDS uses DSB-SC, that is, amplitude modulation with suppressed subcarrier. Carrier frequency of 57 kHz is obtained from the third harmonic of 19 kHz stereo pilot tone [1]. This method of modulation may alternatively be considered as a form of two-phase phase shift keying (PSK) with a phase deviation of ±90°. Spectrum of FM composite multiplex signal with spectrum of the RDS signal is shown in Fig. 1.

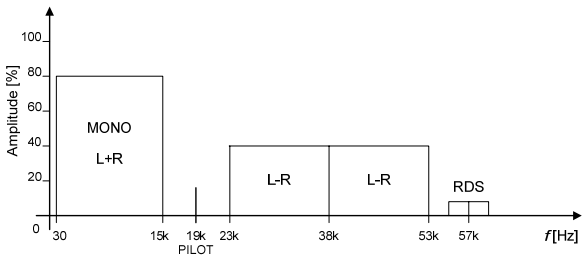

Fig. 1. FM composite multiplex spectrum.

The basic clock frequency is obtained by dividing the transmitted subcarrier frequency by 48 which yields system basic data rate to be 1187.5 bit/s.

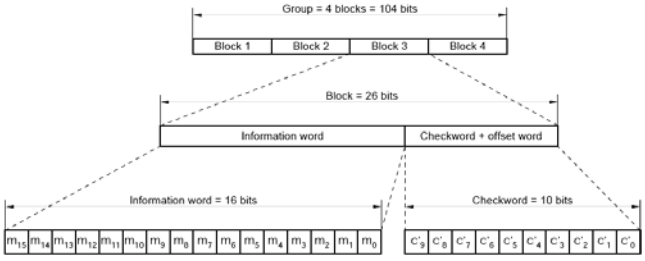

Fig. 2. Structure of the baseband coding.

Fig. 2 shows the structure of the baseband coding. The largest element in the structure is called a "group" having 104 bits. Each group comprises of 4 blocks with 26 bits. Every block consists of information word and a checkword. Information word has 16 bits, while checkword has 10 bits. There are 16 different groups, where each group can be version A and version B. For details about groups see the EBU RDS recommendations [2]. After forming groups, RDS signal is differentially encoded and send to bi-phase modulator.

2. Building RDS Encoder

The main part of the RDS encoder is Atmel microcontroller, ATmega8 [3], which collects user information, forms blocks and groups and generates a 4-bit digital differential bi-phase coded eight times over sampled signal. Next, the signal goes to a 4-bit D/A converter and then to anti-aliasing filter which outputs baseband RDS signal. Finally, RDS signal goes to a DSB-SC modulator where it is modulated with 57 kHz subcarrier and then mixed with stereo or mono FM composite multiplex signal.

2.1 RDS Encoder Block Diagram

The RDS encoder block diagram is shown in Fig. 4. A user uses the keyboard to enter the RDS information like PS, PI, PTY, music/speech flag, mono/stereo flag and TP flag. There is a special key for TA flag which allows toggling TA flag without entering into the setup program. All information and setup enters are shown on an alphanu-

meric 2x16 LCD. Dealing with the encoder is clear and intuitive and is shown in Fig. 3.

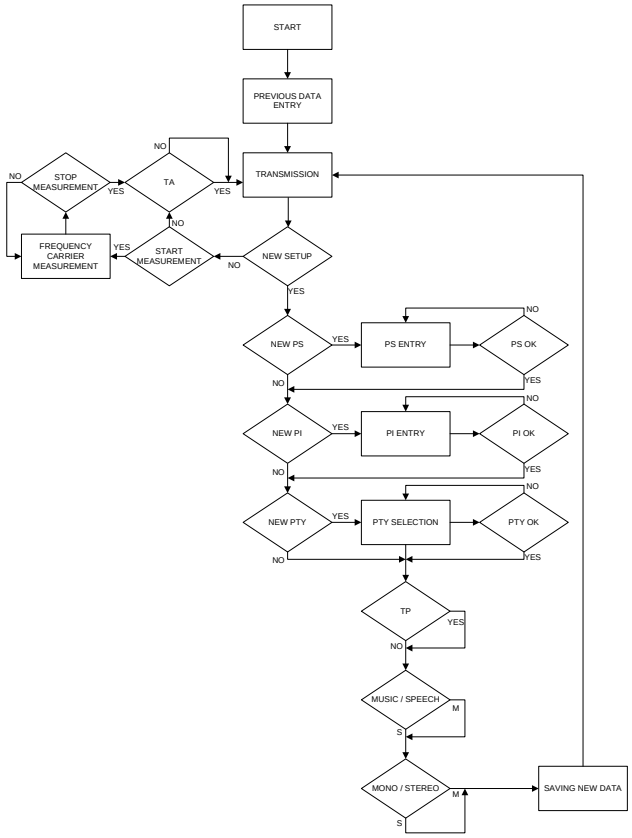

Fig. 3. Microcontroller operating algorithm.

Atmel Atmega8 microcontroller drives LCD and keyboard to collect RDS information and then generates blocks and groups. Next task for ATmega8 is to generate 4-bit differential bi-phase signal. Other blocks in RDS block diagram are explained in detail further on.

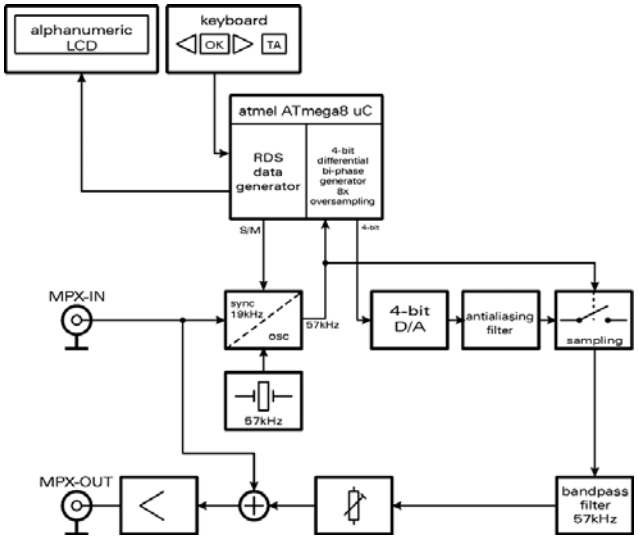

Fig. 4. RDS encoder block diagram.

2.2 4-Bit D/A Converter

The 4-bit D/A converter is done with a R-2R ladder network as shown in Fig. 5 and produces the output voltage according to (1), where the D's take the value 0 or 1 and V_{ref}= 5 V.

$$V_{\text{out}} = \frac{RF}{R}\left(\frac{D_3}{2}+\frac{D_2}{4}+\frac{D_1}{8}+\frac{D_0}{16}\right)\cdot V_{\text{ref}} \tag{1}$$

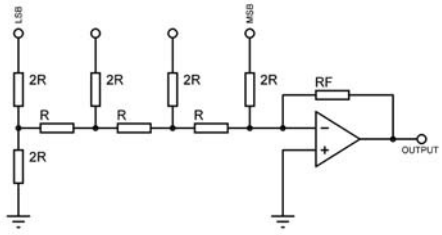

Fig. 5. R-2R ladder network.

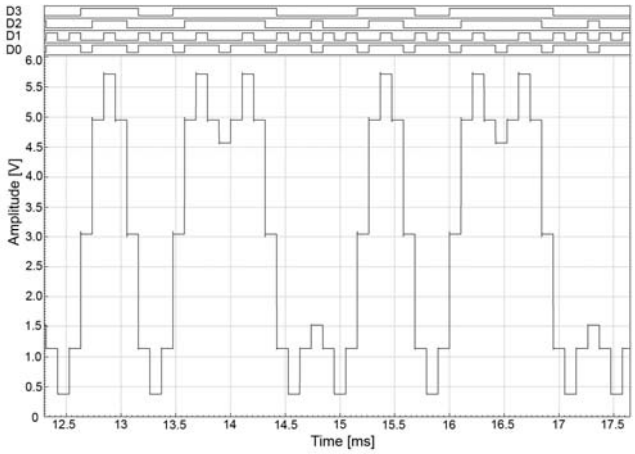

Fig. 6. Digital RDS signal.

Digitally generated eight time over sampled RDS signal after D/A converter and related 4-bit bus states are shown in Fig. 6. At this point anti-aliasing filter is needed to smooth this curve.

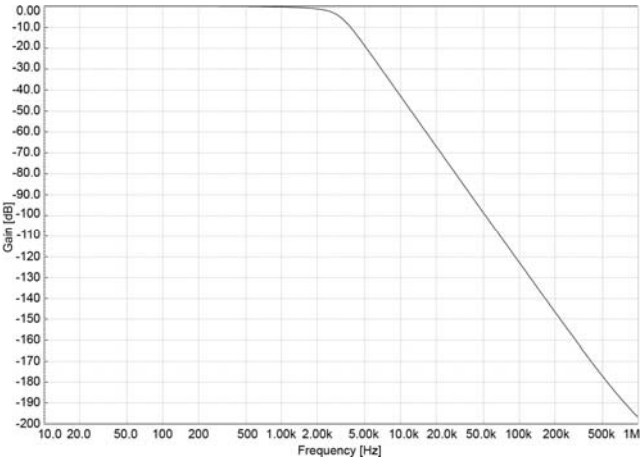

Fig. 7. Anti-aliasing filter frequency response.

2.3 Anti-Aliasing Filter

Since baseband RDS signal is eight times over sampled digitally generated, overtones are occurring. The first overtone is 8 x 1.1875 kHz = 9.5 kHz. The anti-aliasing filter is needed to suppress the overtones. This filter is fourth order active lowpass filter and it's made with cascading three MFB filter topology stages. Its frequency response is shown in Fig. 7, where it can be seen that the first overtone is suppressed with approximately 40 dB. After RDS signal passes through the filter, only baseband bi-phase signal remains as shown in Fig. 8.

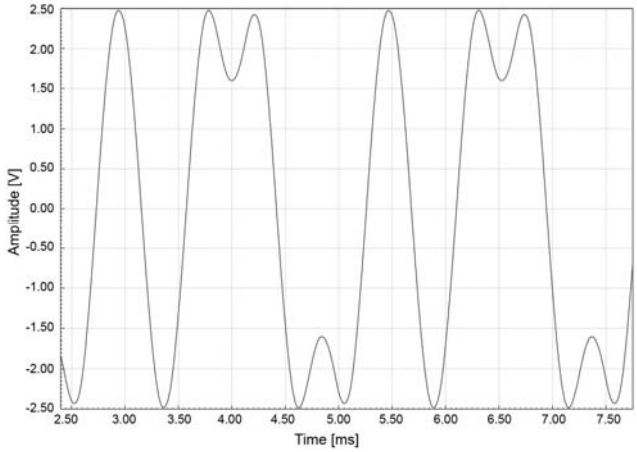

Fig. 8. Baseband RDS bi-phase signal.

Spectrum of the baseband bi-phase signal is shown in Fig. 9. Maximum baseband frequency is 2.4 kHz, and all the frequencies above 2.4 kHz are suppressed over 30 dB.

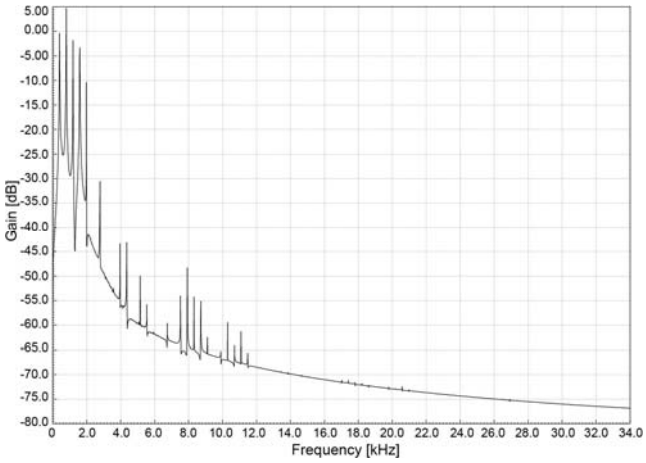

Fig. 9. Spectrum of bi-phase signal.

2.4 DSB-SC Modulation

Double side band - suppressed carrier modulation method is described as

$$u_{\mathrm{DSB-SC}}(t) = u_{\mathrm{m}}(t) \cdot \cos(\omega_0 t) \tag{2}$$

where $u_{\mathrm{m}}(t)$ is the modulation signal, and ω_0 is the circular frequency of the modulated carrier. If $u_{\mathrm{m}}(t)$ is a harmonious function such as,

$$u_{\mathrm{m}}(t) = A\cos(\omega_{\mathrm{m}} t) \tag{3}$$

where A is the amplitude of the modulation signal and ω_{m} is the circular frequency of the modulation signal. Using (2) and (3) gives the DSB-SC expression as follows,

$$u_{\mathrm{DSB-SC}}(t) = A\cos(\omega_{\mathrm{m}} t)\cos(\omega_0 t) \tag{4}$$

and finally in (5) we can see that the DSB-SC modulation method have an upper side band ($\omega_0 + \omega_{\mathrm{m}}$) and a lower side band ($\omega_0 - \omega_{\mathrm{m}}$) around the suppressed carrier.

$$u_{\mathrm{DSB-SC}}(t) = \frac{A}{2}\cos\left[(\omega_0 + \omega_{\mathrm{m}})\cdot t\right] + \frac{A}{2}\cos\left[(\omega_0 - \omega_{\mathrm{m}})\cdot t\right] \tag{5}$$

DSB-SC realization in our case is obtained by sampling the baseband bi-phase signal with a 57 kHz clock and filtering around 57 kHz with a bandpass filter. The bandpass filter is fourth order active filter (type Butterworth) shown in Fig. 10.

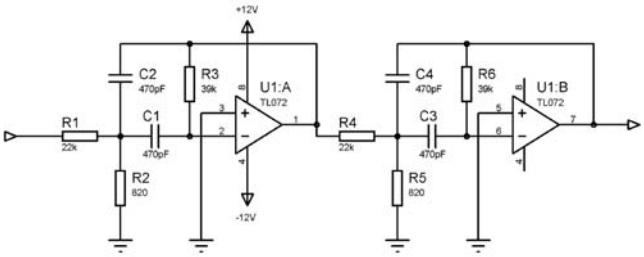

Fig. 10. Bandpass filter.

The whole principle of DSB-SC modulation with this method is shown in Fig. 11. After the DSB-SC realization method, a RDS signal obtains the final figure as shown in Fig. 12. The related spectrum is shown in Fig. 13.

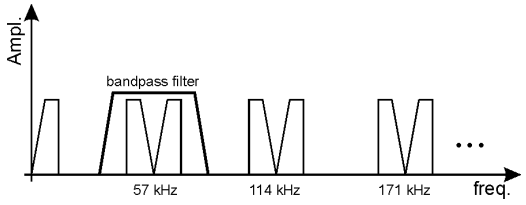

Fig. 11. DSB-SC realization.

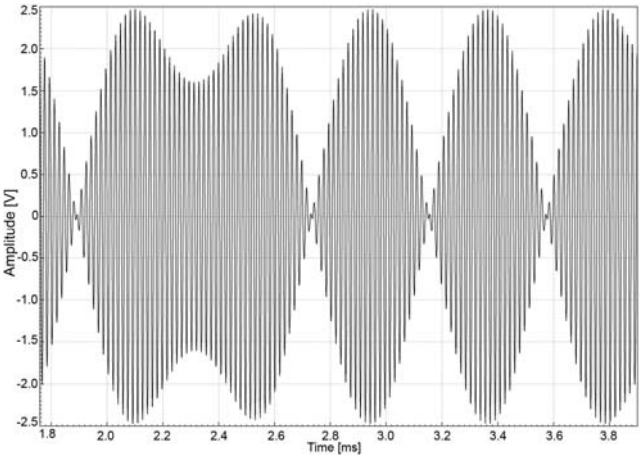

Fig. 12. DSB-SC modulated RDS signal.

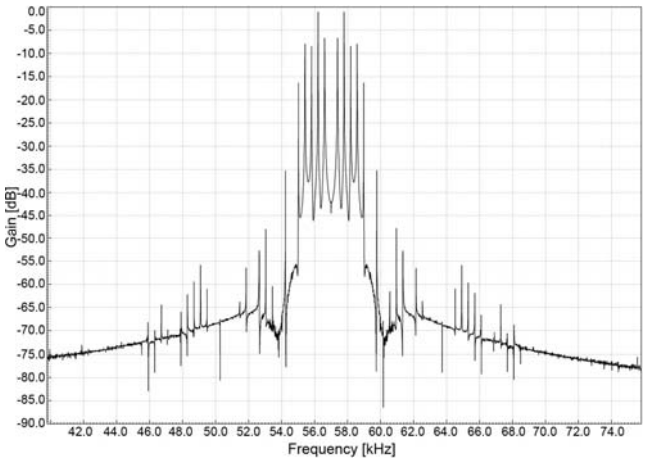

Fig. 13. RDS signal spectrum.

2.5 Subcarrier Oscillator 57 kHz

There are two modes of operation depending whether RDS encoder operates in mono or stereo mode. As shown earlier in Fig. 4, there is control signal coming from an ATmega8 microcontroller, which, using a digital switch, decides which subcarrier oscillator will be in use. When the RDS encoder operates in mono mode, a subcarrier oscillator is stand-alone quartz controlled digital oscillator, done with PLL [4]. This is because for stereo mode the subcarrier must be locked to the third harmonic of the 19 kHz pilot-tone. The tolerance of the frequency for the 19 kHz pilot-tone is ±2 Hz; therefore the tolerance for the frequency of the subcarrier during stereo broadcast is ±6 Hz. Fig. 14 shows the block diagram of the PLL system. First, the 19 kHz bandpass filter is needed to isolate 19 kHz stereo pilot-tone from the MPX signal. Next, the signal goes to the phase detector where it is compared with a three times divided VCO signal. The phase detector gives error signal which passes through the lowpass filter controlled by the VCO. Since the signal from the VCO is three times divided, frequency of the output signal is three times multiplied, thus 3x19 kHz = 57 kHz.

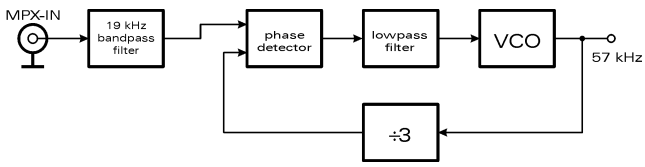

Fig. 14. PLL system.

Fig. 15 shows the waveform of the 19 kHz input and 57 kHz output of the PLL circuit.

2.6 Summation Block

The last issue is to sum RDS signal with a FM composite stereo multiplex or mono signal depending on the input signal. We can use a variable resistor which is used to set the RDS signal level. After the summing, buffer amplifier outputs the MPX and RDS signal together as shown in Fig. 4. The related spectrum is shown in Fig. 1.

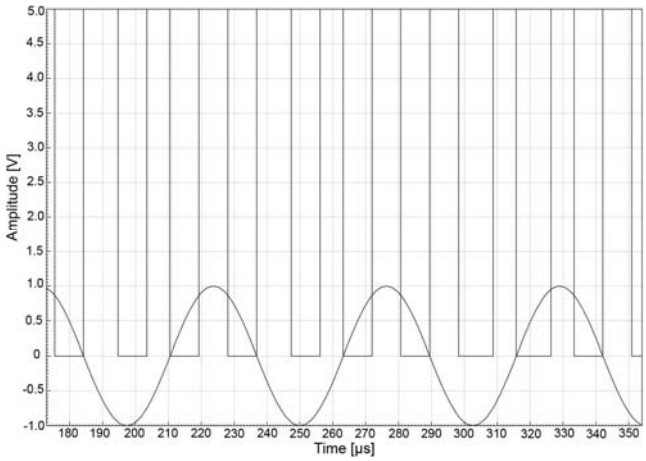

Fig. 15. PLL signals.

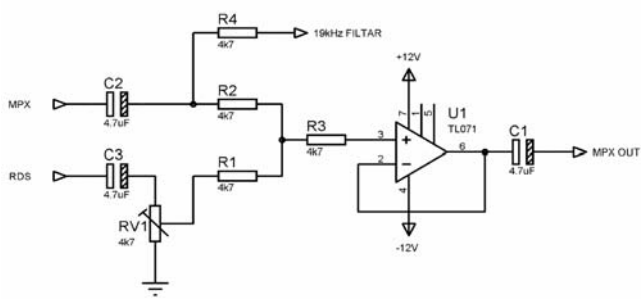

Fig. 16. Realization of summation block.

3. RDS Encoder Measurements

Following the building of the RDS encoder, we have done several measurements. All the results were similar to the ones obtained with the simulations. Fig. 17. shows the RDS signal in time domain. The related spectrum is shown in Fig. 18. RDS encoder prototype is shown in Fig. 19.

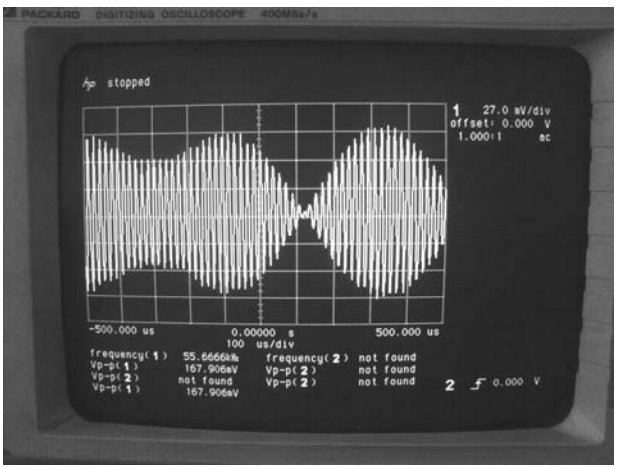

Fig. 17. RDS signal.

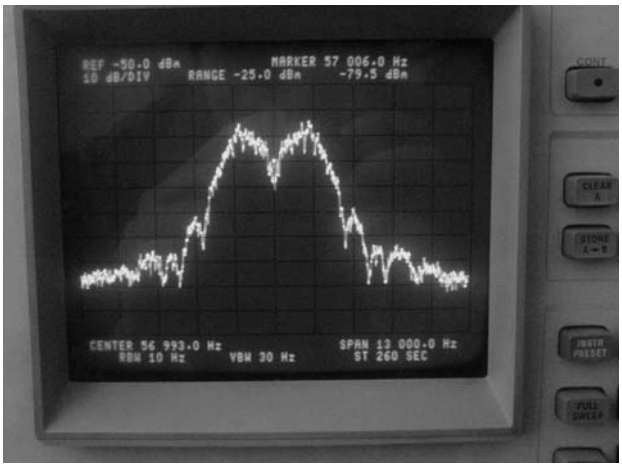

Fig. 18. RDS signal spectrum.

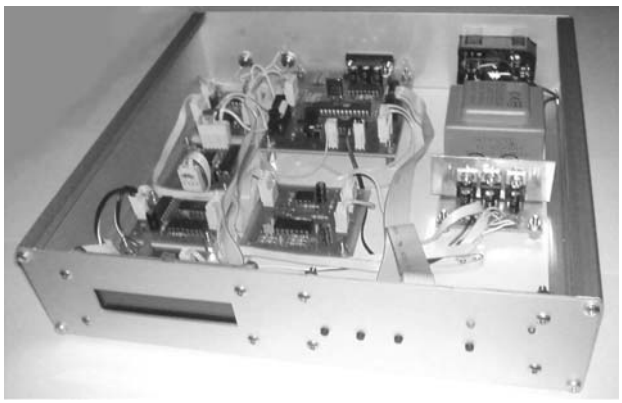

Fig. 19. RDS encoder prototype.

4. Conclusion

The goal was to make simple RDS autonomous equipment. That is done using only one microcontroller for collecting data and for generating bi-phase signal. There is a RS232 port on RDS encoder which can be used to connect to a PC.

RDS encoder was tested on air with FM transmitter and it worked within expectations.

Future work on RDS encoder is to implement alternative frequencies (AF), radio text (RT), enhanced other networks information (EON) and clock time (CT). We will try to minimize the number of hardware elements and build the RDS encoder with a SMD technology.

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